FPGA Assignment1

EE22MTECH02002

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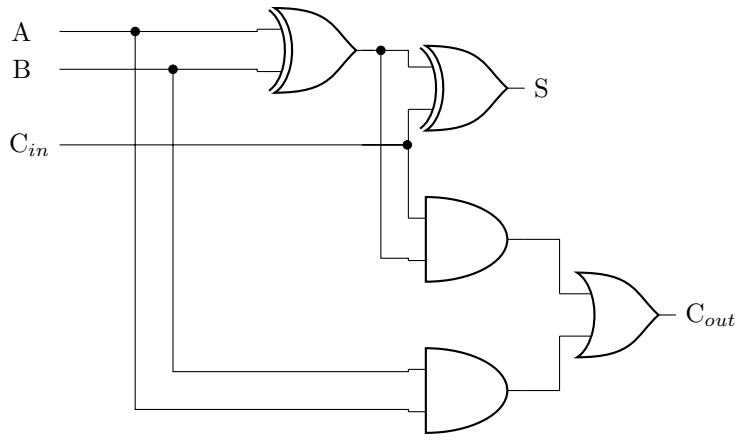
1 Question

Differentiate Between Half adder and Full adder. Draw the Logic Diagram of full adder.

2 Answer

S. No.	HALF ADDER	FULL ADDER
1.	The half adder produces a sum of the two inputs.	The full adder produces a sum of the two inputs and carry value.
2.	Previous carry is not used.	Previous carry is used.
3.	It consists of one EX-OR gate and one AND gate.	It consists of two EX-OR, two AND gate and one OR gate.
4.	Logical Expression for half adder is : S=A $\oplus B; C = A.B$.	Logical Expression for Full adder is : S=A $\oplus B \oplus Cin; Cout = (A.B) + (Cin.(A \oplus B))$.

Full Adder Diagram.



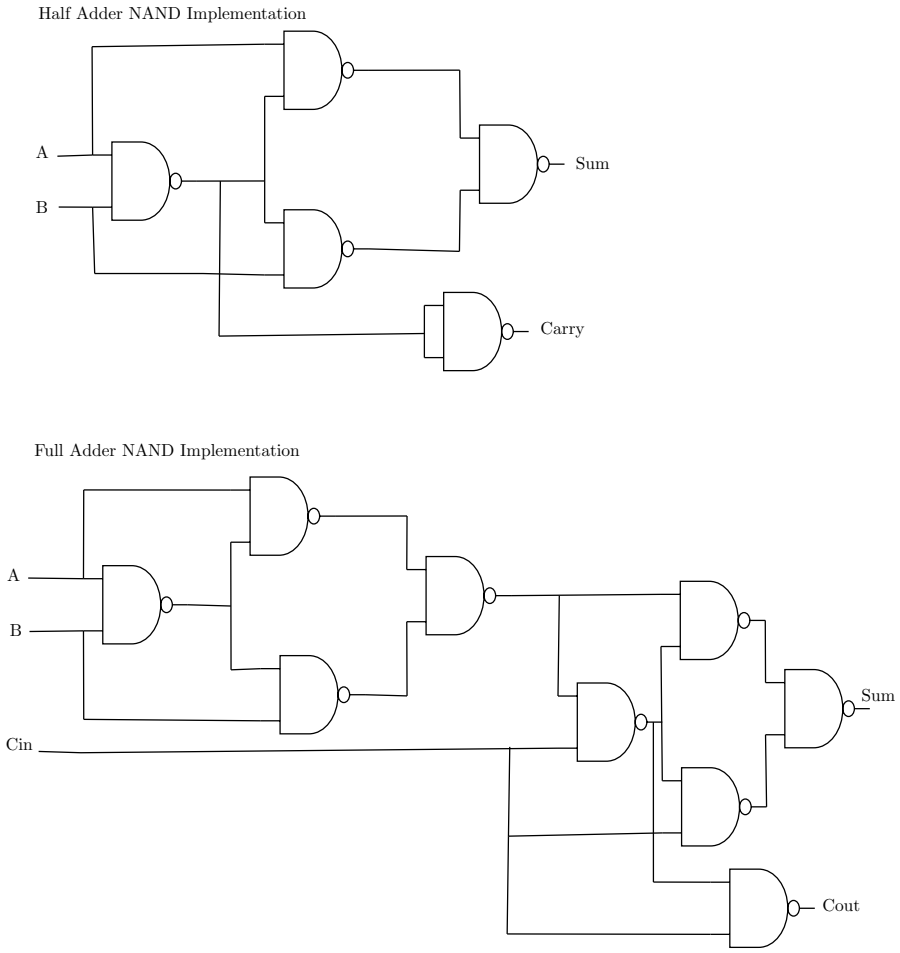


Figure 1: Circuit Diagram of NAND Gate Implementation of Half Adder and Full Adder