



An Infineon Technologies Company

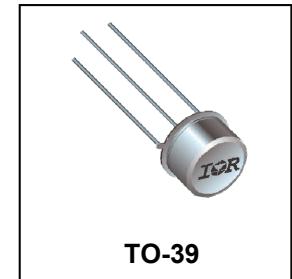
**IRFF110**  
**JANTX2N6782**  
**JANTXV2N6782**

**REPETITIVE AVALANCHE AND dv/dt RATED  
 HEXFET® TRANSISTORS  
 THRU-HOLE TO-205AF (TO-39)**

**100V, N-CHANNEL**  
 REF: MIL-PRF-19500/556

**Product Summary**

Part Number	BVDSS	RDS(on)	I <sub>D</sub>
IRFF110	100V	0.60Ω	3.5A



**Description**

The HEXFET® technology is the key to International Rectifier's HiRel advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on state resistance combined with high trans conductance.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high energy pulse circuits.

**Absolute Maximum Ratings**

Symbol	Parameter	Value	Units
I <sub>D1</sub> @ V <sub>GS</sub> = 10V, T <sub>C</sub> = 25°C	Continuous Drain Current	3.5	A
I <sub>D2</sub> @ V <sub>GS</sub> = 10V, T <sub>C</sub> = 100°C	Continuous Drain Current	2.25	
I <sub>DM</sub> @ T <sub>C</sub> = 25°C	Pulsed Drain Current ①	14	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation	15	W
	Linear Derating Factor	0.12	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	±20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	68	mJ
I <sub>AR</sub>	Avalanche Current ①	3.5	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	1.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.5	V/ns
T <sub>J</sub>	Operating Junction and	-55 to + 150	°C
T <sub>STG</sub>	Storage Temperature Range		
	Lead Temperature	300 (0.063 in. /1.6 mm from case for 10s)	
	Weight	0.98 (Typical)	g

For Footnotes, refer to the page 2.

### Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0\text{V}$ , $I_D = 1.0\text{mA}$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.10	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D = 1.0\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.60	$\Omega$	$V_{GS} = 10\text{V}$ , $I_{D2} = 2.25\text{A}$ ④
		—	—	0.61		$V_{GS} = 10\text{V}$ , $I_{D1} = 3.5\text{A}$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}$ , $I_D = 250\mu\text{A}$
$Gfs$	Forward Transconductance	0.8	—	—	S	$V_{DS} = 15\text{V}$ , $I_{D2} = 2.25\text{A}$ ④
$I_{DSS}$	Zero Gate Voltage Drain Current	—	—	25	$\mu\text{A}$	$V_{DS} = 80\text{V}$ , $V_{GS} = 0\text{V}$
		—	—	250		$V_{DS} = 80\text{V}$ , $V_{GS} = 0\text{V}$ , $T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Leakage Forward	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Leakage Reverse	—	—	-100		$V_{GS} = -20\text{V}$
$Q_G$	Total Gate Charge	—	—	8.1	nC	$I_{D1} = 3.5\text{A}$
$Q_{GS}$	Gate-to-Source Charge	—	—	1.7		$V_{DS} = 50\text{V}$
$Q_{GD}$	Gate-to-Drain ('Miller') Charge	—	—	4.5		$V_{GS} = 10\text{V}$
$t_{d(on)}$	Turn-On Delay Time	—	—	15	ns	$V_{DD} = 50\text{V}$
$t_r$	Rise Time	—	—	25		$I_{D1} = 3.5\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	—	25		$R_G = 7.5\Omega$
$t_f$	Fall Time	—	—	20		$V_{GS} = 10\text{V}$
$L_s + L_D$	Total Inductance	—	7.0	—	nH	Measured from Drain lead (6mm / 0.25 in from package) to Source lead (6mm / 0.25 in from package) with Source wire internally bonded from Source pin to Drain pin
$C_{iss}$	Input Capacitance	—	180	—	pF	$V_{GS} = 0\text{V}$
$C_{oss}$	Output Capacitance	—	82	—		$V_{DS} = 25\text{V}$
$C_{rss}$	Reverse Transfer Capacitance	—	15	—		$f = 1.0\text{MHz}$

### Source-Drain Diode Ratings and Characteristics

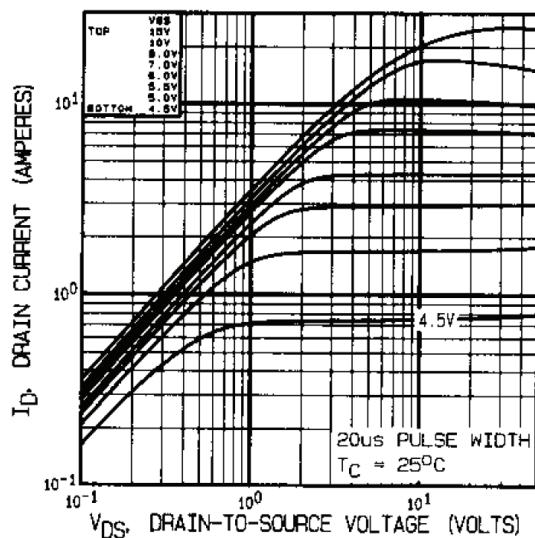
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	3.5	A	
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	14		
$V_{SD}$	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}$ , $I_S = 3.5\text{A}$ , $V_{GS} = 0\text{V}$ ④
$t_{rr}$	Reverse Recovery Time	—	—	180	ns	$T_J = 25^\circ\text{C}$ , $I_F = 3.5\text{A}$ , $V_{DD} \leq 50\text{V}$
$Q_{rr}$	Reverse Recovery Charge	—	—	2.0		$di/dt = 100\text{A}/\mu\text{s}$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_s + L_D$ )				

### Thermal Resistance

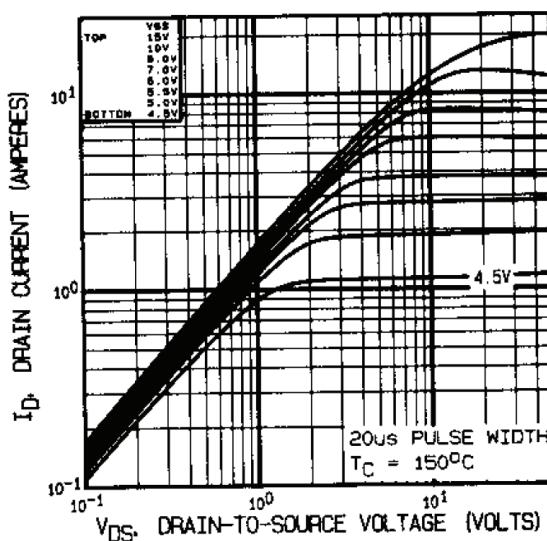
Symbol	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	8.33	°C/W
$R_{\theta JA}$	Junction-to-Ambient (Typical Socket Mount)	—	—	175	

#### Footnotes:

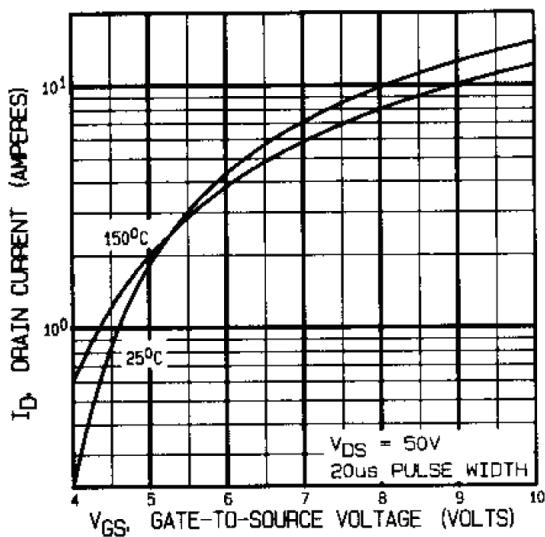
- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ②  $V_{DD} = 25\text{V}$ , starting  $T_J = 25^\circ\text{C}$ , Peak  $I_L = 3.5\text{A}$
- ③  $I_{SD} \leq 3.5\text{A}$ ,  $di/dt \leq 75\text{A}/\mu\text{s}$ ,  $V_{DD} \leq 100\text{V}$ ,  $T_J \leq 150^\circ\text{C}$ , Suggested  $R_G = 7.5\Omega$
- ④ Pulse width  $\leq 300\ \mu\text{s}$ ; Duty Cycle  $\leq 2\%$



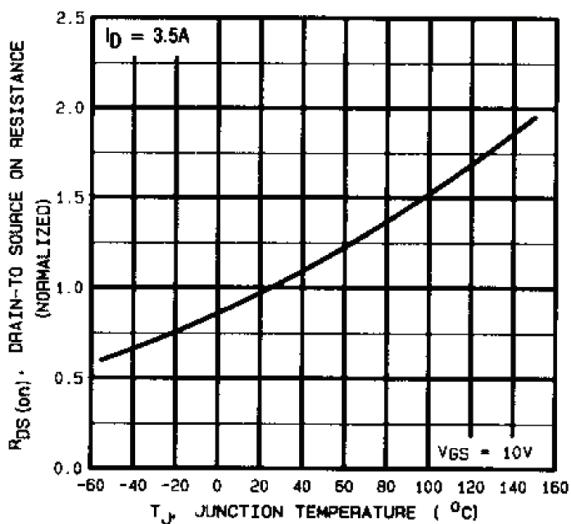
**Fig 1.** Typical Output Characteristics



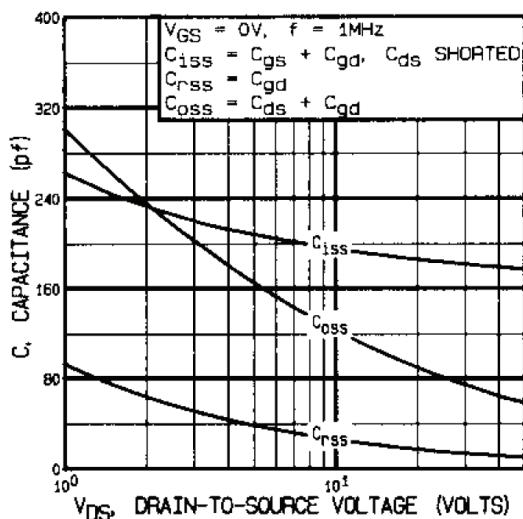
**Fig 2.** Typical Output Characteristics



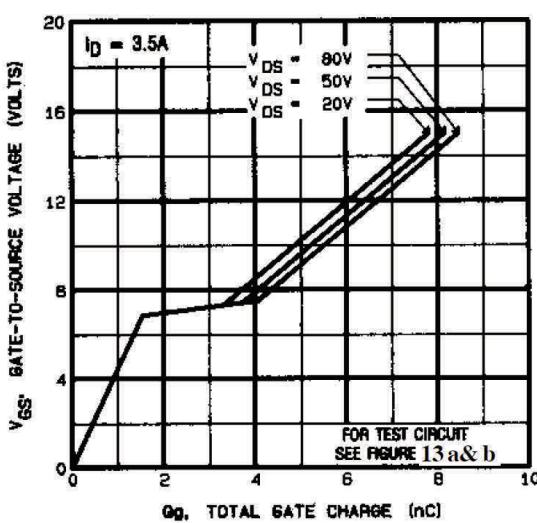
**Fig 3.** Typical Transfer Characteristics



**Fig 4.** Normalized On-Resistance Vs. Temperature



**Fig 5.** Typical Capacitance Vs.  
Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs.  
Gate-to-Source Voltage

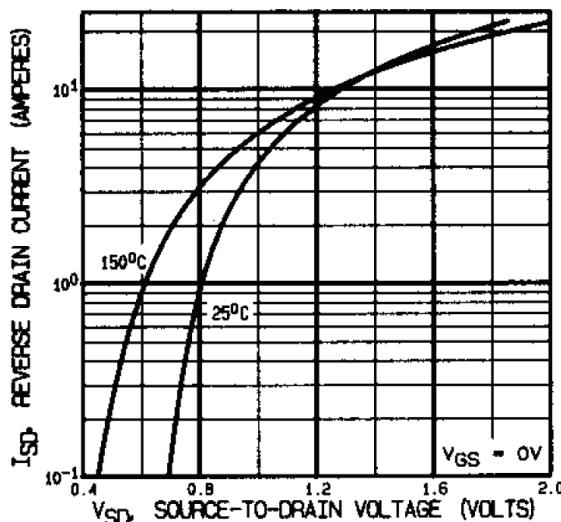


Fig 7. Typical Source-Drain Diode Forward Voltage

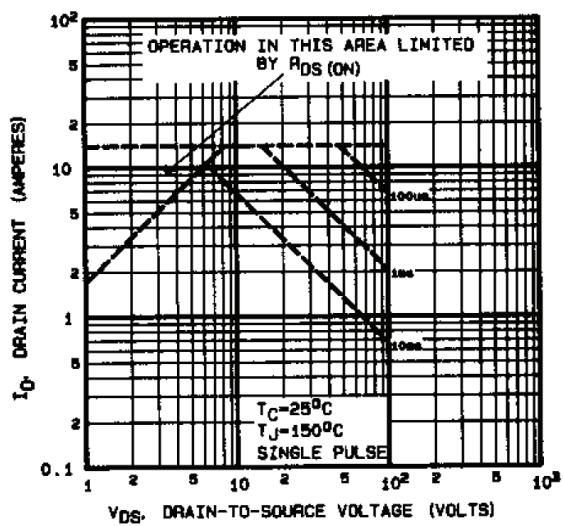


Fig 8. Maximum Safe Operating Area

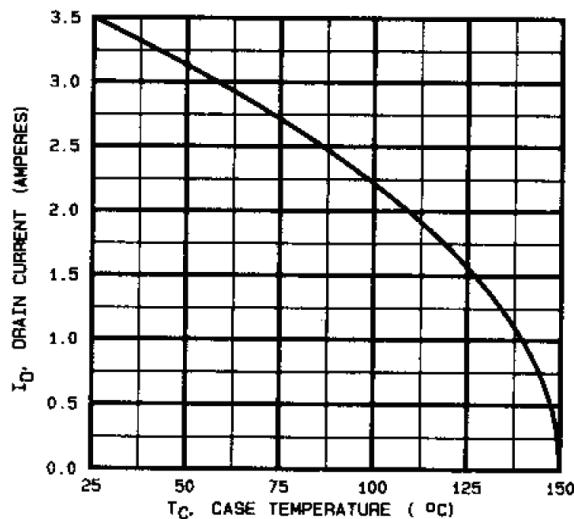


Fig 9. Maximum Drain Current Vs. Case Temperature

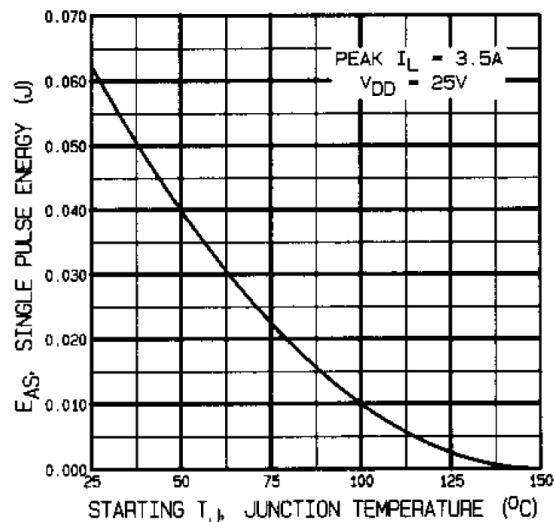


Fig 10. Maximum Avalanche Energy Vs. Drain Current

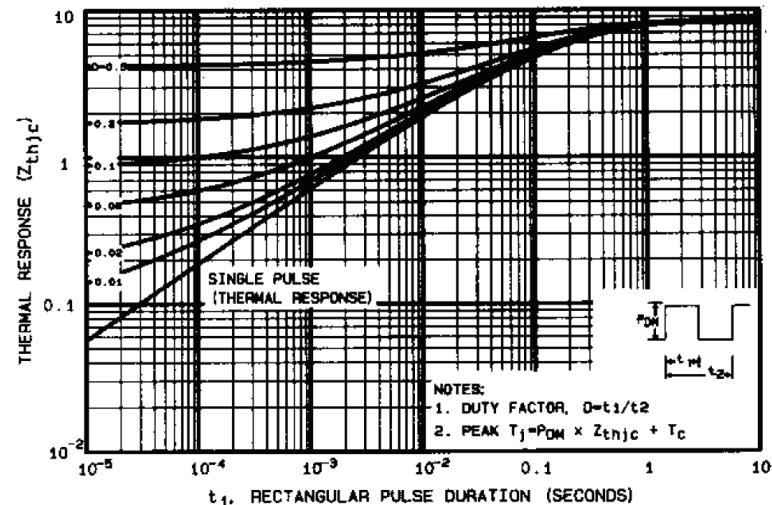
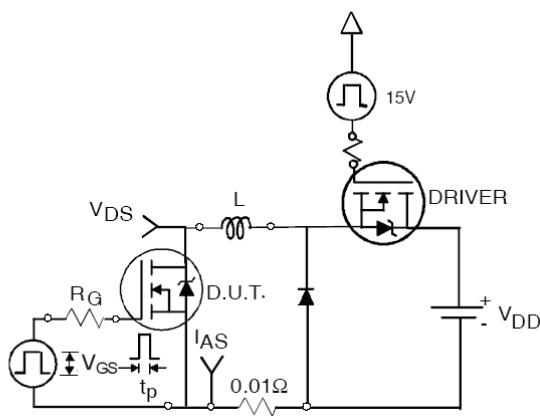
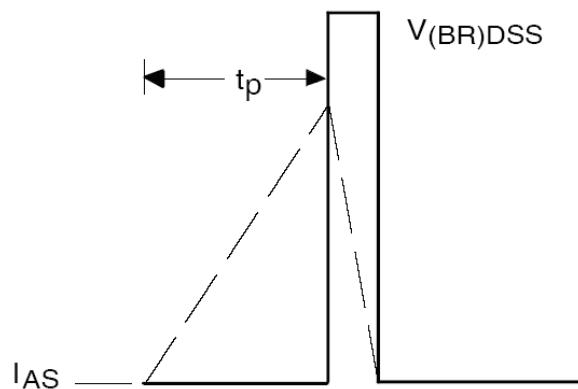


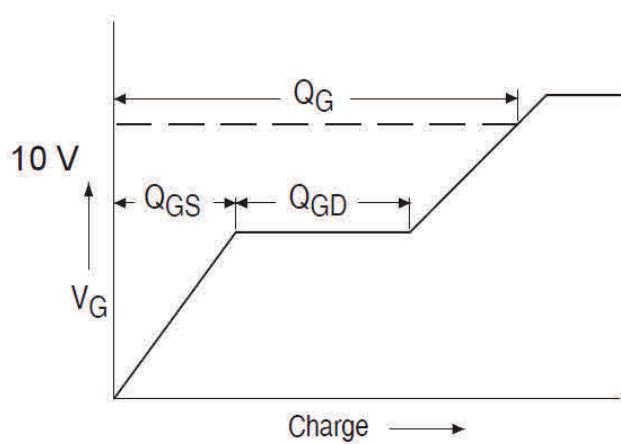
Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case



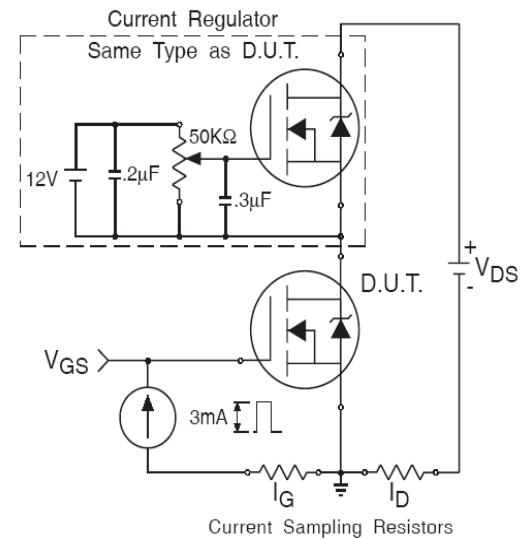
**Fig 12a.** Unclamped Inductive Test Circuit



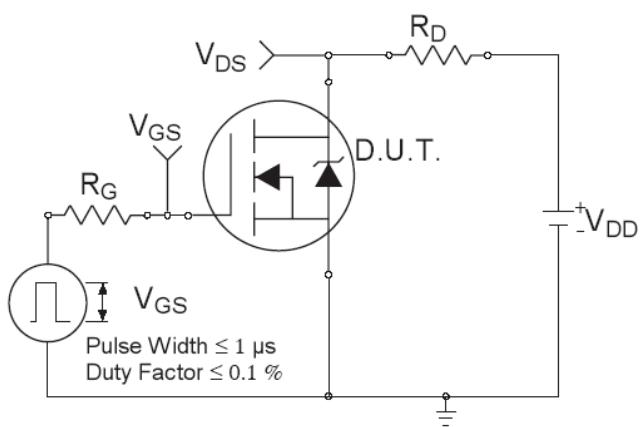
**Fig 12b.** Unclamped Inductive Waveforms



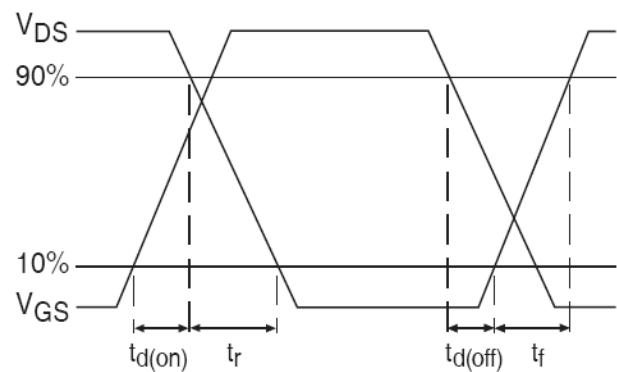
**Fig 13a.** Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

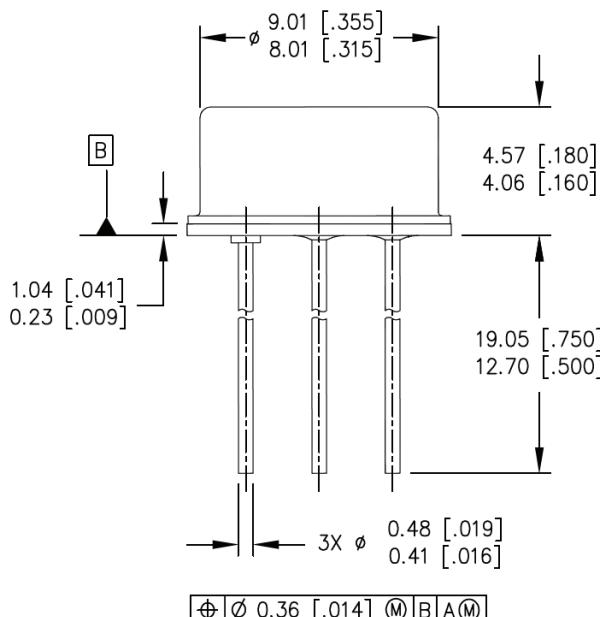


**Fig 14a.** Switching Time Test Circuit



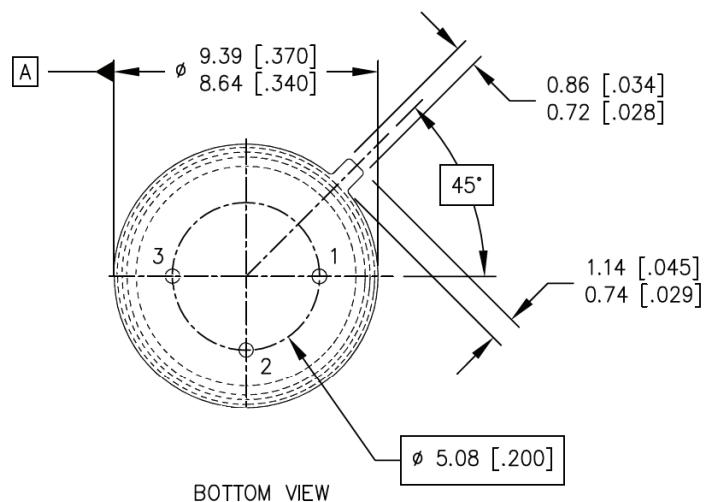
**Fig 14b.** Switching Time Waveforms

### Case Outline and Dimensions - TO-205AF (TO-39)



NOTES: SIDE VIEW

1. DIMENSIONING AND TOLERANCING PER ASME 14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO-205AF (TO-39).



#### LEGEND

- 1- SOURCE
- 2- GATE
- 3- DRAIN (CONNECTED TO THE CASE)

**IMPORTANT NOTICE**

The information given in this document shall be in no event regarded as guarantee of conditions or characteristic. The data contained herein is a characterization of the component based on internal standards and is intended to demonstrate and provide guidance for typical part performance. It will require further evaluation, qualification and analysis to determine suitability in the application environment to confirm compliance to your system requirements.

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