



40V N-Channel MOSFET

Lead Free Package and Finish

General Features

- Proprietary New Trench Technology
- $R_{DS(ON),typ.}=2.1\text{ m }\Omega @ V_{GS}=10\text{V}$
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

BV_{DSS}	$R_{DS(ON),typ.}$	$I_D^{[2]}$
40V	2.1mΩ	240A

Applications

- High efficiency DC/DC Converters
- Synchronous Rectification
- UPS Inverter

Ordering Information

Part Number	Package	Brand
PTP03N04N	TO-220	

Absolute Maximum Ratings

$T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	PTP03N04N	Unit
V_{DSS}	Drain-to-Source Voltage ^[1]	40	V
V_{GSS}	Gate-to-Source Voltage	± 20	
I_D	Continuous Drain Current ^[2]	240	A
	Continuous Drain Current ^[3]	80	
	Continuous Drain Current @ $T_C=100^\circ\text{C}$ ^[2]	180	
I_{DM}	Pulsed Drain Current at $V_{GS}=10\text{V}$ ^[2,4]	960	
E_{AS}	Single Pulse Avalanche Energy	1500	mJ
dv/dt	Peak Diode Recovery $dv/dt^{[3]}$	5.0	V/ns
P_D	Power Dissipation	300	W
	Derating Factor above 25°C	2.0	W/ $^\circ\text{C}$
T_L T_{PAK}	Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	300 260	$^\circ\text{C}$
	Operating and Storage Temperature Range	-55 to 175	

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	PTP03N04N	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	

Electrical Characteristics

OFF Characteristics $T_J = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	40	--	--	V	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_D=250\mu\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	--	--	5	uA	$\text{V}_{\text{DS}}=40\text{V}, \text{V}_{\text{GS}}=0\text{V}$
		--	--	100		$\text{V}_{\text{DS}}=32\text{V}, \text{V}_{\text{GS}}=0\text{V}, \text{T}_J=125^\circ\text{C}$
I_{GSS}	Gate-to-Source Leakage Current	--	--	+100	nA	$\text{V}_{\text{GS}}=+20\text{V}, \text{V}_{\text{DS}}=0\text{V}$
		--	--	-100		$\text{V}_{\text{GS}}=-20\text{V}, \text{V}_{\text{DS}}=0\text{V}$

ON Characteristics

$T_J = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$\text{R}_{\text{DS(ON)}}$	Static Drain-to-Source On-Resistance	--	2.1	3.0	$\text{m}\Omega$	$\text{V}_{\text{GS}}=10\text{V}, \text{I}_D=80\text{A}$ [5]
$\text{V}_{\text{GS(TH)}}$	Gate Threshold Voltage	2.0	--	4.0	V	$\text{V}_{\text{DS}}=\text{V}_{\text{GS}}, \text{I}_D=250\mu\text{A}$
gfs	Forward Transconductance	--	221	--	S	$\text{V}_{\text{DS}}=10\text{V}, \text{I}_D=80\text{A}$ [5]

Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{iss}	Input Capacitance	--	5.02	--	nF	$\text{V}_{\text{GS}}=0\text{V}, \text{V}_{\text{DS}}=25\text{V}, \text{f}=1.0\text{MHz}$
C_{rss}	Reverse Transfer Capacitance	--	0.29	--		
C_{oss}	Output Capacitance	--	0.79	--		
R_G	Gate Series Resistance	--	1.8	--	Ω	$\text{f}=1.0\text{MHz}$
Q_g	Total Gate Charge	--	74	--	nC	$\text{V}_{\text{DD}}=20\text{V}, \text{I}_D=80\text{A}, \text{V}_{\text{GS}}=0 \text{ to } 10\text{V}$
Q_{gs}	Gate-to-Source Charge	--	23	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	26	--		

Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$\text{t}_{\text{d(ON)}}$	Turn-on Delay Time	--	19	--	nS	$\text{V}_{\text{DD}}=20\text{V}, \text{I}_D=80\text{A}, \text{V}_{\text{GS}}=10\text{V}, \text{R}_G=2.5\Omega$
t_{rise}	Rise Time	--	67	--		
$\text{t}_{\text{d(OFF)}}$	Turn-Off Delay Time	--	49	--		
t_{fall}	Fall Time	--	31	--		

Source-Drain Body Diode Characteristics

T_J=25°C unless otherwise specified

Symbol	Parameter	Min	Typ.	Max.	Unit	Test Conditions
I _{SD}	Continuous Source Current ^[2]	--	--	240	A	Integral PN-diode in MOSFET
I _{SM}	Pulsed Source Current ^[2]	--	--	960		
V _{SD}	Diode Forward Voltage	--	0.90	1.2	V	I _S =80A, V _{GS} =0V
t _{rr}	Reverse recovery time	--	77	--	ns	V _{GS} =0V, I _F =80A, dI _F /dt=100A/μs
Q _{rr}	Reverse recovery charge	--	53	--	nC	

Note:

[1] T_J=+25°C to +175°C .

[2] Silicon limited current only.

[3] Package limited current.

[4] Repetitive rating; pulse width limited by maximum junction temperature.

[5] Pulse width≤380μs; duty cycle≤2%.

Typical Characteristics

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

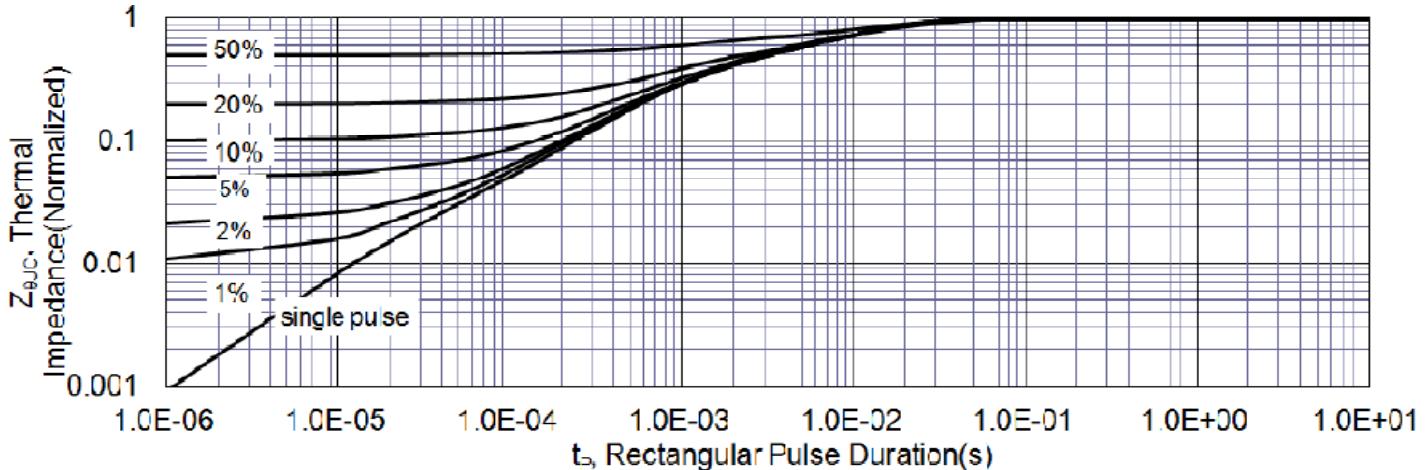


Figure 2. Maximum Power Dissipation vs Case Temperature

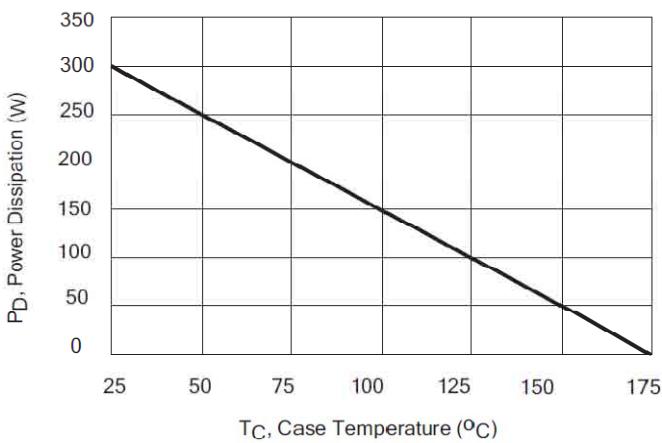


Figure 3. Maximum Continuous Drain Current vs Case Temperature

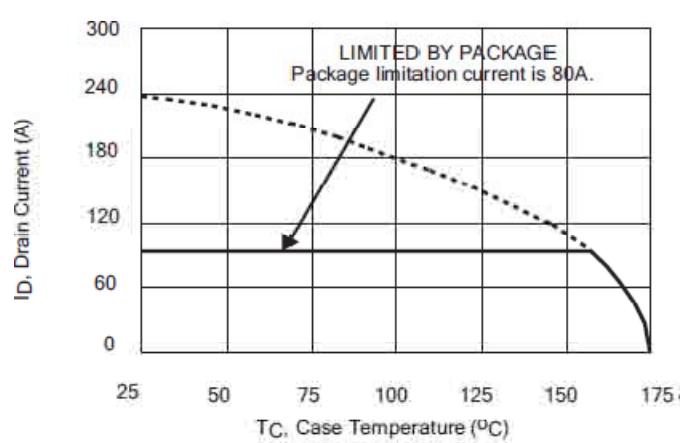


Figure 4. Typical Output Characteristics

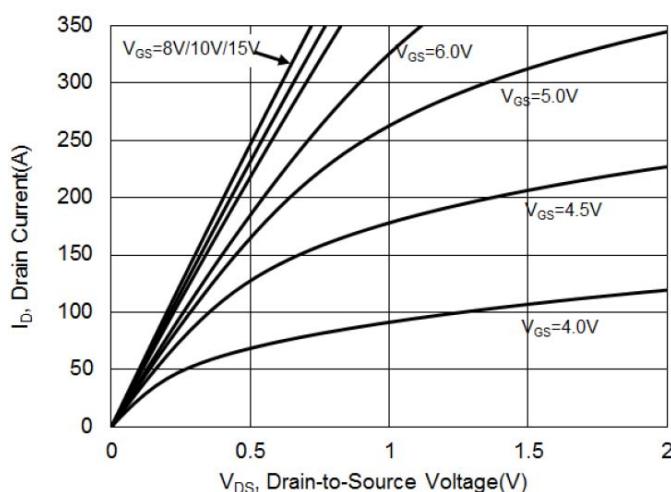
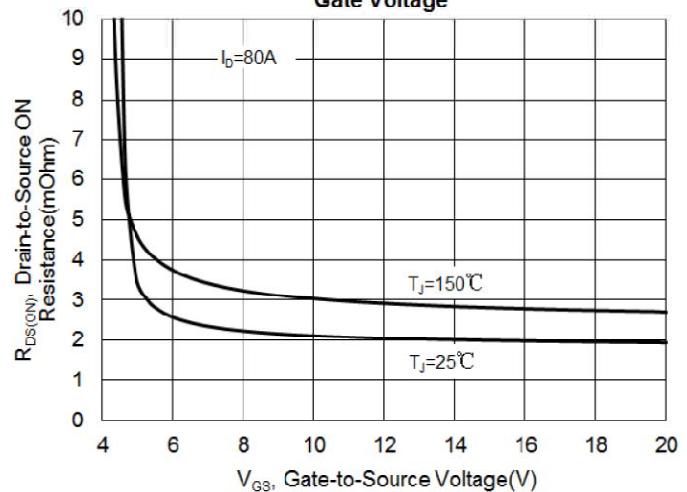
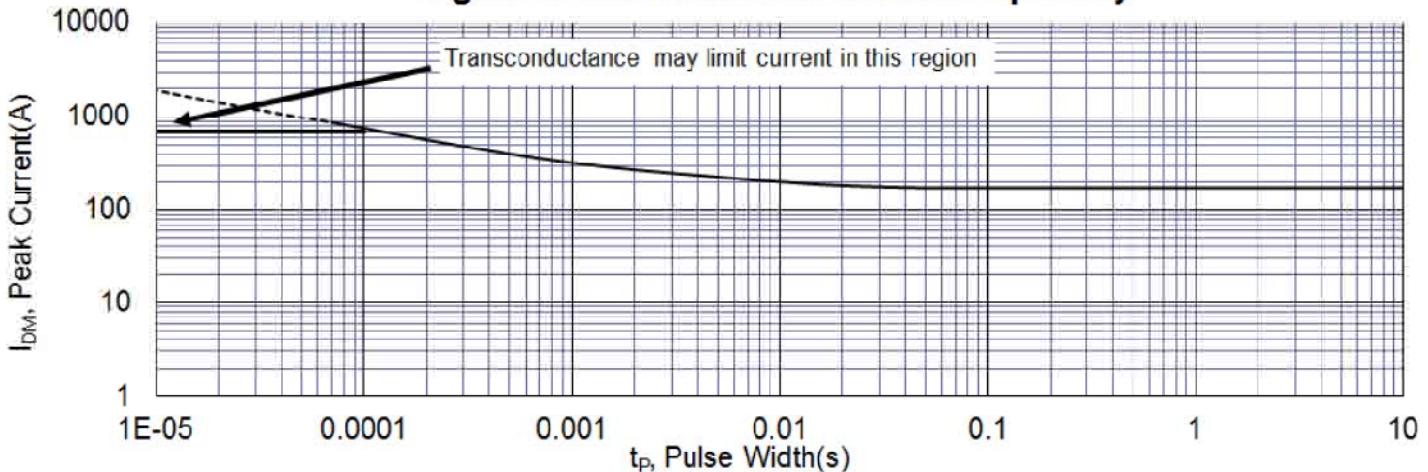
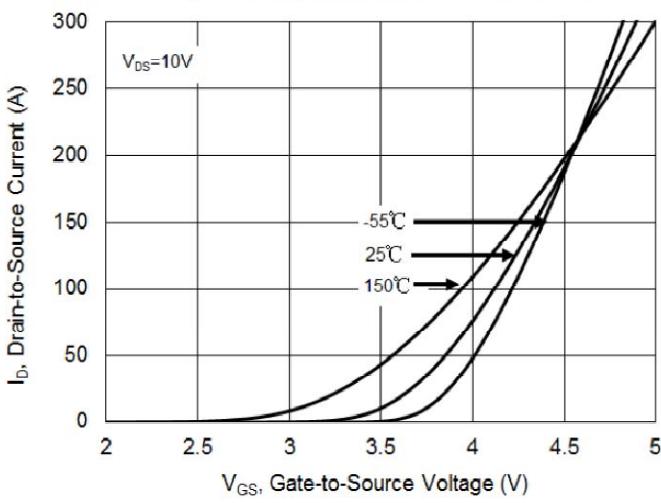
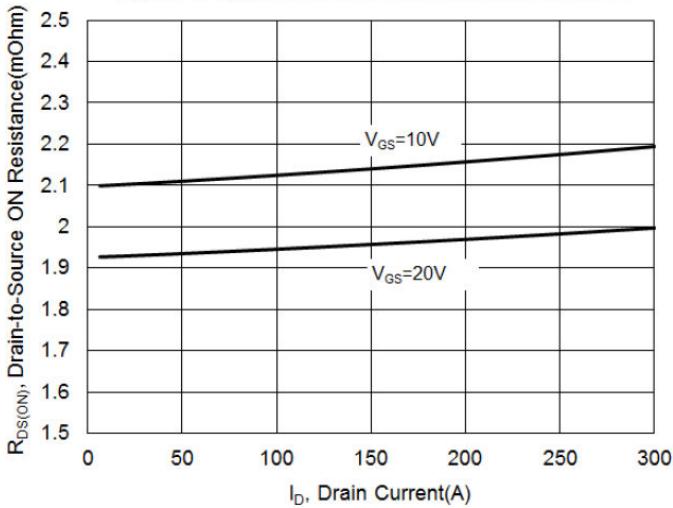
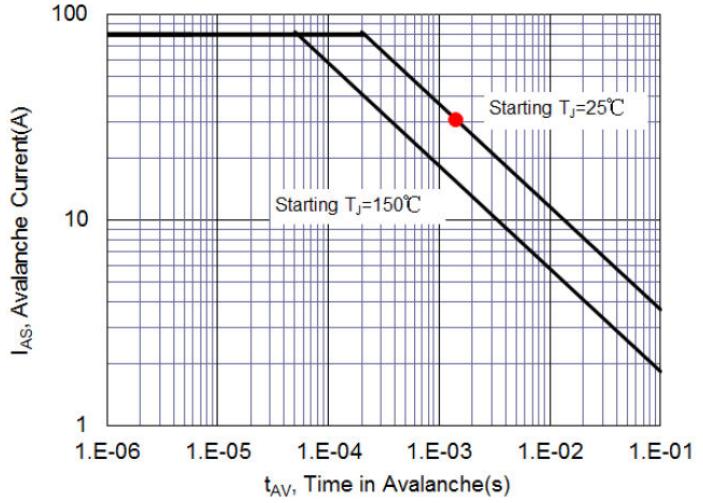
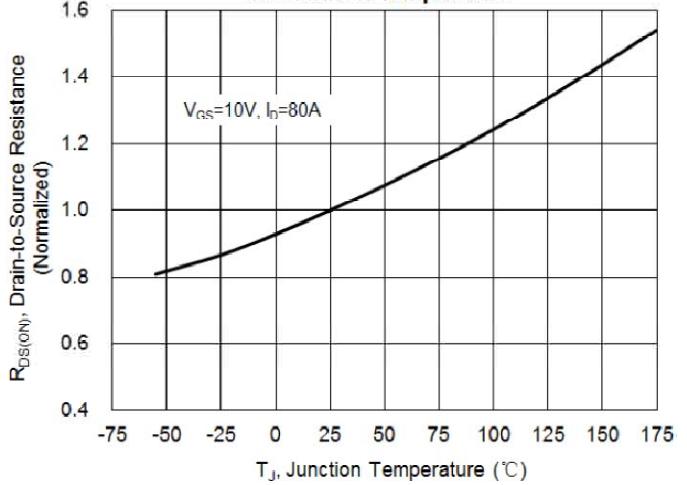


Figure 5. Typical Drain-to-Source ON Resistance vs. Gate Voltage



Typical Characteristics(Cont.)

Figure 6. Maximum Peak Current Capability**Figure 7. Typical Transfer Characteristics****Figure 9. Typical Drain-to-Source ON Resistance****Figure 8. Unclamped Inductive Switching Capability****Figure 10. Typical Drain-to-Source On Resistance vs. Junction Temperature**

Typical Characteristics(Cont.)

Figure 11. Typical Breakdown Voltage vs. Junction Temperature

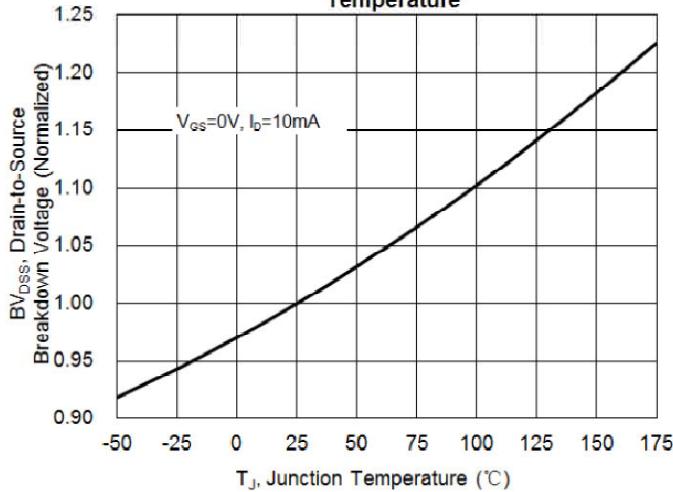


Figure 12. Typical Threshold Voltage vs. Junction Temperature

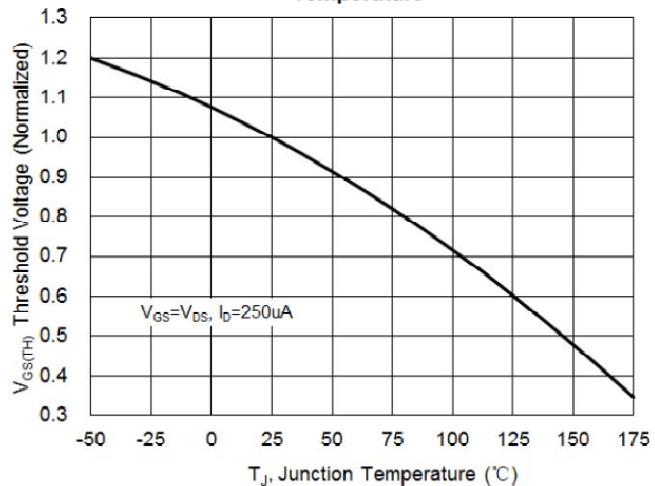


Figure 13. Maximum Forward Safe Operation Area

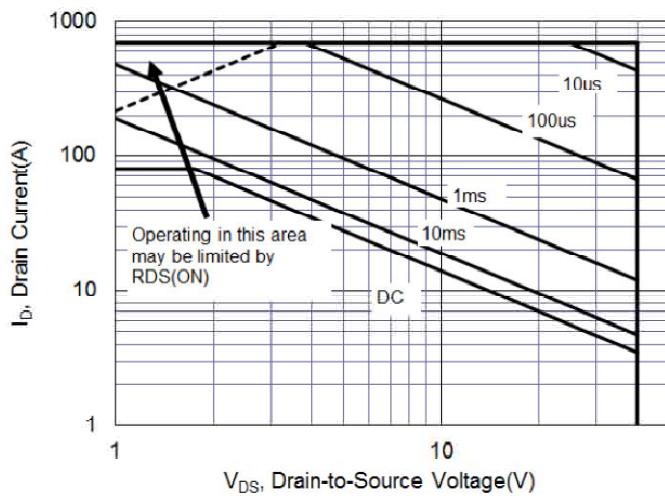


Figure 14. Typical Capacitance vs. Drain-to-Source Voltage

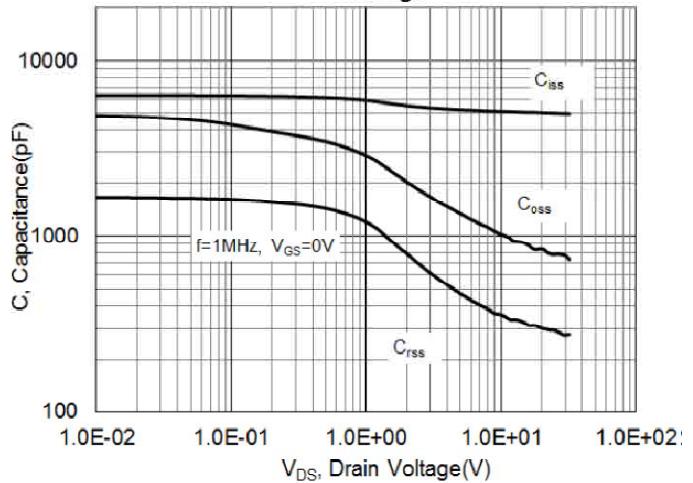


Figure 15. Typical Gate Charge vs. Gate-to-Source Voltage

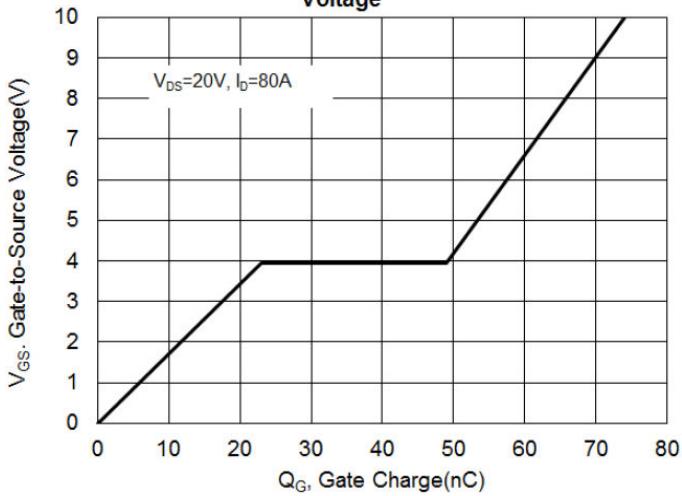
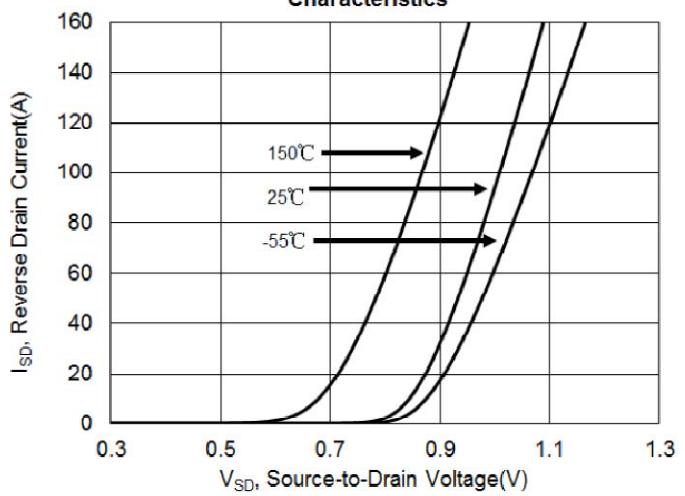


Figure 16. Typical Body Diode Transfer Characteristics



Test Circuits and Waveforms

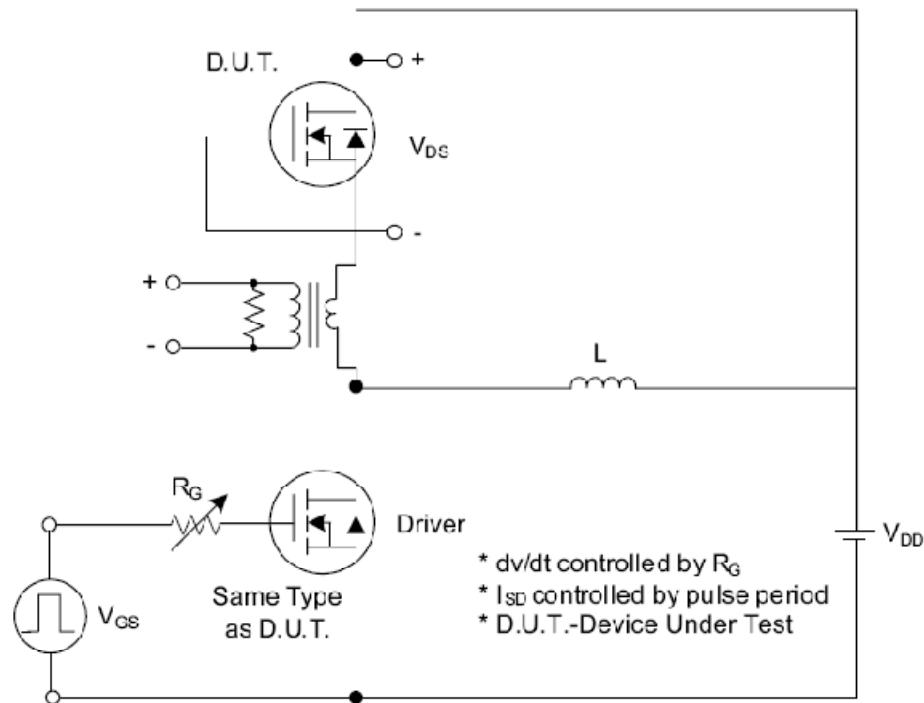


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

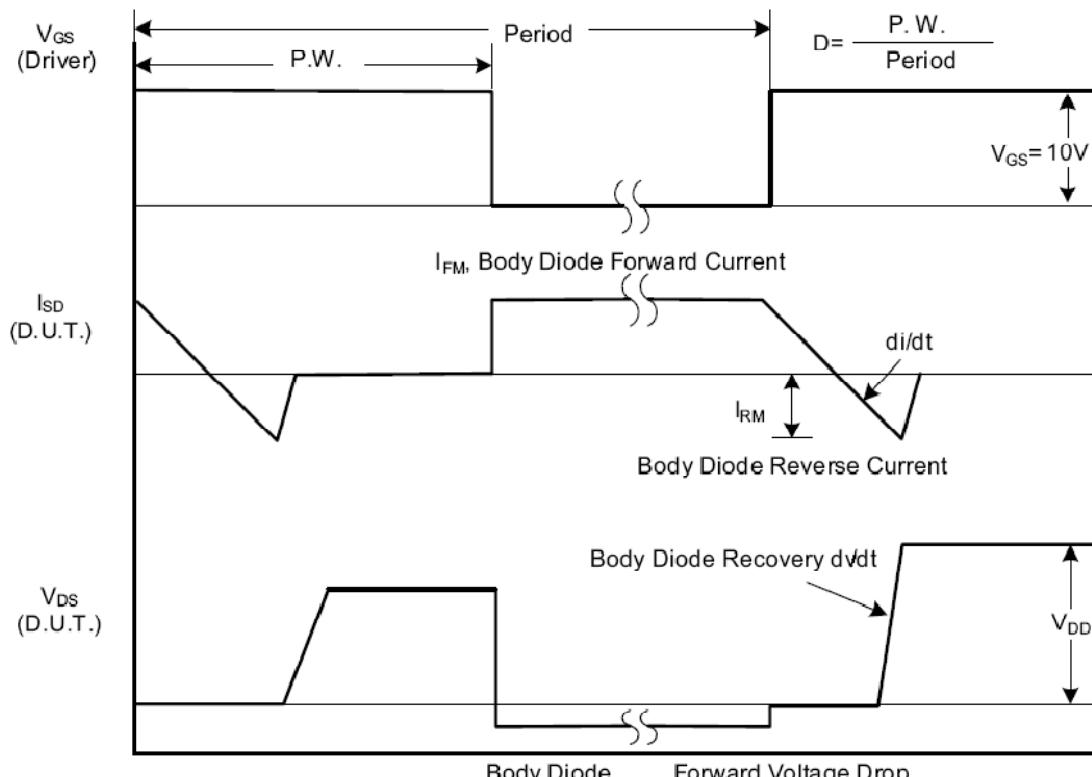


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

Test Circuits and Waveforms (Cont.)

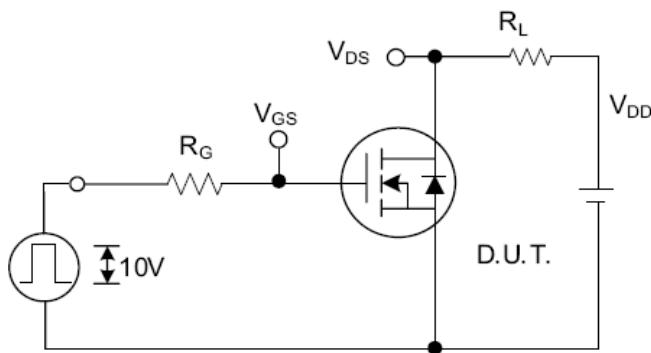


Fig. 2.1 Switching Test Circuit

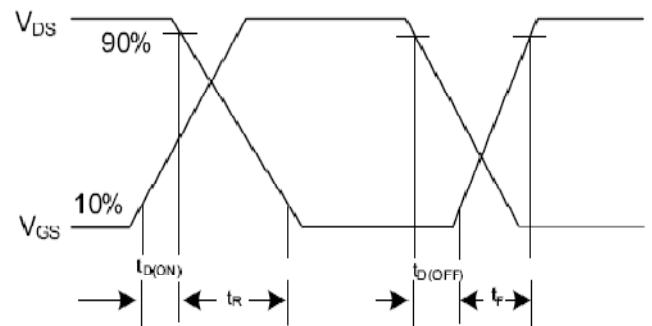


Fig. 2.2 Switching Waveforms

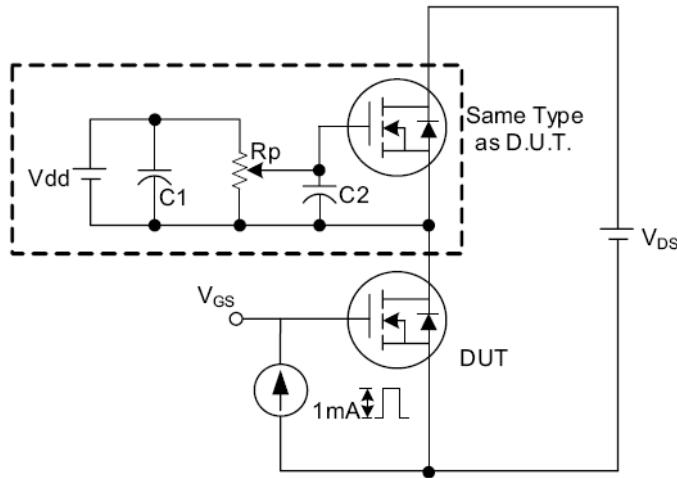


Fig. 3.1 Gate Charge Test Circuit

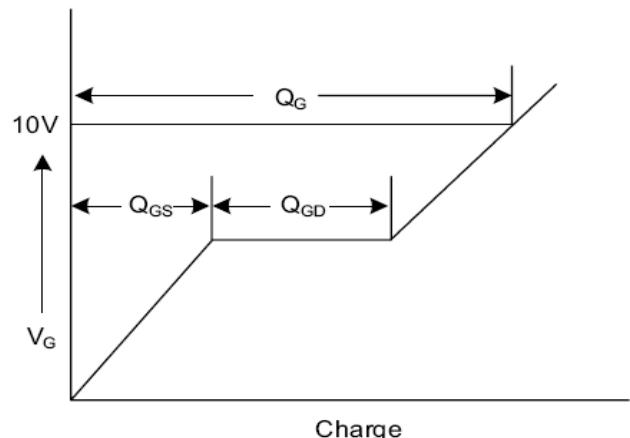


Fig. 3.2 Gate Charge Waveform

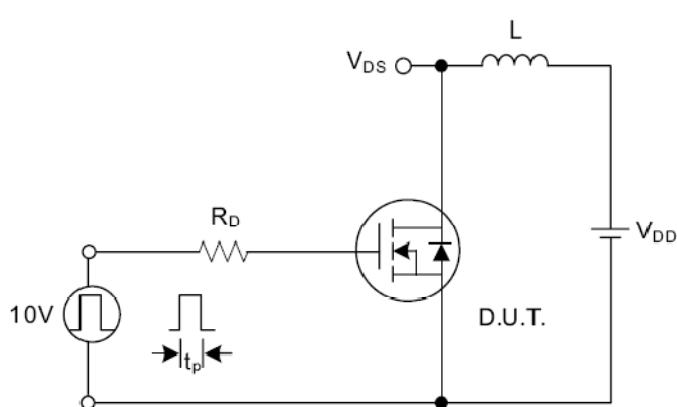


Fig. 4.1 Unclamped Inductive Switching Test Circuit

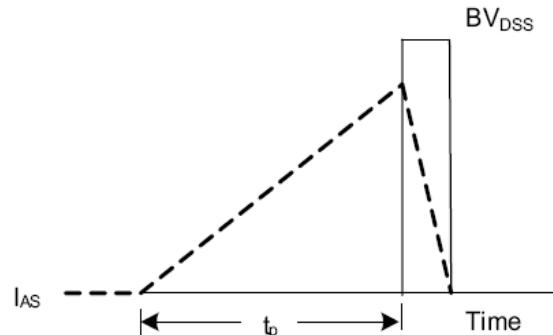


Fig. 4.2 Unclamped Inductive Switching Waveforms



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