HLK-TX510 Module Interface Pin Definitions							
NO.	Pin name	Default function	Type	Pull up and down	Power domain	Interface	
1	DPU_DPI_PCLK		I/O	NA	3.3V	DPU RGB Interface	DPUs can be configured as IOs if no RGB signals are used or if only MIPI signals are used, if DPUs are configured with RGB signals the remaining unused DPUs cannot be configured as IOs. The characteristics of the DPU interface are as follows: ● Programmable display resolutions (VGA, XGA, HD, Full HD) up to 1920x1080 with optional RGB to YUV/YBCCR conversion. ● Supports MIPI DPI-2 (Display Pixel Interface) parallel RGB ● Support for MIPI DBI (Display Bus Interface) Type B. ● Support for BT.656 (4:2:2 level digital component video signal interface in 525/625 line TV systems). ● Supports parallel YUV/YCbCr. ● Support for serial format 3-tap and 4-tap. ● Serial format biphasic 12-bit. ● Support for programmable HSYNC, VSYNC, DE, pixel clock polarity. ● Supports 3-4 wire SPI (Serial Peripheral Interface) bus. ● Support for DSPI and QSPI buses.
2	DPU_DPI_DE		I/O	NA	3.3V		
3	DPU_DPI_CM		I/O	NA	3.3V		
4	DPU_DPI_CSYNC		I/O	NA	3.3V		
5	DPU_DPI_D0		I/O	NA	3.3V		
6	DPU_DPI_D1		I/O	NA	3.3V		
7	DPU_DPI_D2		I/O	NA	3.3V		
8	DPU_DPI_D3		I/O	NA	3.3V		
9	DPU_DPI_D4		I/O	NA	3.3V		
10	DPU_DPI_D5		I/O	NA	3.3V		
11	DPU_DPI_D6		I/O	NA	3.3V		
12	DPU_DPI_D7		I/O	NA	3.3V		
13	DPU_DPI_D8		I/O	NA	3.3V		
14	DPU_DPI_D9		I/O	NA	3.3V		
15	DPU_DPI_D10		I/O	NA	3.3V		
16	DPU_DPI_D11		I/O	NA	3.3V		
17	DPU_DPI_D12		I/O	NA	3.3V		
18	DPU_DPI_D13		I/O	NA	3.3V		
19	DPU_DPI_D14		I/O	NA	3.3V		
20	DPU_DPI_D15		I/O	NA	3.3V		
21	DPU_DPI_D16		I/O	NA	3.3V		
22	DPU_DPI_D17		I/O	NA	3.3V		
23	DPU_DPI_D18		I/O	NA	3.3V		
24	DPU_DPI_D19		I/O	NA	3.3V		
25	DPU_DPI_D20		I/O	NA	3.3V		
26	DPU_DPI_D21		I/O	NA	3.3V		
27	DPU_DPI_D22		I/O	NA	3.3V		
28	DPU_DPI_D23		I/O	NA	3.3V		
29	CLK_24MHz_1		0	NA	3.3V	Synchronous clock output	
30	CK805_JTG_TCK		I/O	down	3.3V	CK805 JTAG Interface	
31	CK805_JTG_TMS		I/O	up	3.3V		
32	CK805_UART_RXD		I/O	NA	3.3V	CK805 UART Interface	
33	CK805_UART_TXD		I/O	NA	3.3V		
34	I2C3_SDA		I/O	up	3.3V	I2C Interface	

35	I2C3_SCL		I/O	up	3.3V		
36	USI1_SDO	USI1_UART_TXD	I/O	NA	3.3V	USI Interface	
37	USI1_SCLK	USI1_UART_RXD	I/O	NA	3.3V		
38	UART1_TXD		I/O	NA	3.3V	USI Interface	
39	UART1_RXD		I/O	NA	3.3V		
40	USI0_SDO	USI0_UART_TXD	I/O	NA	3.3V	USI Interface	
41	USI0_SCLK	USI0_UART_RXD	I/O	NA	3.3V		
42	PWM_CH0		I/O	NA	3.3V	PWM Interface	
43	PWM_CH2		I/O	NA	3.3V		
44	UART0_TXD		I/O	NA	3.3V	UART Interface	
45	UART0_RXD		I/O	NA	3.3V		
46	I2C0_SCL		I/O	up	1.8V	I2C Interface	Supports three IIC speeds: standard mode (0-100kb/s), fast mode (≤ 400kb/s) or fast mode plus (≤ 1000Kb/s), high speed mode (≤ 3.4mb/s).
47	I2C0_SDA		I/O	up	1.8V		
48	I2C1_SCL		I/O	up	1.8V		
49	I2C1_SDA		I/O	up	1.8V		
50	GND						
51	MIPI3_DATAP3		A	NA		MIPI TX Bus	1 MIPI3 is a TX transmit signal, supporting up to 2.5 Gbps per channel, supporting up to four D-PHY data channels
52	MIPI3_DATAN3		A	NA			
53	MIPI3_DATAP0		A	NA			
54	MIPI3_DATAN0		A	NA			
55	MIPI3_CLKP		A	NA			
56	MIPI3_CLKN		A	NA			
57	MIPI3_DATAP1		A	NA			
58	MIPI3_DATAN1		A	NA			
59	MIPI3_DATAP2		A	NA			
60	MIPI3_DATAN2		A	NA			
61	GND						
62	VBUS_HOST		A	NA		USB Interface	USB2.0 supports LS 1.5-Mbps/FS 12-Mbps/HS 480- Mbps.
63	DRVVBUS		O	NA	3.3V		
64	USB_ID		A	NA			
65	DM0		A	NA			
66	DP0		A	NA			
67	ADC_CH1		A	NA		ADC Interface	ADC module 12-bit resolution, 5MS/s sampling rate, 0~1.8V acquisition voltage range.
68	ADC_CH2		A	NA			
69	MIPI2_DATAP1		A	NA		MIPI RX Bus	
70	MIPI2_DATAN1		A	NA			
71	MIPI2_CLKP		A	NA			
72	MIPI2_CLKN		A	NA			
73	MIPI2_DATAP0		A	NA			

74	MIPI2_DATAN0		A	NA			
75	GND						
76	MIPI1_DATAP1		A	NA		MIPI RX Bus	
77	MIPI1_DATAN1		A	NA			
78	MIPI1_CLKP		A	NA			
79	MIPI1_CLKN		A	NA			
80	MIPI1_DATAP0		A	NA			
81	MIPI1_DATAN0		A	NA			
82	GND						
83	MIPI0_DATAP1		A	NA			
84	MIPI0_DATAN1		A	NA			
85	MIPI0_CLKP		A	NA		MIPI RX Bus	
86	MIPI0_CLKN		A	NA			
87	MIPI0_DATAP0		A	NA			
88	MIPI0_DATAN0		A	NA			
89	GND						
90	CLK_24MHz_3		O	NA	3.3V	Synchronous clock output	
91	GND						
92	AOGPIO11		I/O	NA	1.8V		
93	AOGPIO0		I/O	NA	1.8V		
94	AOGPIO1		I/O	NA	1.8V		
95	AOGPIO4		I/O	NA	1.8V		
96	AOGPIO5		I/O	NA	1.8V	AOGPIO Interface	
97	AOGPIO7		I/O	NA	1.8V		
98	AOGPIO9		I/O	NA	1.8V		
99	AOGPIO2		I/O	NA	1.8V		
100	AOGPIO3		I/O	NA	1.8V		
101	AOGPIO8		I/O	NA	1.8V		
102	GND						
103	1V8_VDD_VOUT		P			1.8VPower output	
104	VDD_5V0		P			5V Power input	
105	VDD_5V0		P				
106	GND						
107	JTAG_NRST		I	NA	1.8V	Module hardware reset	
108	CK804_JTG_TMS		I/O	up	3.3V	CK804 JTAG Interface	
109	CK804_JTG_TCK		I/O	down	3.3V		
110	DPU_DPI_SD		I/O	NA	3.3V	DPU RGB	
111	DPU_DPI_HSYNC		I/O	NA	3.3V		

The 3-way MIPI [0,1,2] is the RX receive signal and operates at speeds from 80 Mbps to 2.5 Gbps, with a total throughput of up to 5 Gbps for each of the two data channels, supporting a maximum of 10 Mbps LP data rate.

The AOGPIO pin cannot be used as an interrupt (high level normal, low level interrupt) but can be used as a wake-up (high level wake-up, low level normal) and all IOs except AOGPIO can be used as interrupts.

112	DPU_DPI_VSYNC		I/O	NA	3.3V		

Description: Type: I = input, O = output, I/O = input/output (bidirectional), A = analogue, P = power

NA-Indicates an indeterminate state, if a determinate state is required, an external pull-down resistor can be used.
UP/DOWN-Indicates an internal pull-up/pull-down resistor.

103	1V8_VDD_VOUT		P			1.8VPower output	
104	VDD_5V0		P			5V Power input	
105	VDD_5V0		P				
50	GND						
61	GND						
75	GND						
82	GND						
89	GND						
91	GND						
102	GND						
106	GND						
1	DPU_DPI_PCLK		I/O	NA	3.3V	DPU RGB Interface	DPUs can be configured as IOs if no RGB signals are used or if only MIPI signals are used, if DPUs are configured with RGB signals the remaining unused DPUs cannot be configured as IOs. The DPU interface has the following characteristics: ● Programmable display resolution (VGA, XGA, HD, Full HD) up to 1920x1080, with optional RGB to YUV/YBCCR conversion. ● Support for MIPI DPI-2 (Display Pixel Interface) parallel RGB. ● Support for MIPI DBI (Display Bus Interface) Type B. ● Support for BT.656 (4:2:2 level digital component video signal interface in 525/625 line TV systems). ● Supports parallel YUV/YCbCr. ● Support for serial format 3-tap and 4-tap. ● Serial format bi-phase 12-bit.
2	DPU_DPI_DE		I/O	NA	3.3V		
3	DPU_DPI_CM		I/O	NA	3.3V		
4	DPU_DPI_CSYNC		I/O	NA	3.3V		
5	DPU_DPI_D0		I/O	NA	3.3V		
6	DPU_DPI_D1		I/O	NA	3.3V		
7	DPU_DPI_D2		I/O	NA	3.3V		
8	DPU_DPI_D3		I/O	NA	3.3V		
9	DPU_DPI_D4		I/O	NA	3.3V		
10	DPU_DPI_D5		I/O	NA	3.3V		
11	DPU_DPI_D6		I/O	NA	3.3V		
12	DPU_DPI_D7		I/O	NA	3.3V		
13	DPU_DPI_D8		I/O	NA	3.3V		
14	DPU_DPI_D9		I/O	NA	3.3V		
15	DPU_DPI_D10		I/O	NA	3.3V		
16	DPU_DPI_D11		I/O	NA	3.3V		
17	DPU_DPI_D12		I/O	NA	3.3V		
18	DPU_DPI_D13		I/O	NA	3.3V		
19	DPU_DPI_D14		I/O	NA	3.3V		
20	DPU_DPI_D15		I/O	NA	3.3V		
21	DPU_DPI_D16		I/O	NA	3.3V		
22	DPU_DPI_D17		I/O	NA	3.3V		
23	DPU_DPI_D18		I/O	NA	3.3V		
24	DPU_DPI_D19		I/O	NA	3.3V		
25	DPU_DPI_D20		I/O	NA	3.3V		

26	DPU_DPI_D21		I/O	NA	3.3V		● Support for programmable HSYNC, VSYNC, DE, pixel clock polarity. ● Support for 3-4 wire SPI (Serial Peripheral Interface) bus.
27	DPU_DPI_D22		I/O	NA	3.3V		
28	DPU_DPI_D23		I/O	NA	3.3V		
110	DPU_DPI_SD		I/O	NA	3.3V		
111	DPU_DPI_HSYNC		I/O	NA	3.3V		
112	DPU_DPI_VSYNC		I/O	NA	3.3V		
51	MIPI3_DATAP3		A	NA		MIPI TX 总线	1 MIPI3 is a TX transmit signal, supporting up to 2.5 Gbps per channel, supporting up to four D-PHY data channels
52	MIPI3_DATAN3		A	NA			
53	MIPI3_DATAP0		A	NA			
54	MIPI3_DATAN0		A	NA			
55	MIPI3_CLKP		A	NA			
56	MIPI3_CLKN		A	NA			
57	MIPI3_DATAP1		A	NA			
58	MIPI3_DATAN1		A	NA			
59	MIPI3_DATAP2		A	NA			
60	MIPI3_DATAN2		A	NA			
69	MIPI2_DATAP1		A	NA		MIPI RX Bus	The 3-way MIPI [0,1,2] is an RX receive signal that operates at speeds from 80 Mbps to 2.5 Gbps, with a total throughput of up to 5 Gbps for each of the two data channels, and supports a maximum LP data rate of 10 Mbps.
70	MIPI2_DATAN1		A	NA			
71	MIPI2_CLKP		A	NA			
72	MIPI2_CLKN		A	NA			
73	MIPI2_DATAP0		A	NA			
74	MIPI2_DATAN0		A	NA			
76	MIPI1_DATAP1		A	NA		MIPI RX Bus	
77	MIPI1_DATAN1		A	NA			
78	MIPI1_CLKP		A	NA			
79	MIPI1_CLKN		A	NA			
80	MIPI1_DATAP0		A	NA			
81	MIPI1_DATAN0		A	NA			
83	MIPI0_DATAP1		A	NA		MIPI RX Bus	
84	MIPI0_DATAN1		A	NA			
85	MIPI0_CLKP		A	NA			
86	MIPI0_CLKN		A	NA			
87	MIPI0_DATAP0		A	NA			
88	MIPI0_DATAN0		A	NA			
92	AOGPIO11		I/O	NA	1.8V	AOGPIO Interface	The AOGPIO pin cannot be used as an interrupt (high level normal, low level interrupt), but can be used as a wakeup (high level wakeup, low level normal), and all IOs except AOGPIO can be used as interrupts.
93	AOGPIO0		I/O	NA	1.8V		
94	AOGPIO1		I/O	NA	1.8V		
95	AOGPIO4		I/O	NA	1.8V		
96	AOGPIO5		I/O	NA	1.8V		
97	AOGPIO7		I/O	NA	1.8V		
98	AOGPIO9		I/O	NA	1.8V		

99	AOGPIO2		I/O	NA	1.8V		
100	AOGPIO3		I/O	NA	1.8V		
101	AOGPIO8		I/O	NA	1.8V		
46	I2C0_SCL		I/O	up	1.8V	I2C Interface	Support IIC three speeds: standard mode (0-100kb/s), Fast mode (≤400kb/s) or fast mode plus (≤1000Kb/s), high speed mode (≤3.4mb/s).
47	I2C0_SDA		I/O	up	1.8V		
48	I2C1_SCL		I/O	up	1.8V		
49	I2C1_SDA		I/O	up	1.8V		
34	I2C3_SDA		I/O	up	3.3V		
35	I2C3_SCL		I/O	up	3.3V		
107	JTAG_NRST		I	NA	1.8V	Module hardware reset	
108	CK804_JTG_TMS		I/O	up	3.3V	CK804 JTAG Interface	
109	CK804_JTG_TCK		I/O	down	3.3V		
30	CK805_JTG_TCK		I/O	down	3.3V	CK805 JTAG Interface	
31	CK805_JTG_TMS		I/O	up	3.3V		
32	CK805_UART_RXD		I/O	NA	3.3V	CK805 UART Interface	
33	CK805_UART_TXD		I/O	NA	3.3V		
38	UART1_TXD		I/O	NA	3.3V	UART Interface	
39	UART1_RXD		I/O	NA	3.3V		
44	UART0_TXD		I/O	NA	3.3V		
45	UART0_RXD		I/O	NA	3.3V		
40	USI0_SDO	USI0_UART_TXD	I/O	NA	3.3V	USI Interface	
41	USI0_SCLK	USI0_UART_RXD	I/O	NA	3.3V		
36	USI1_SDO	USI1_UART_TXD	I/O	NA	3.3V		
37	USI1_SCLK	USI1_UART_RXD	I/O	NA	3.3V		
42	PWM_CH0		I/O	NA	3.3V	PWM Interface	
43	PWM_CH2		I/O	NA	3.3V		
62	VBUS_HOST		A	NA		USB Interface	USB2.0 supports LS 1.5-Mbps/FS 12-Mbps/HS 480- Mbps.
63	DRVVBUS		O	NA	3.3V		
64	USB_ID		A	NA			
65	DM0		A	NA			
66	DP0		A	NA			
67	ADC_CH1		A	NA		ADC Interface	ADC module 12-bit resolution, 5MS/s sampling rate, 0~1.8V acquisition voltage range.
68	ADC_CH2		A	NA			
29	CLK_24MHz_1		O	NA	3.3V	Synchronous clock output	
90	CLK_24MHz_3		O	NA	3.3V		