Counter

Asynchronus / Ripple

Clocks are not simultaneously given

- UP counter
- Down counter
- UP-Down counter

Synchronus counter

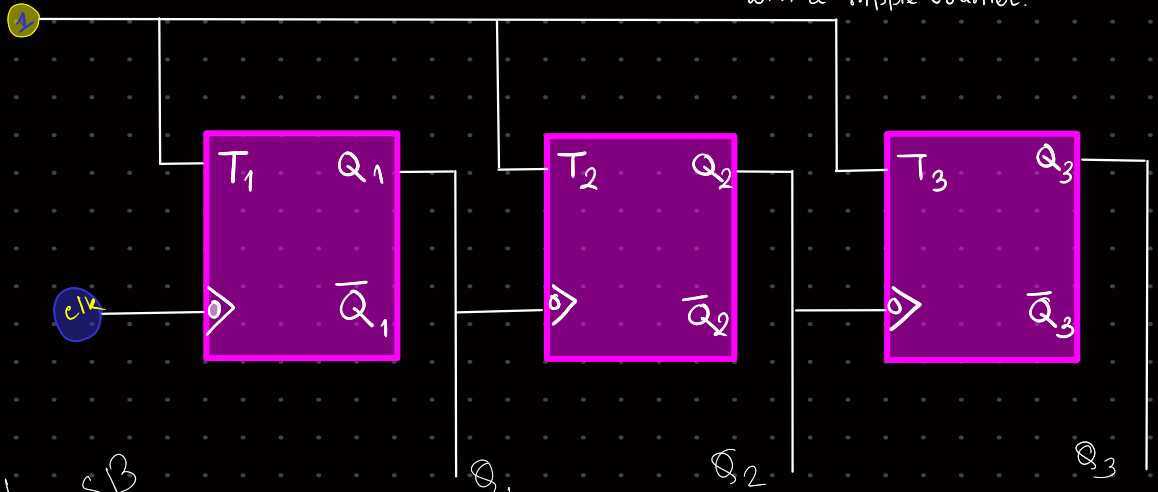
Clocks are simultaneously given.

- **Advantages of Synchronus counter.**

i) each ff has a delay time, In the ripple counter these delay times are additive. So the total "settling" time for the counter is approximately the delay time times the total no. of F.F.

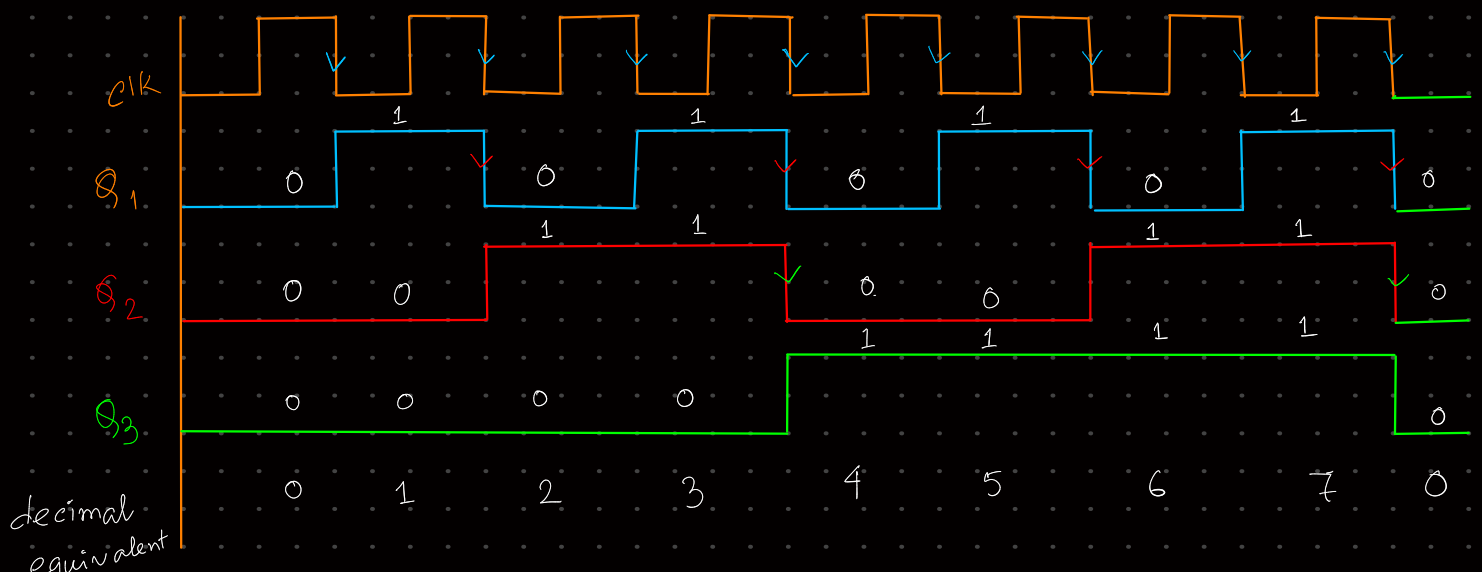
ii) There is the possibility of glitches ocurring at the output of decoding gates used with a ripple counter.

- **Asynchronus counter:**
- **3-bit up counter**

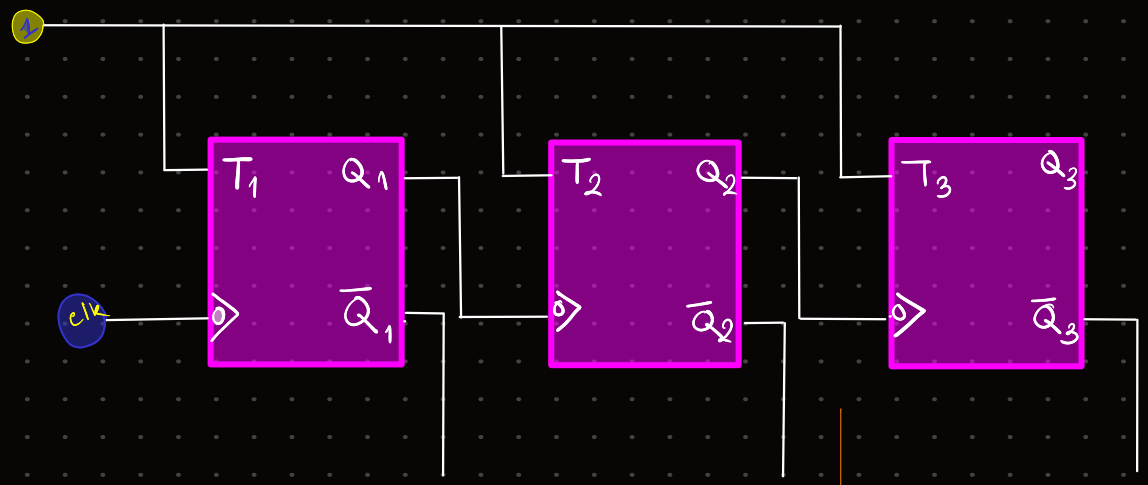


MSB $Q_3 Q_2 Q_1$ LSB

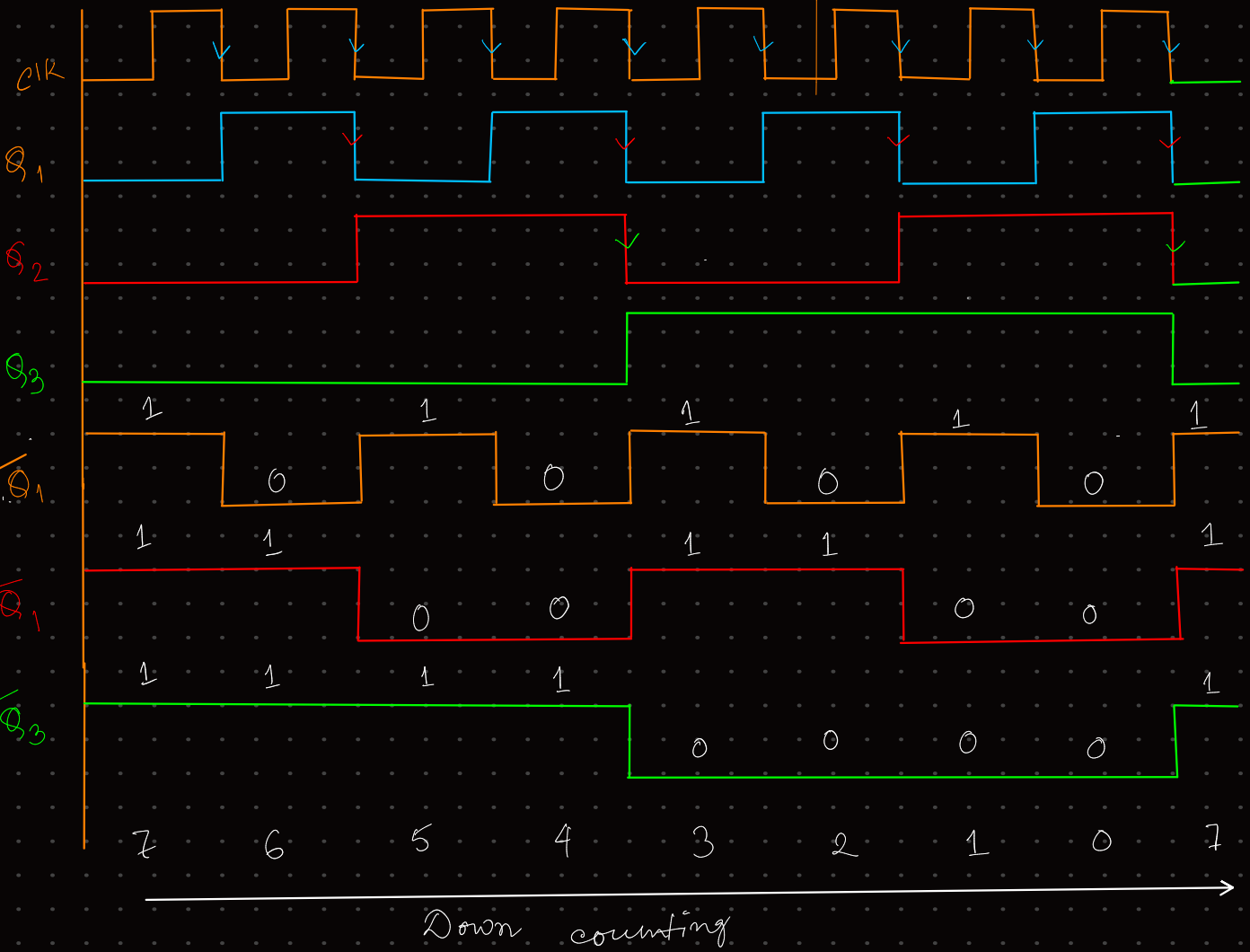
- every clock pulse the OUT will toggle (T ff so used)



3-bit down counter

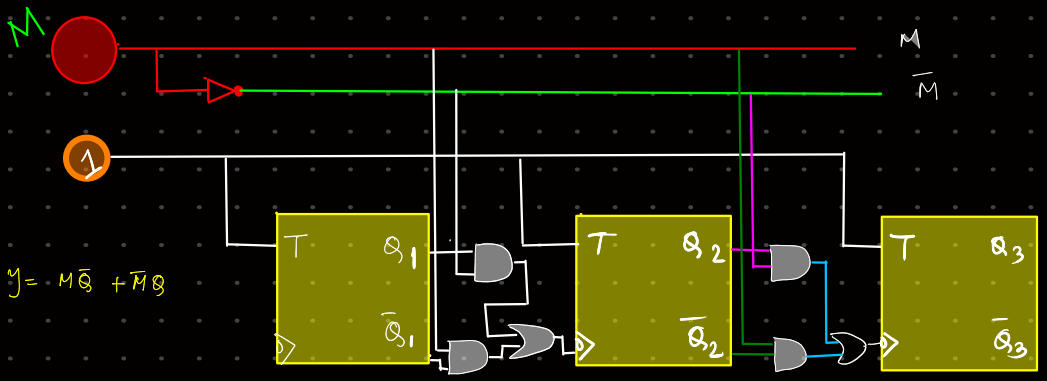


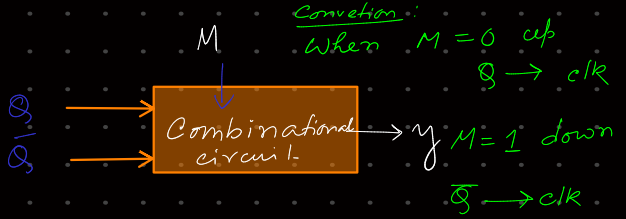
- Q's are high
- Q̄ are low.



- There are several circuit available for up and down counting.

3-bit up-down ripple counter



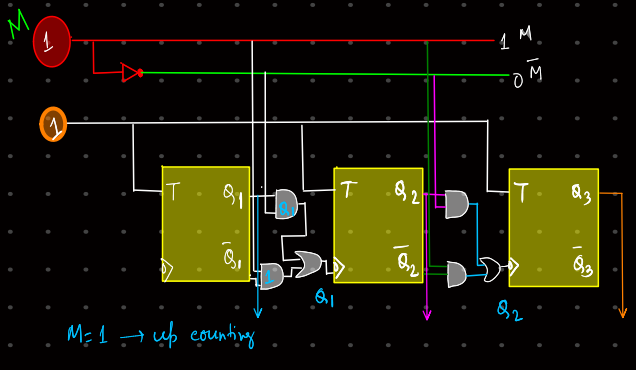


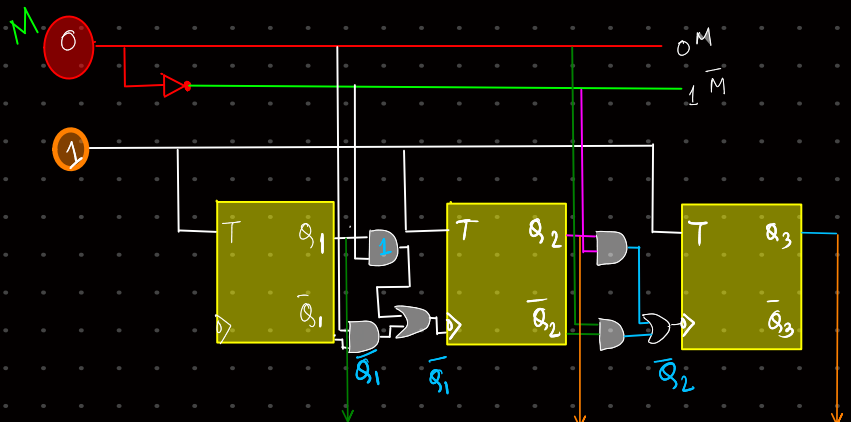
A mode control i/p

M	Q	$\bar{Q}$	y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

M \ Q$\bar{Q}$	00	01	11	10
0	0	0	1	1
1	0	1	1	0

$y = M\bar{Q} + \bar{M}Q = M \oplus Q$



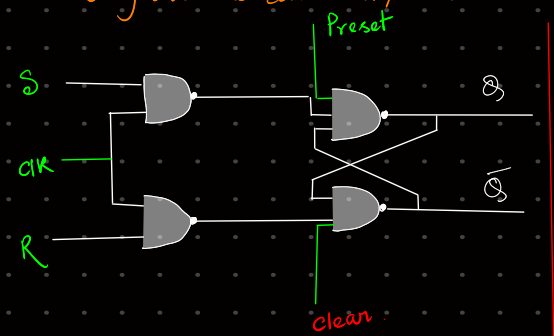


Modulus of a counter — counting upto a particular value

- 2 bit ripple counter → Mod-4
- 3 bit ripple counter → Mod-8.

- **Important concept:** Set & Reset

• They are the direct inputs or overridding input.

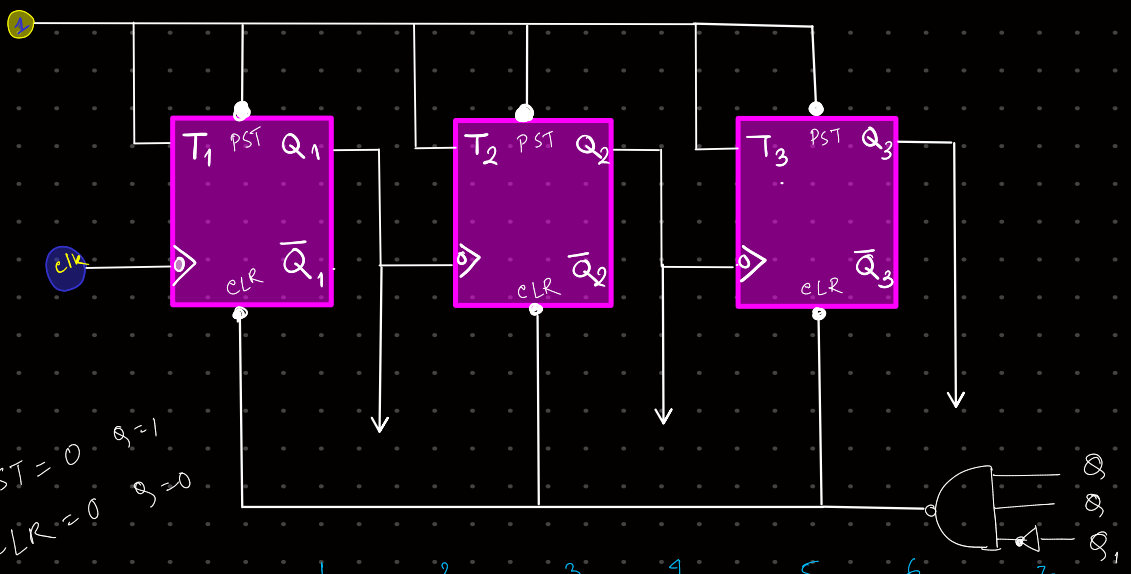


• When preset is 0, Q is always 1.
When clear is 0, $\bar{Q}$ is always 1 ie, Q = 0

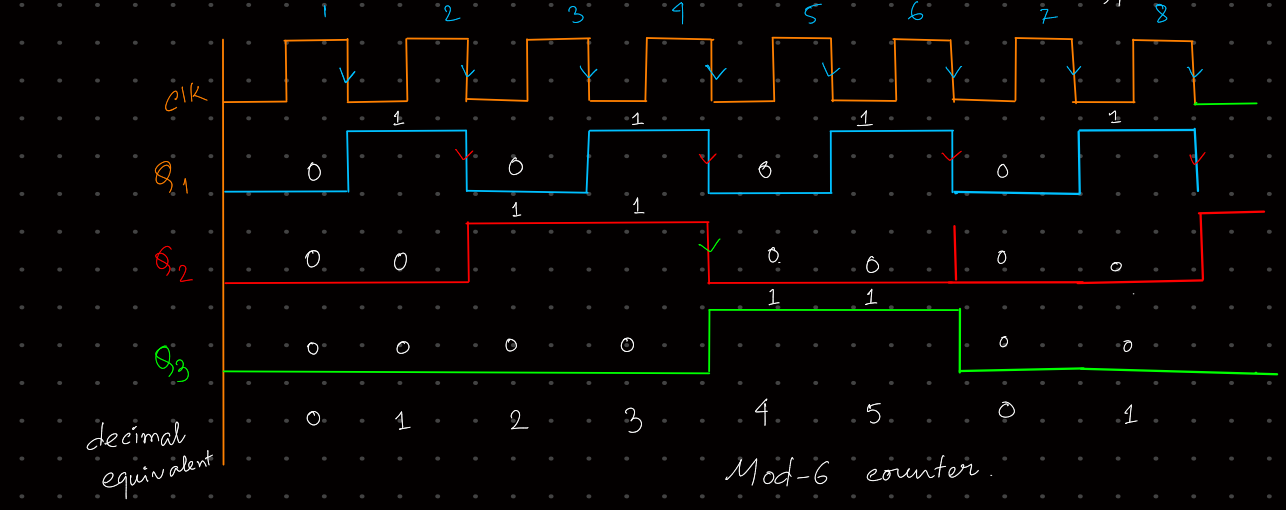
Preset	Clear	Q_n
0	0	Not used
0	1	1
1	0	0
1	1	No chan

They are active low signal!
SET ← 0
Reset ← 1
FF will perform normaly

- Now we want to creat MOD-6 counter ie, 0-5 count



Q_3	Q_2	Q_1	
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6 X
1	1	1	7 X

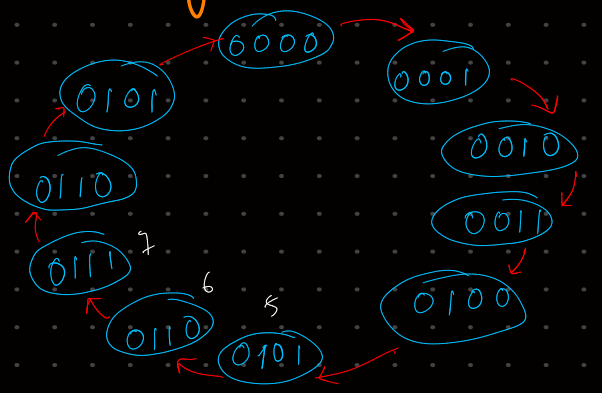


Mod-6 counter.

• Decade (BCD) counter

0 → 9 can be used in 7 segment display!

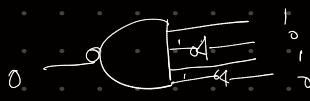
• State diagram :-



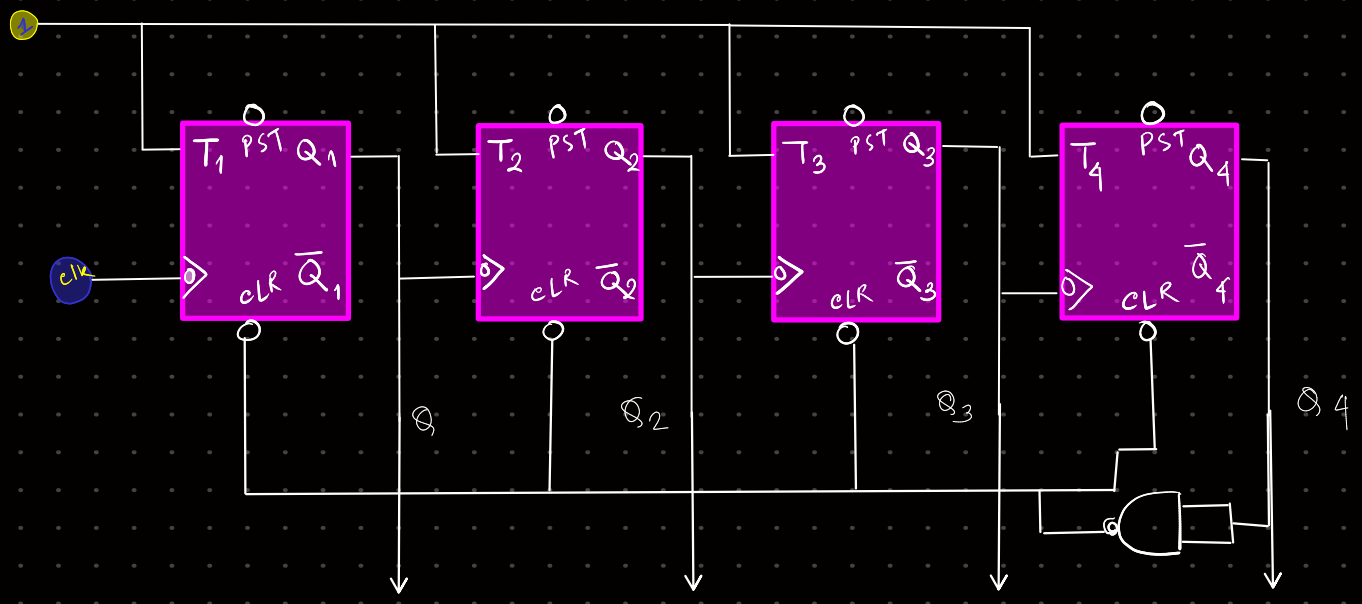
CLK	Q_4	Q_3	Q_2	Q_1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	0	1	1	0
9	0	1	0	1
10	1	0	1	0

How.

0 0 0 0



↓ do we really need that.



Synchronus counter

How to design Synchronus counter

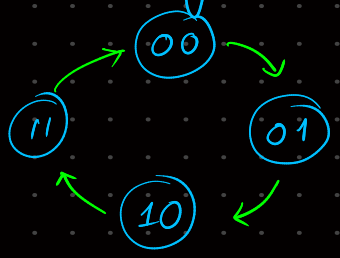
1. Decide the no. of F.F.
2. Excitation table of F.F.
3. State diagram and circuit excitation table.
4. Obtaine the simplified eqn using K-Map.
5. Draw the logic diagram.

- Design 2-bit synchronus up counter.

- T-FF excitation table.

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	0
1	1	1

- State diagram :-



- Ckt excitation tab:

Q_1	Q_2	Q_1^*	Q_2^*	T_1	T_2
0	0	0	1	0	1
0	1	1	0	1	0
1	0	1	1	0	1
1	1	0	0	1	0

- For T_1

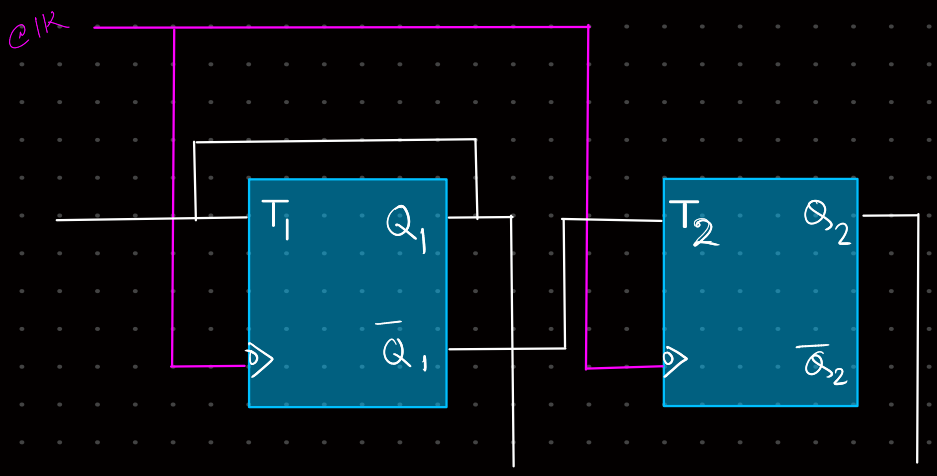
Q_2 \ Q_1	0	1
0	0	1
1	0	1

$T_1 = Q_1$

- For T_2

Q_2 \ Q_1	0	1
0	1	0
1	1	0

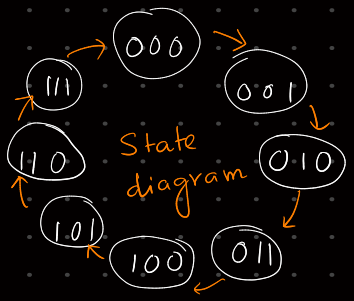
$T_2 = \bar{Q}_1$



3 bit synchronous up counter

Exitation:

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0



Ckt exitation tab:

Present state			Next state					
Q_C	Q_B	Q_A	Q_C^*	Q_B^*	Q_A^*	T_C	T_B	T_A
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

for T_C

Q_C \ Q_BQ_A	00	01	11	10
0	0	0	1	0
1	0	0	1	0

$T_C = Q_AQ_B$

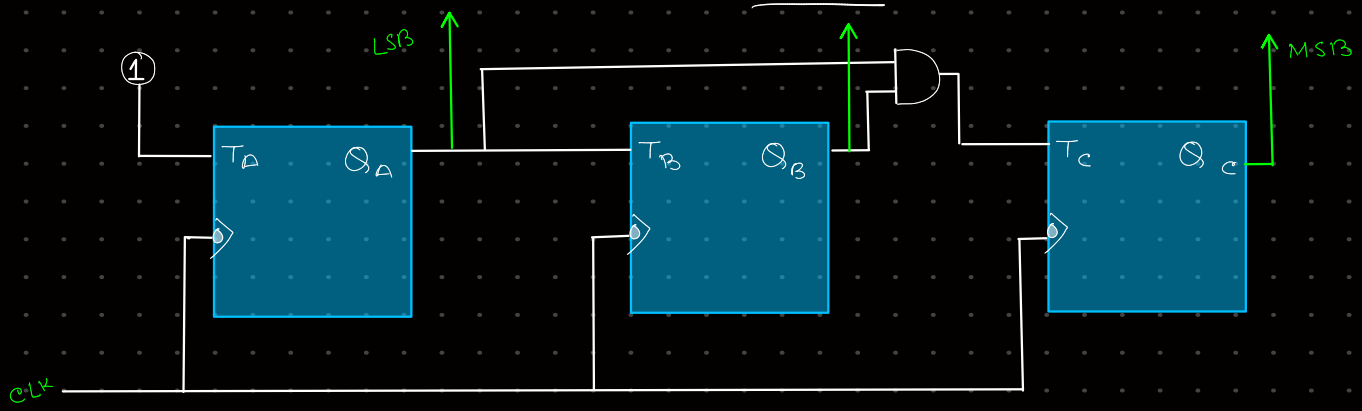
For T_B

Q_C \ Q_BQ_A	00	01	11	10
0	0	1	1	0
1	0	1	1	0

$T_B = Q_A$

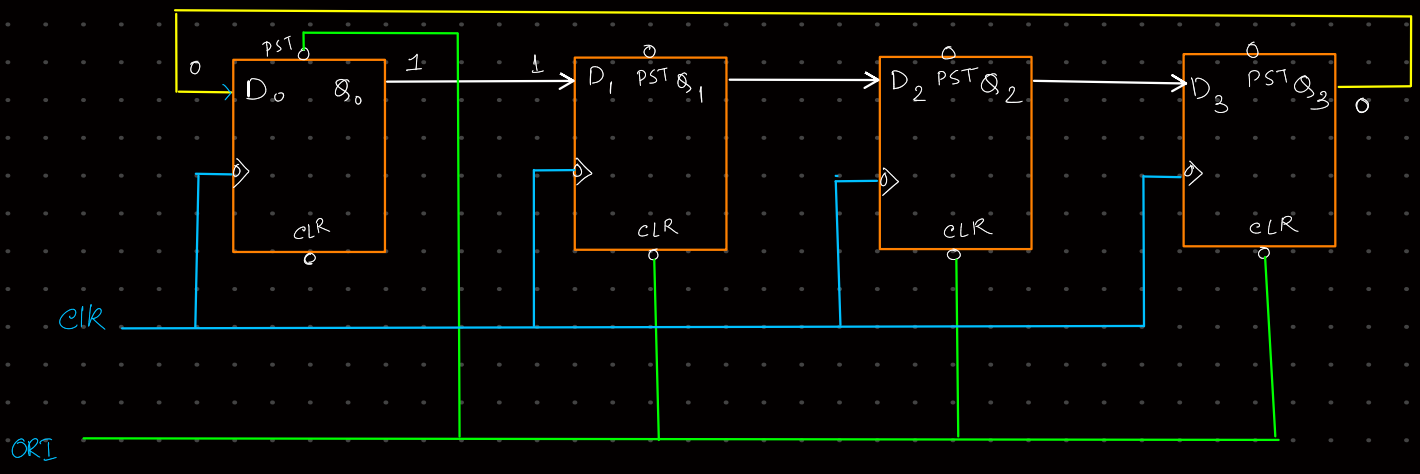
Q_C \ Q_BQ_A	00	01	11	10
0	1	1	1	1
1	1	1	1	1

$T_A = 1$



Ring Counter

- Ring counter is a typical application of "shift Register".
- The only change is the output of last F.F. is connected to the input of first F.F.
- no. of state = no of F.F used



PST = 0 → Q = 1
CLR = 0 → Q = 0

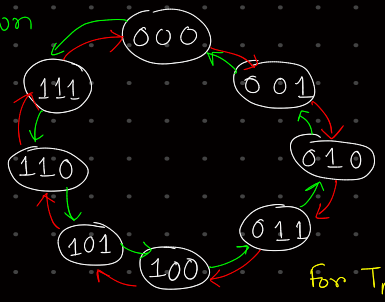
ORI	CLK	Q_0	Q_1	Q_2	Q_3
⊓	X	1	0	0	0
1	↓				
1	↓				
1	↓				
1	↓				

3-bit UP/DOWN Synchronous counter

- M=0 up counting
- M=1 down counting

M	Q_C Q_B Q_A	Q_C^* Q_B^* Q_A^*	T_C T_B T_A
0	0 0 0	0 0 1	0 0 1
0	0 0 1	0 1 0	0 1 1
0	0 1 0	0 1 1	0 0 1
0	0 1 1	1 0 0	1 1 1
0	1 0 0	1 0 1	0 0 1
0	1 0 1	1 1 0	0 1 1
0	1 1 0	1 1 1	0 0 1
0	1 1 1	0 0 0	1 1 1
1	0 0 0	1 1 1	1 1 1
1	0 0 1	0 0 0	0 0 1
1	0 1 0	0 0 1	0 1 1
1	0 1 1	0 1 0	0 0 1
1	1 0 0	0 1 1	1 1 1
1	1 0 1	1 0 0	0 0 1
1	1 1 0	1 0 1	0 1 1
1	1 1 1	1 1 0	0 0 1

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0



for T_B

MQ_C \ Q_BQ_A	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	1	0	0	1
10	1	0	0	1

$T_B = \bar{M} Q_A + M \bar{Q}_A$

$= M \oplus Q_A$

MQ_C \ Q_BQ_A	00	01	11	10
00			1	
01			1	
11	1			
10	1			

$T_A = 1$

for T_C

MQ_C \ Q_BQ_A	00	01	11	10
00	0	0	1	0
01	0	0	1	0
11	1	0	0	0
10	1	0	0	0

$T_C = \bar{M} Q_A Q_B$