

Brac University

Department of Electrical & Electronic Engineering

Semester 25

EEE205L

Electronic Circuits I Laboratory

Section: 01



Project Report

Name of the experiment : *Observation of a load resistor on the gain of an BJT for both with and without the impact of a bypass capacitor.*

Prepared by:

Group Number: 01

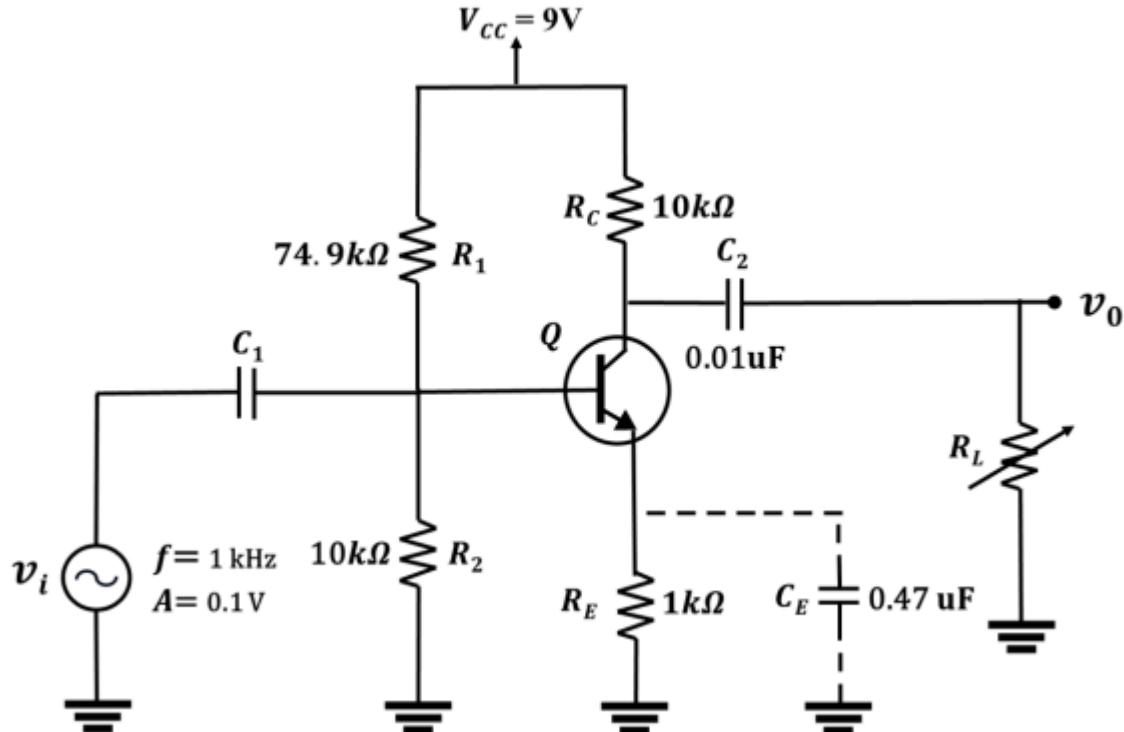
Group members:

Sl.	Name	ID	Contribution
1.	Muhammad Mushfiqur Rahman	24121058	Hardware, Calculation, and Report
2.	Tashin Ahmed Sakib	24121076	Software Part
3.	Alif Tamjid	24121308	Software Part
4.	Souvik Bamran Ratul	24121205	Hardware, Report
5.	Abir Chowdhury Ratul	24121204	Hardware Part

Objective

To observe how the load resistor affects the gain of a BJT amplifier, analyze the impact of including and excluding the emitter bypass capacitor, and determine the value of the coupling capacitor C₁ required to achieve a lower cut-off frequency of 18 Hz.

Circuit Diagram



Calculation of C₁:

Low Cut-Off frequency, $f_{cl} = 18 \text{ Hz}$

$$\begin{aligned} \text{Input Impedance, } R_{TH} &= (R_1 \times R_2) / (R_1 + R_2) && [\text{Using Thevenin theorem}] \\ &= (10 \times 74.9) / (10 + 74.9) \\ &= 8.82 \text{ k}\Omega \end{aligned}$$

We know, $f_{cl} = 1/2\pi RC$

$$\begin{aligned} \Rightarrow C_1 &= 1/(2\pi \times R_{TH} \times f_{cl}) \\ &= 1/(2 \times 3.1416 \times 8.82 \times 10^3 \times 18) \\ &= 1.002432 \times 10^{-6} \text{ F} \\ &\approx 1 \mu\text{F} \end{aligned}$$

Software Implementation:

Software Circuit Set Up (Without the Emitter Bypass Capacitor)

1(a)Circuit:

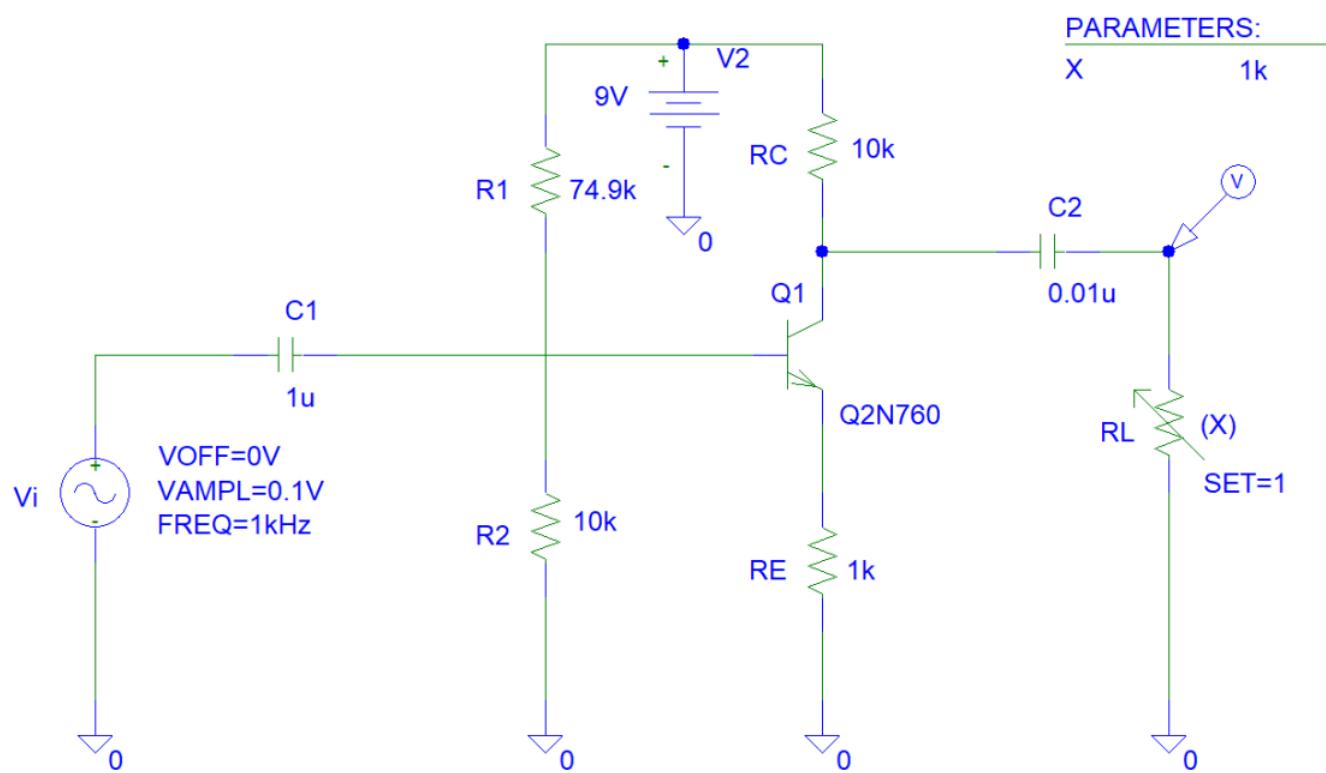
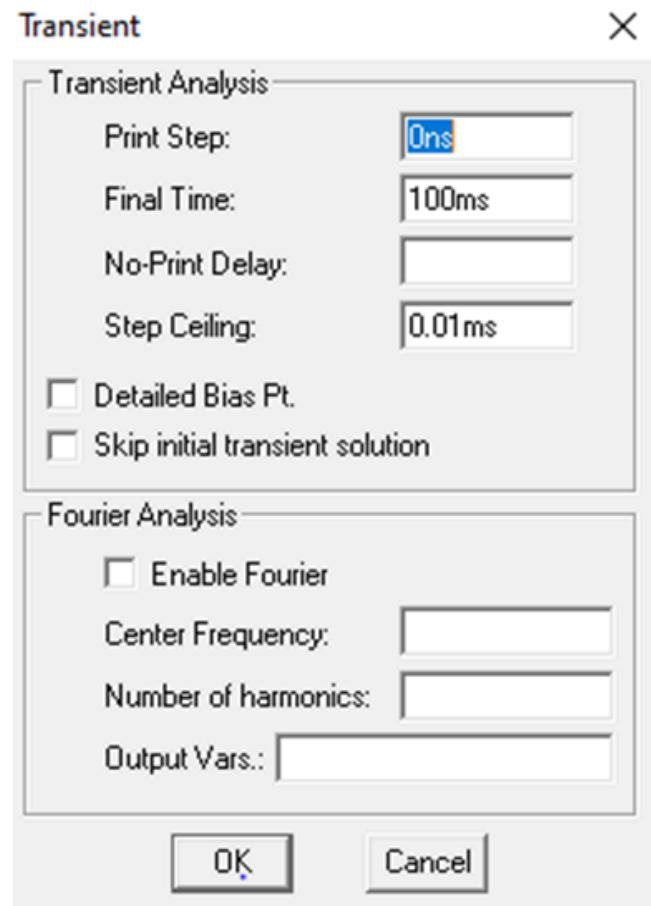
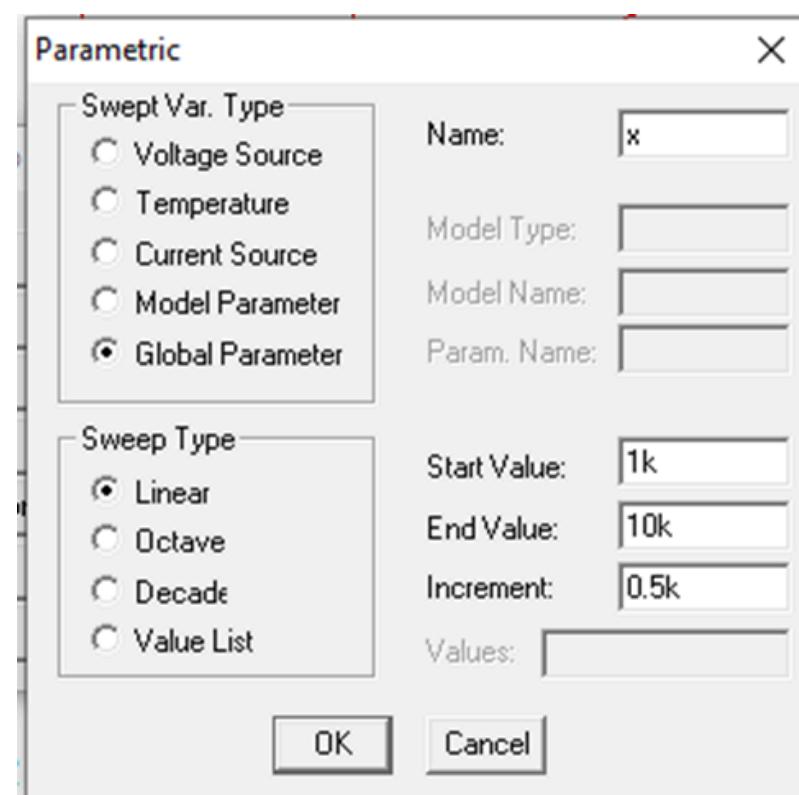


Figure: Simulation Circuit Without Capacitor

Transient Parameter



Parametric parameter



1(b) Varying Load Resistance and Gain vs. Time Graph

Graph 01:

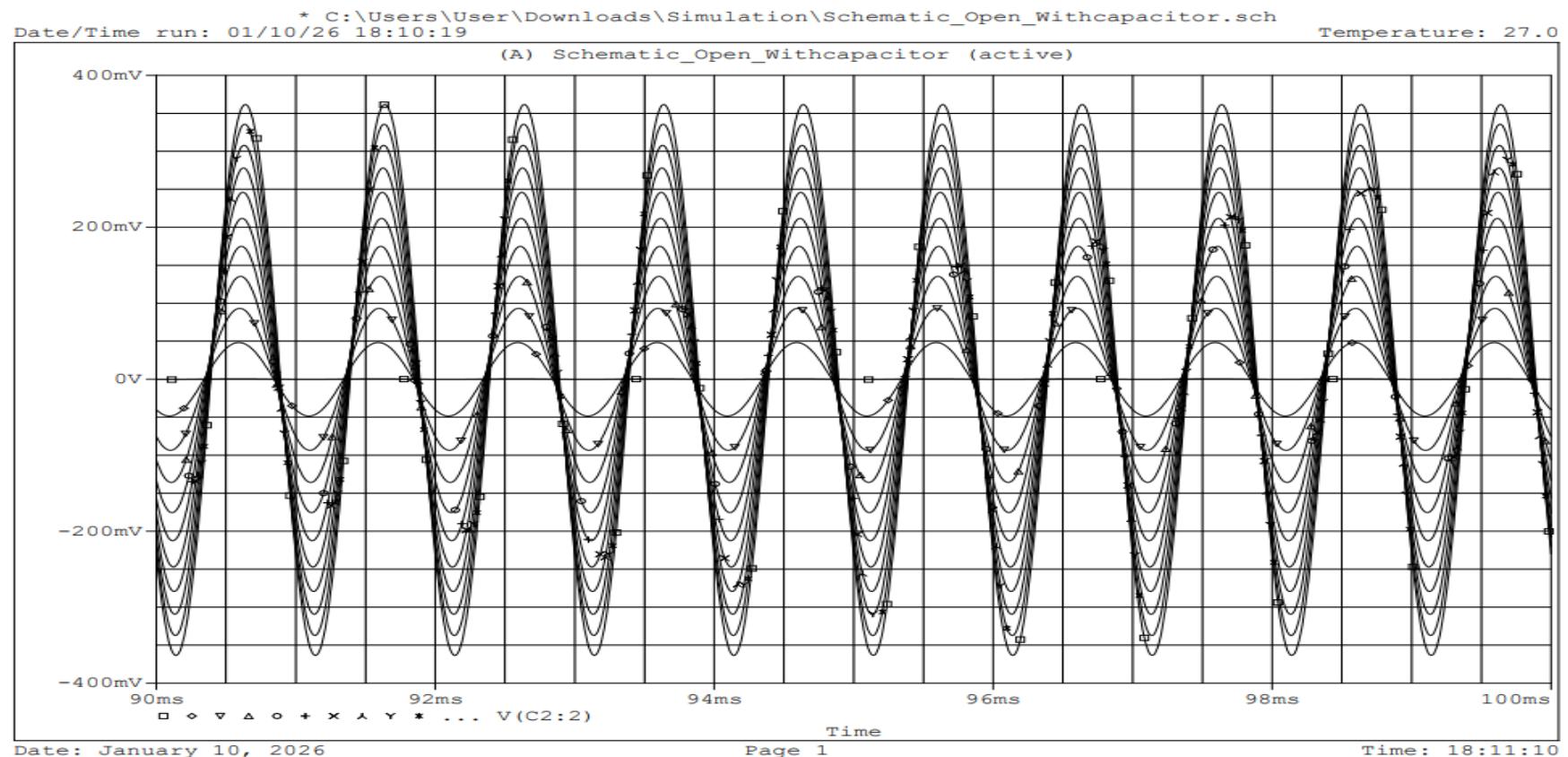
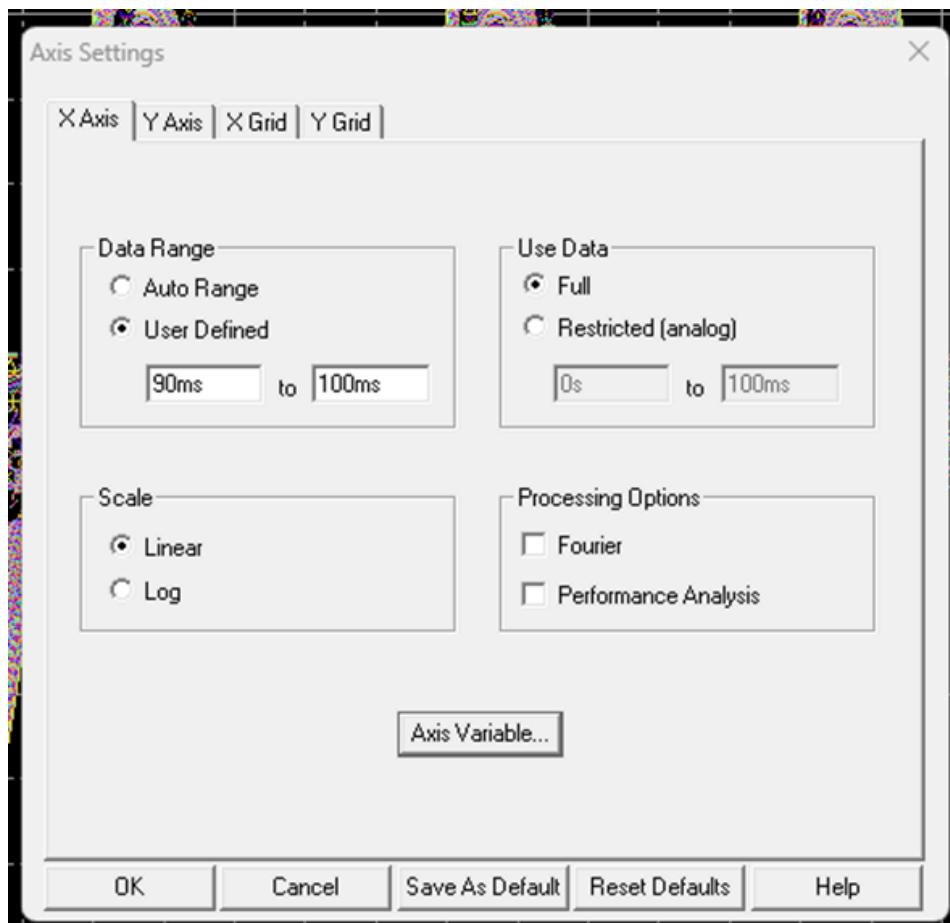


Figure: Gain Vs time Graph

Axis Setting



Graph 02:

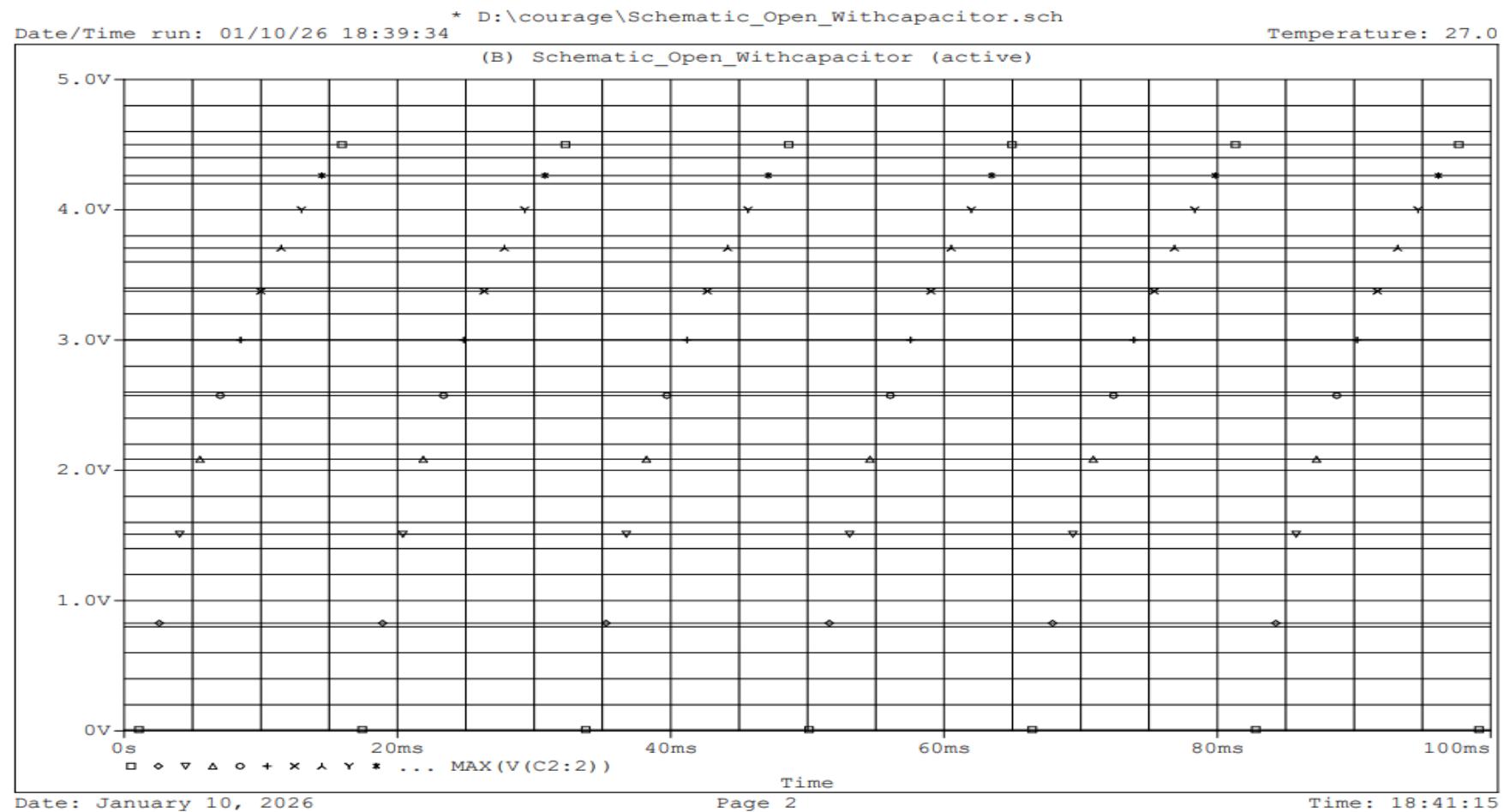


Figure: Gain Vs time Graph

1(c) Plotting Gain vs Load Resistance:

Data Table:

Gain	Raw curve
0.008978	0.0001
0.82679	0.1001
1.510254	0.2001
2.085233	0.3001
2.573527	0.4001
3.000824	0.5001
3.374993	0.6001
3.705541	0.7001
3.999551	0.8001
4.262665	0.9001
4.499884	1.0001

Gain vs Load Resistance Graph using Excel :

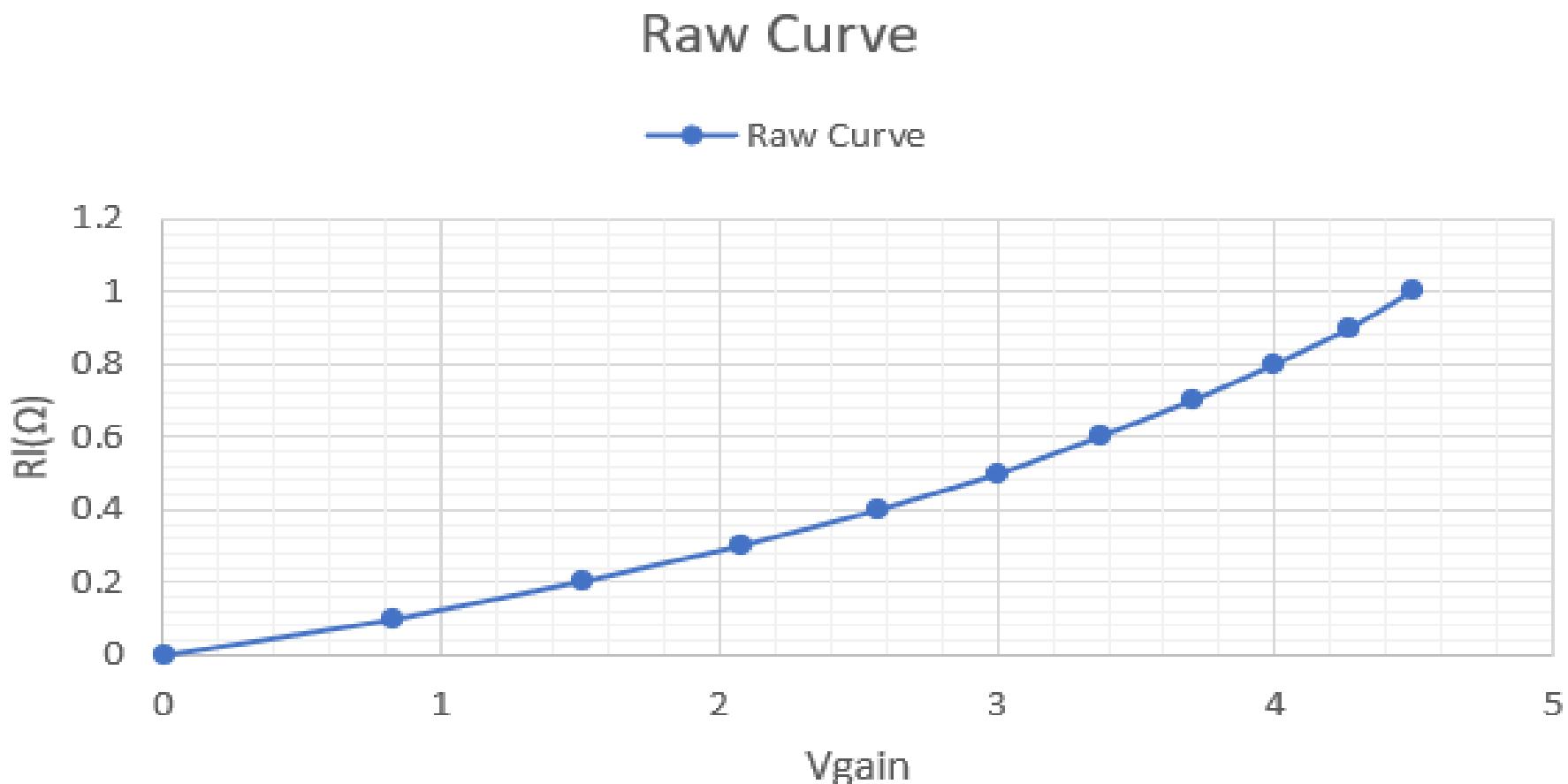


Figure: Gain VS R_l graph from the value of Pspice without Emitter Bypass Capacitor

Software Circuit Set Up (With the Emitter Bypass Capacitor):

2(a)Circuit:

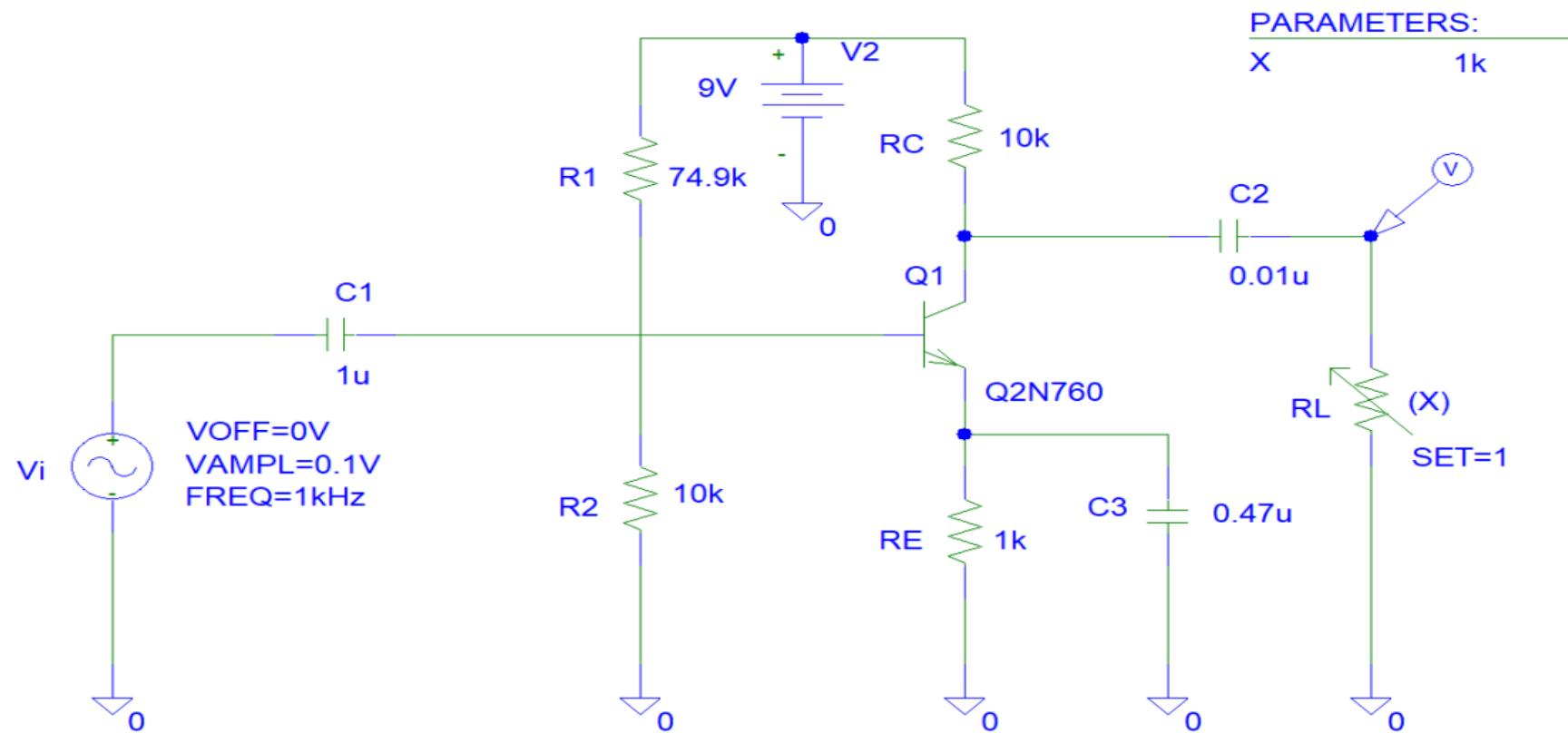
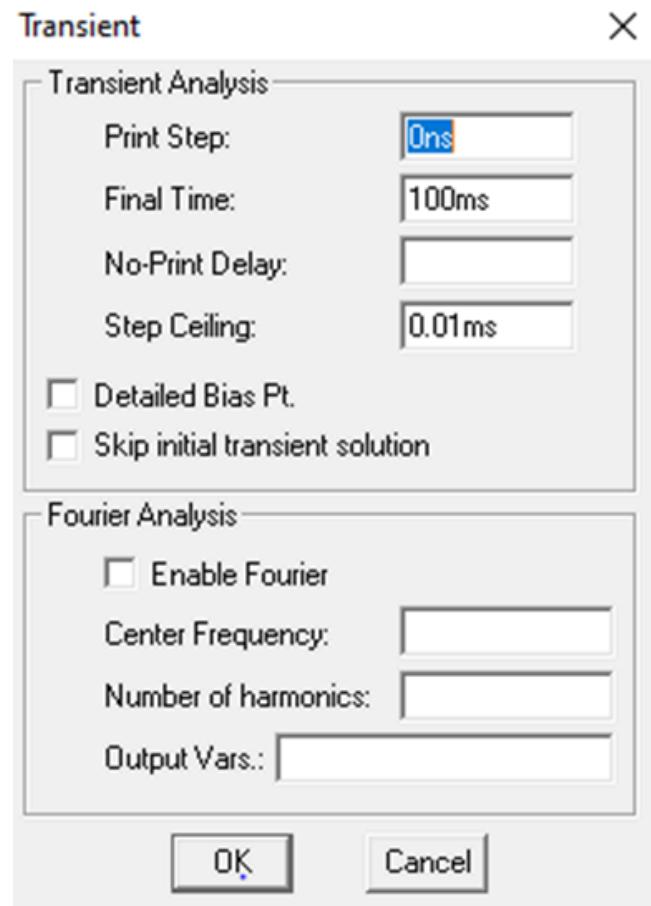
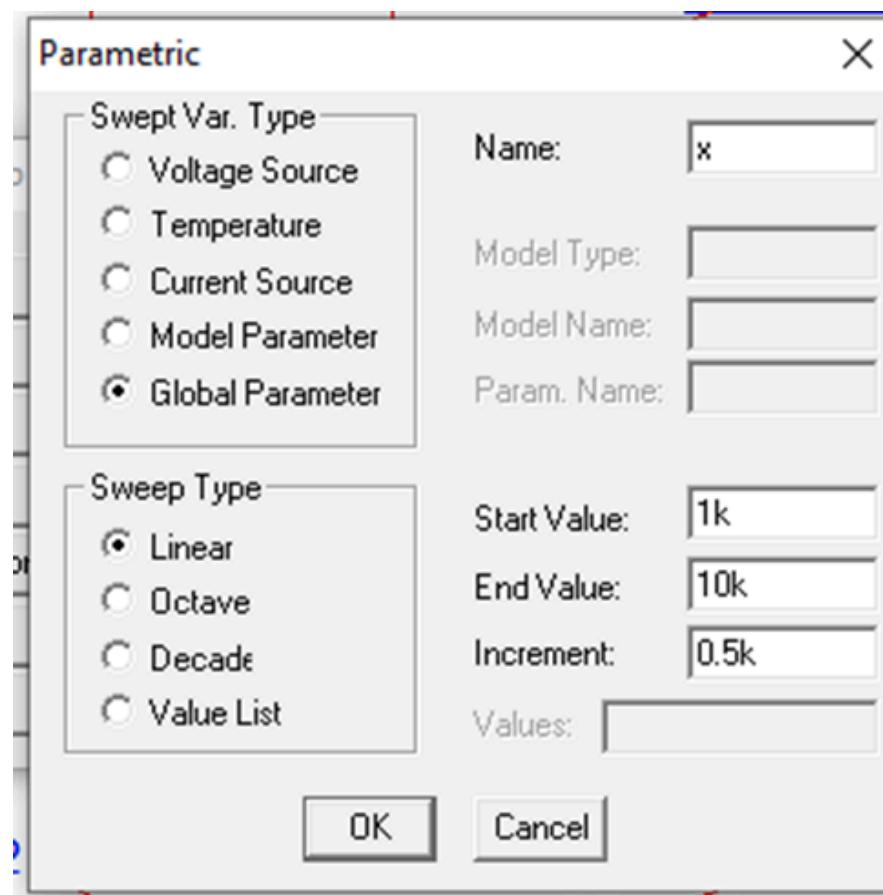


Figure: Simulation Circuit With Capacitor

Transient Parameter



Parametric parameter



2(b) Varying Load Resistance and Gain vs. Time Graph

Graph 01:

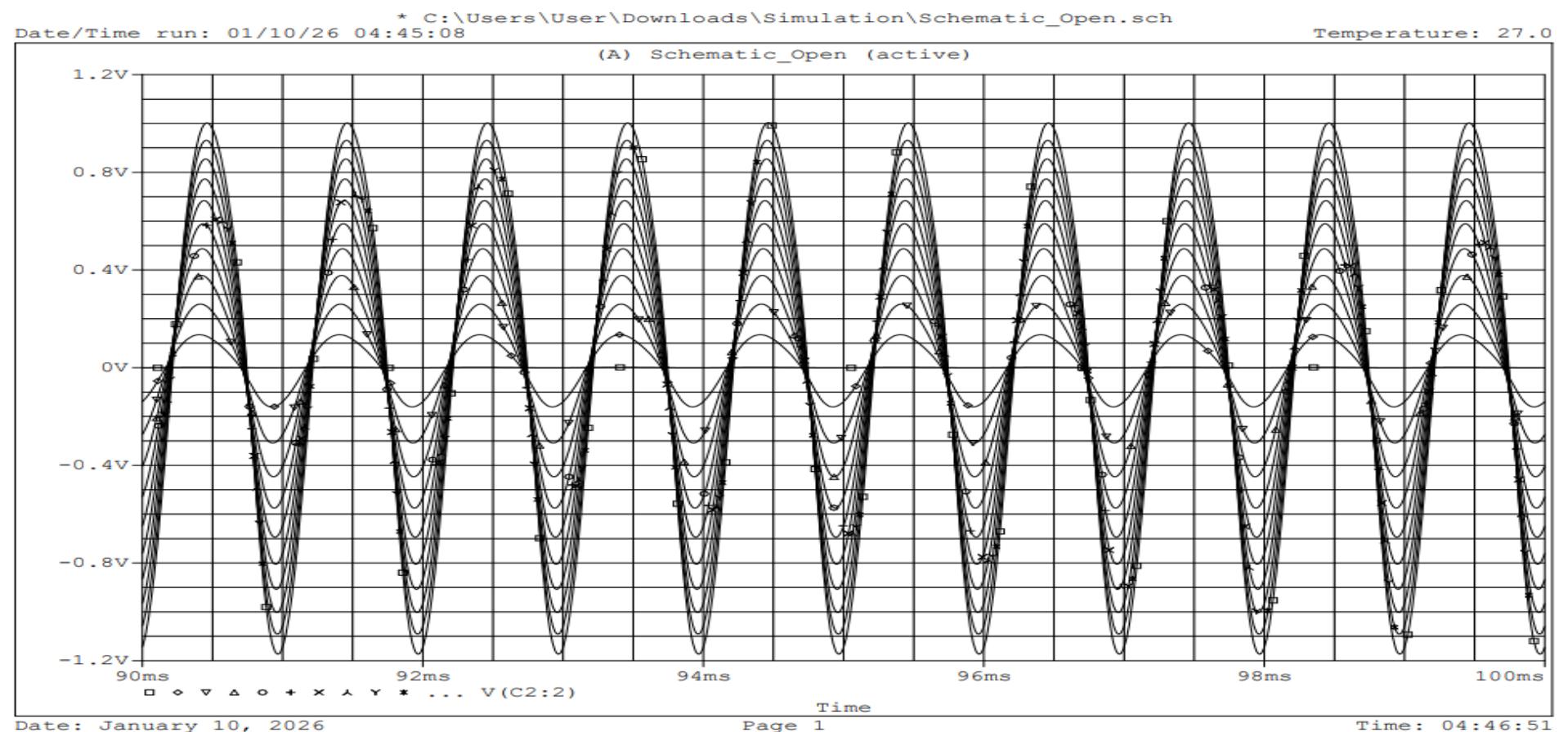
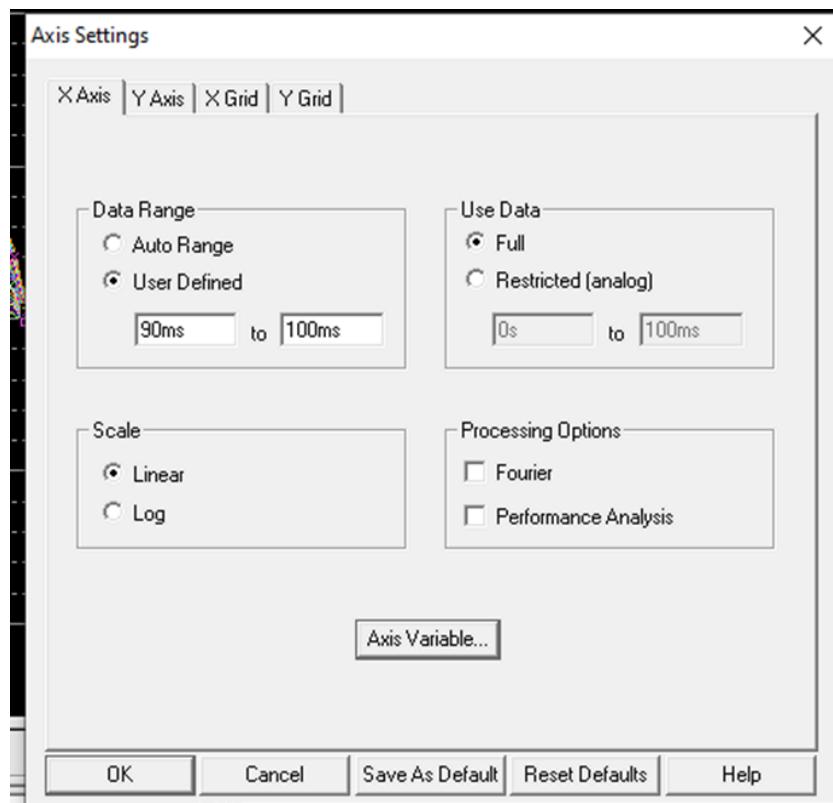


Figure: Gain Vs time Graph

Axis Setting



Graph 02:

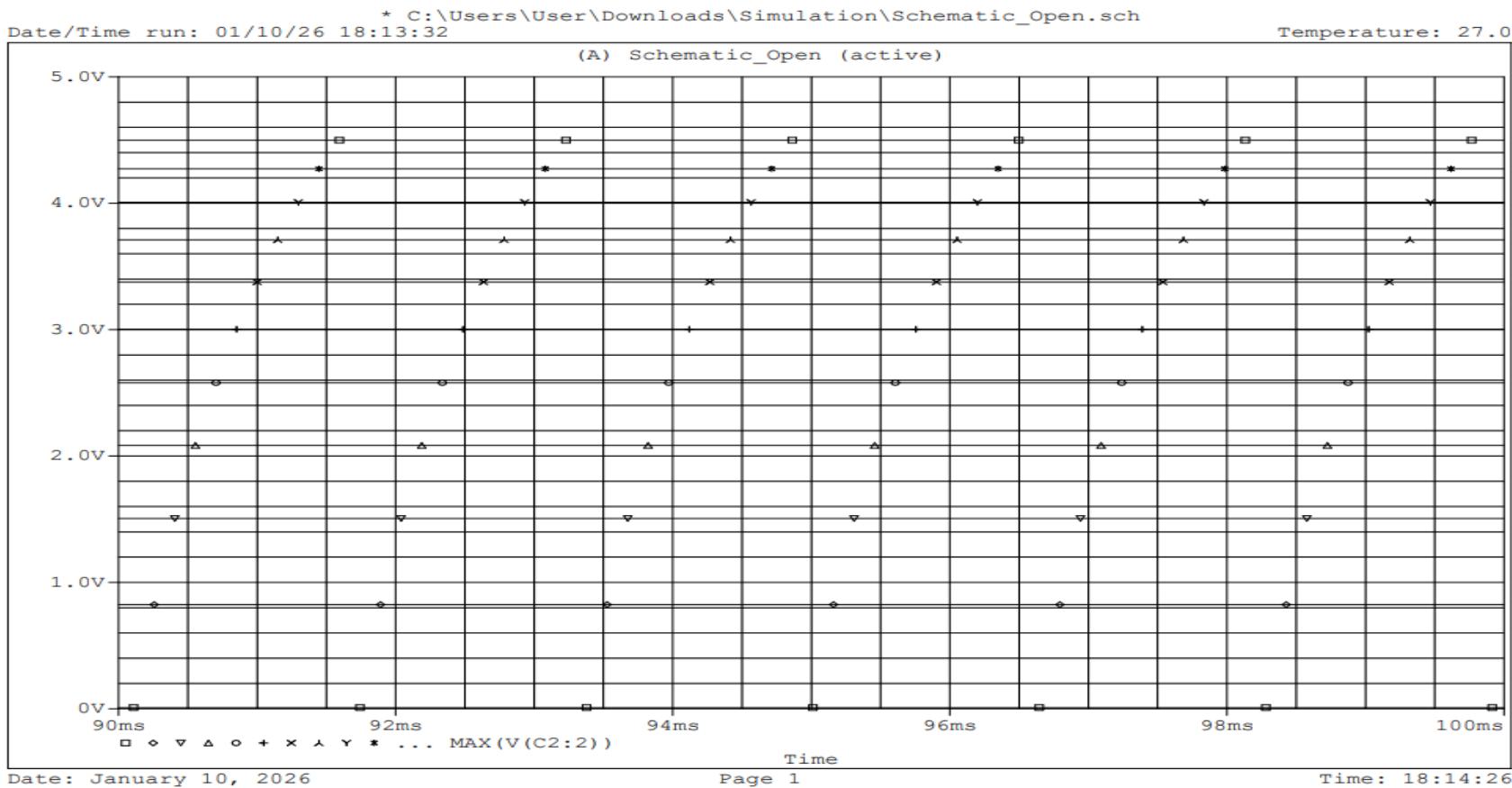


Figure: Gain Vs time Graph

2(c) Plotting Gain vs Load Resistance:

Data Table:

Gain	Raw Curve
0.008978	0.0001
0.824703	0.1001
1.506105	0.2001
2.083898	0.3001
2.579029	0.4001
3.002371	0.5001
3.376723	0.6001
3.709849	0.7001
4.006592	0.8001
4.272204	0.9001
4.498654	1.0001

Gain vs Load Resistance Graph using Excel:

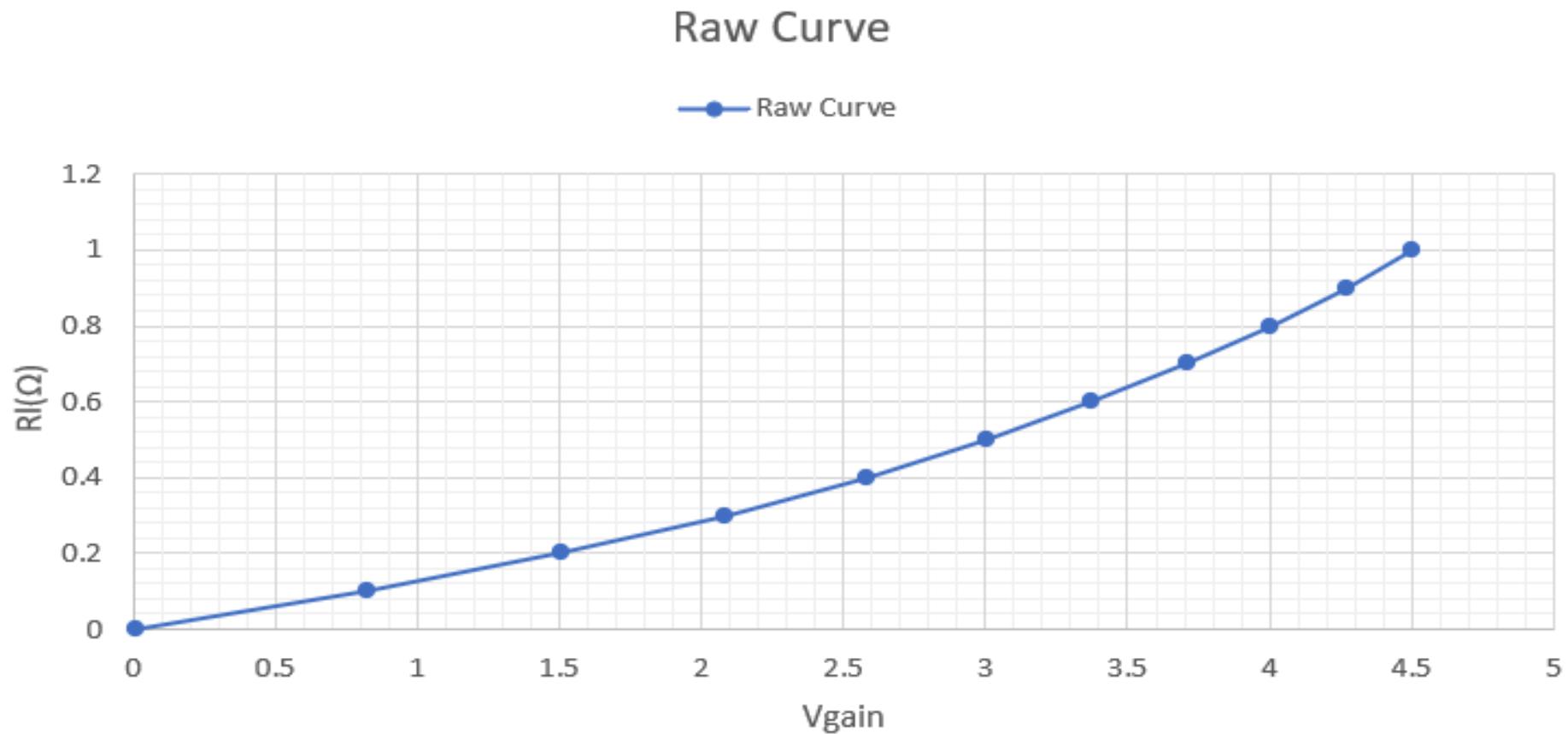


Figure: Av VS R_l graph from the value of Pspice with Emitter Bypass Capacitor

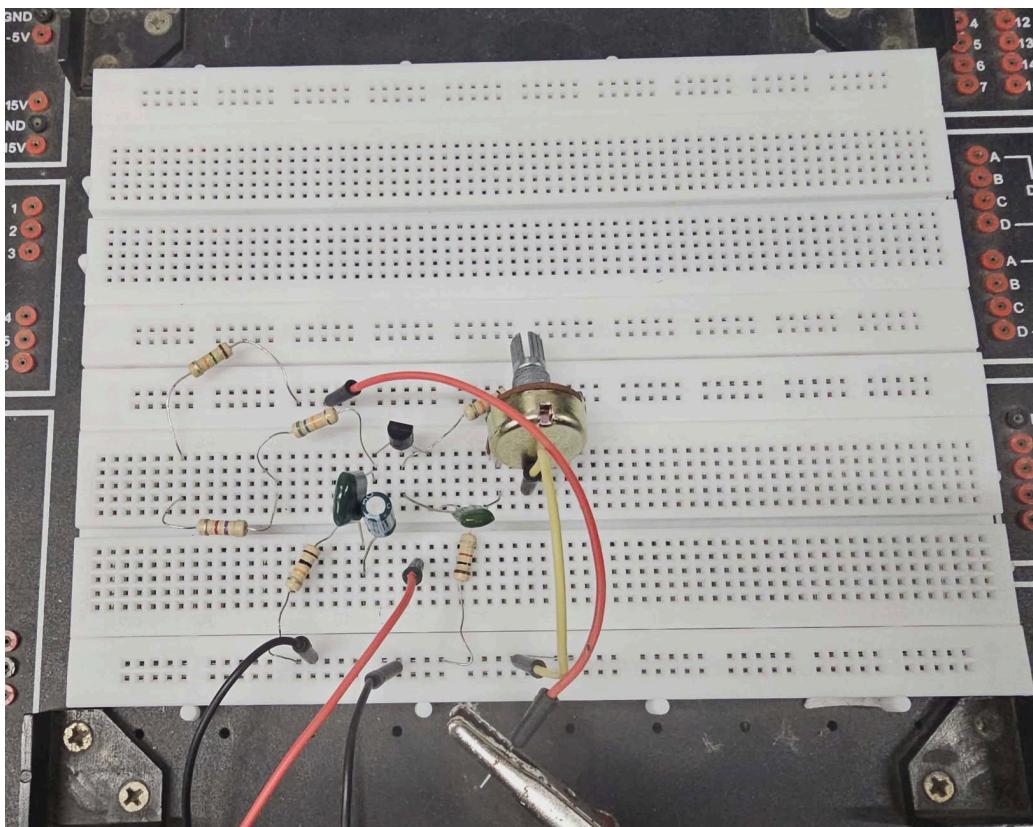
Hardware Implementation

Apparatus:

1. DC power supply
2. AC power supply
3. Resistors ($1\text{k}\Omega$, $10\text{k}\Omega$, $56\text{k}\Omega$, $15\text{k}\Omega$, $4.7\text{k}\Omega$)
4. Potentiometer ($10\text{k}\Omega$)
5. Capacitors ($0.01\mu\text{F}$, $0.47\mu\text{F}$, $1\mu\text{F}$, $0.1\mu\text{F}$)
6. NPN BJT
7. Wires
8. Breadboard
9. Digital Multimeter

1. Without the Emitter Bypass Capacitor

a) Circuit

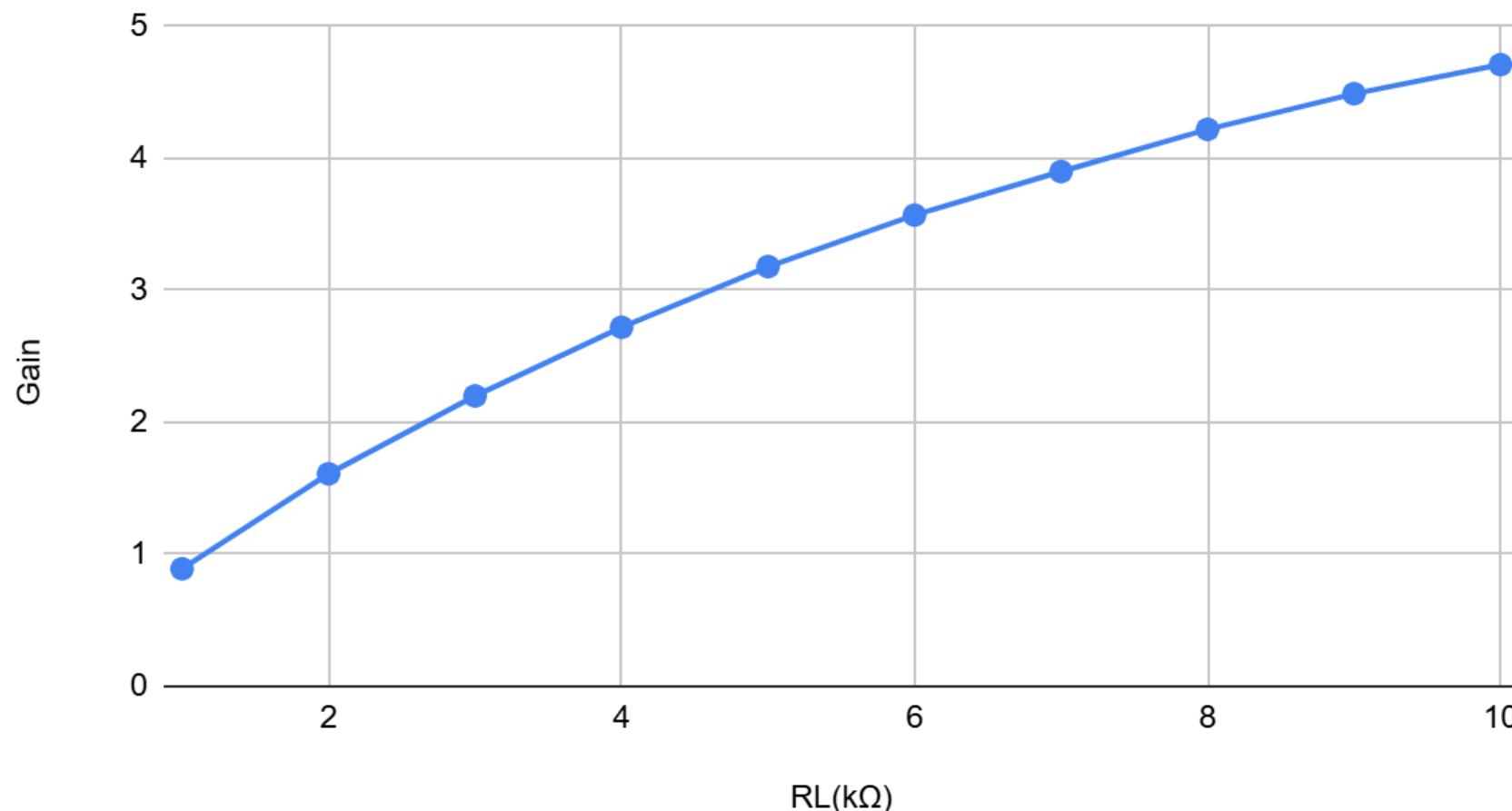


b) Data Table

$R_L(k\Omega)$	$V_{in}(mV)$	$V_{out}(mV)$	Gain, $A_V = V_{out}/V_{in}$
1	100	89	0.89
2	100	161	1.61
3	100	220	2.2
4	100	272	2.72
5	100	318	3.18
6	100	357	3.57
7	100	390	3.9
8	100	422	4.22
9	100	449	4.49
10	100	471	4.71

c) Graph Plotting

Gain vs. $RL(k\Omega)$ (Without Bypass Capacitor)

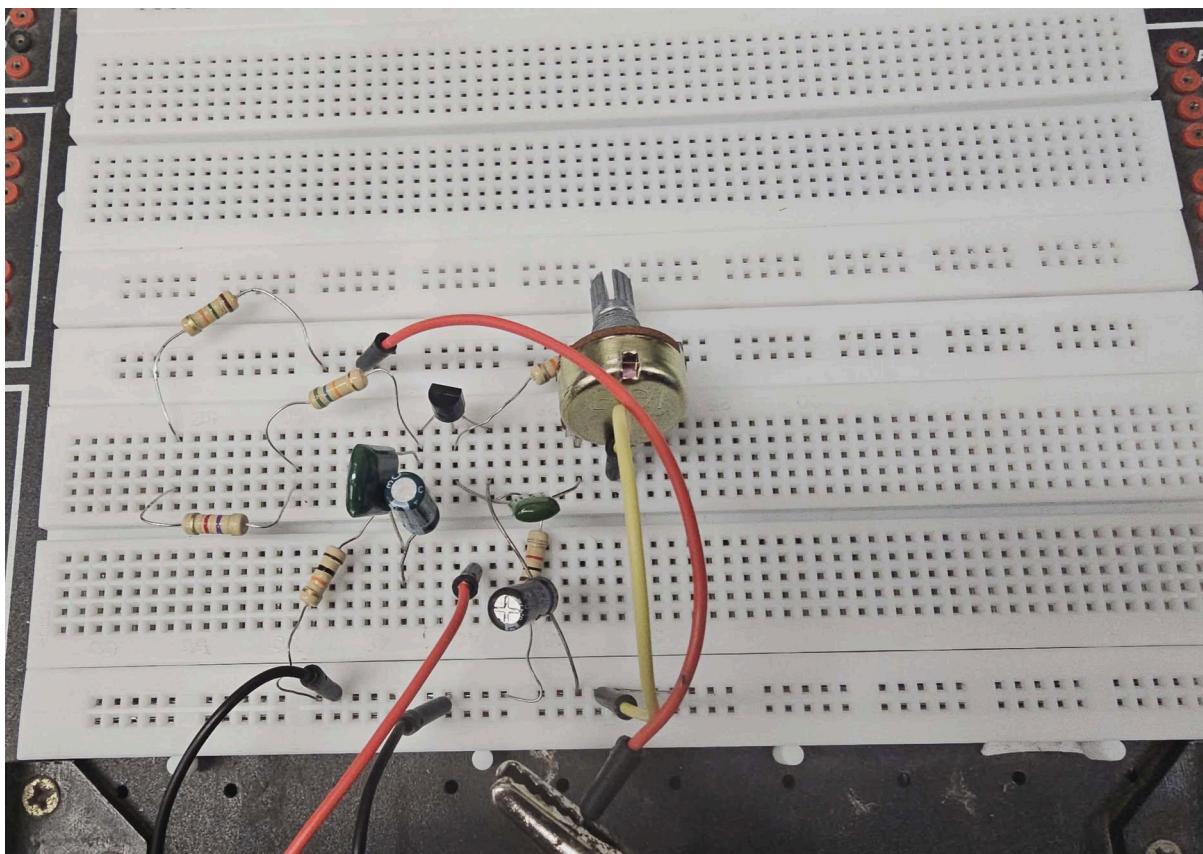


Interpretation

The graph indicates that the voltage gain of this common emitter amplifier increases with increasing load resistance R_L , where the gain remains relatively low and increases gradually because the absence of the bypassing capacitor in the emitter introduces emitter degeneration. This unbypassed emitter resistance gives rise to negative feedback that stabilizes the amplifier by significantly lowering its gain. For an increased value of R_L , the effective collector load is increased. It results in an increase in the voltage gain. However, because of the negative feedback, the gain does not increase as rapidly, since the growth is saturated rather than a steep rise in gain.

2. With the Emitter Bypass Capacitor

a) Circuit

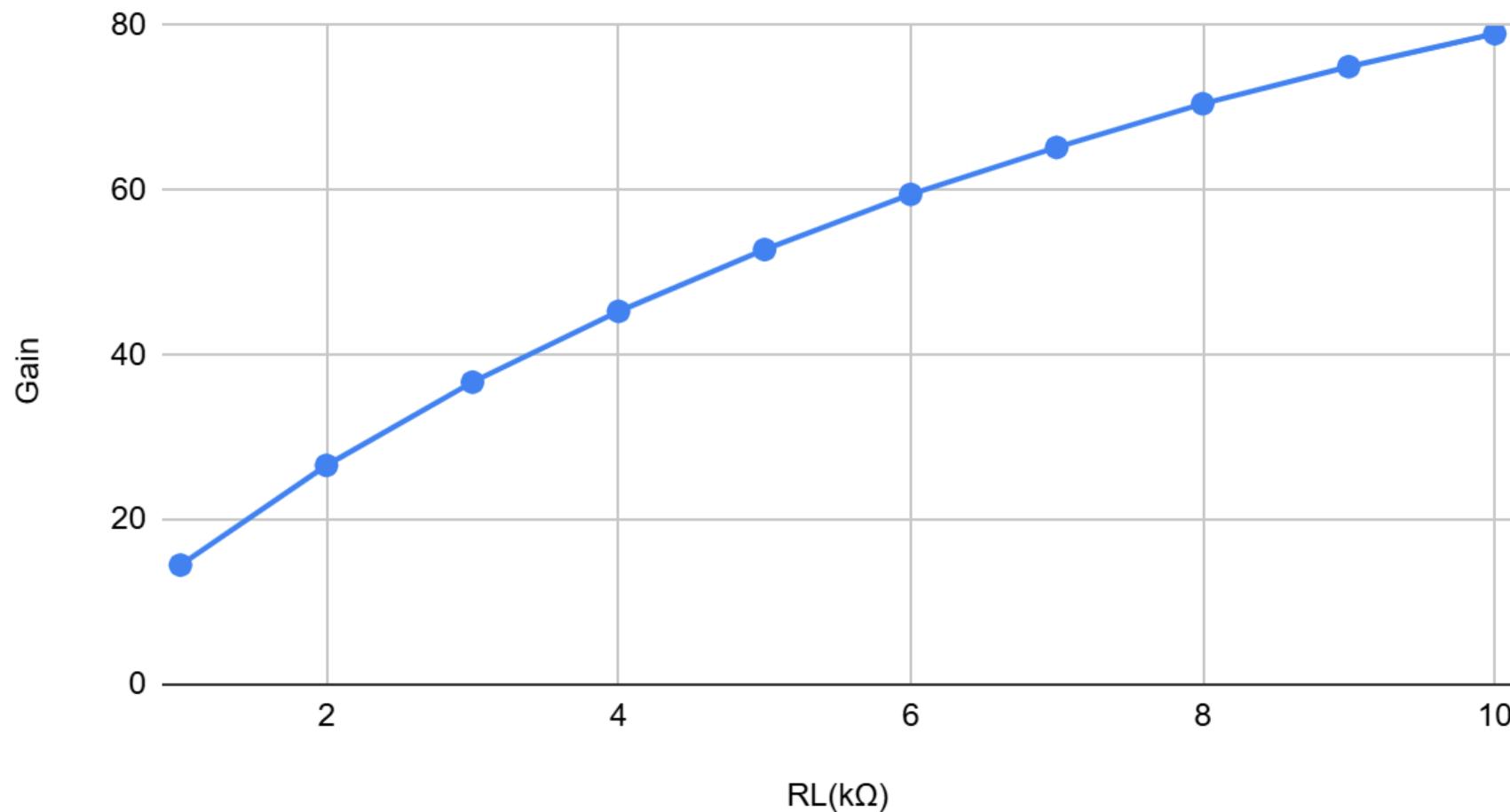


b) Data Table

R_L(kΩ)	V_{in}(mV)	V_{out}(V)	Gain, A_V=V_{out}/V_{in}
1	100	1.45	14.5
2	100	2.66	26.6
3	100	3.67	36.7
4	100	4.53	45.3
5	100	5.28	52.8
6	100	5.95	59.5
7	100	6.52	65.2
8	100	7.05	70.5
9	100	7.5	75
10	100	7.9	79

c) Graph Plotting

Gain vs. $RL(k\Omega)$ (With Bypass Capacitor)



Interpretation

When the emitter bypass capacitor is added to the circuit, the gain becomes highly dependent on the value of the load resistance R_L . This is due to the absence of the emitter ac resistance; hence, there is no emitter degeneration or negative feedback. Consequently, the gain of the circuit becomes high compared to the previous circuit and is dependent on the value of R_L . From the graph, there is a sudden increase in gain for smaller values of R_L . Additionally, as R_L increases, the gain levels off to a saturation point. This means that for the circuit, the gain is dependent on the transistor's characteristics and the collector resistor.

Comparision

The amplifier without the emitter bypass capacitor shows low and slowly increasing gain with increasing R_L because the emitter resistor remains in the AC signal path, introducing emitter degeneration and strong negative feedback that stabilizes operation but reduces gain. In contrast, with the emitter bypass capacitor present, the emitter resistor is effectively shorted for AC signals, removing negative feedback and significantly increasing the voltage gain, making the gain much more sensitive to changes in R_L . Thus, the difference arises because the bypass capacitor eliminates AC emitter resistance, increasing the effective transconductance and allowing the collector–load combination to produce a much larger output voltage for the same input signal.

Troubleshooting:

1. No Output Signal on Oscilloscope

Reason: The input AC signal was too low, or the oscilloscope probe was not properly grounded.

Solution: We increased the input signal to a measurable range and checked the probe connection.

2. No $74.9\text{k}\Omega$ Valued Resistor

Solution: We added $56\text{k}\Omega$, $15\text{k}\Omega$ & $3.9\text{k}\Omega$ in series to make a total $74.9\text{k}\Omega$.

3. Series resistor lost resistance

Reason: Every resistor has some error, and when added in series errors also add up.

Solution: We replaced $3.9\text{k}\Omega$ with $4.7\text{k}\Omega$ to get closer to the $74.9\text{k}\Omega$ measured value.

4. $1\mu\text{F}$ was showing $0.88\mu\text{F}$ with multimeter

Reason: Component tolerances, parasitic resistance and inductance, meter limitations.

Solution: We added $0.1\mu\text{F}$ in parallel to increase capacitance

5. Couldn't find Q2N760 in Pspice

Reason: The Old model was installed

Solution: Downloaded orcade 9.2

