Steps to follow while solving:

1. **Check if channel is induced:**

- If a current is shown to be flowing $(I_D \neq 0)$ then channel is **definitely induced**.
- If $V_{GS} < V_{TN}$, **no channel is induced (NMOS)**$\rightarrow Cut-off$
- If $V_{GS} > V_{TP}$, **no channel is induced (PMOS)** $\rightarrow Cut-off$
- If gate terminal voltage is greater than source terminal voltage (even if there is a resistance connected between source terminal and the DC voltage source) by more than the threshold voltage, then channel is induced. (NMOS)
- If gate terminal voltage is smaller than source terminal voltage (even if there is a resistance connected between source terminal and the DC voltage source) by more than the threshold voltage, then channel is induced. (PMOS)

Steps to follow while solving:

2. check $\boldsymbol{V_{GD}}$, **If channel is induced, [to determine the region of operation]**

- if V_{GD} can be measured directly, then find the region of operation.
  For **NMOS**, $\boldsymbol{V_{GD} < V_{TN}: saturation, V_{GD} \geq V_{TN}: Triode}$.
  For **PMOS**, $\boldsymbol{V_{GD} > V_{TP}: saturation, V_{GD} \leq V_{TP}: Triode}$.

- If V_{GD} cannot be determined directly (as there is resistor between drain terminal and the V_{DD}, for example), then go for **assumption**.
- Assume **saturation region/Triode**.
- Solve the circuit based on the assumption you have made, find $\boldsymbol{I_D, V_D, V_S\ etc}$.
- **Justify** your assumption. For justification check $\boldsymbol{V_{GD}}$,
- if V_{GD} can be measured directly, then find the region of operation.
  For **NMOS**, $\boldsymbol{V_{GD} < V_{TN}: saturation, V_{GD} \geq V_{TN}: Triode}$.
  For **PMOS**, $\boldsymbol{V_{GD} > V_{TP}: saturation, V_{GD} \leq V_{TP}: Triode}$.

- Follow the problems solved in the class.

$k_n = 0.5\ {}^{mA}/_{V^2}, V_t = 0.8V, Determine\ I_D, V_D, V_S. Determine\ the\ region\ of\ operation.$

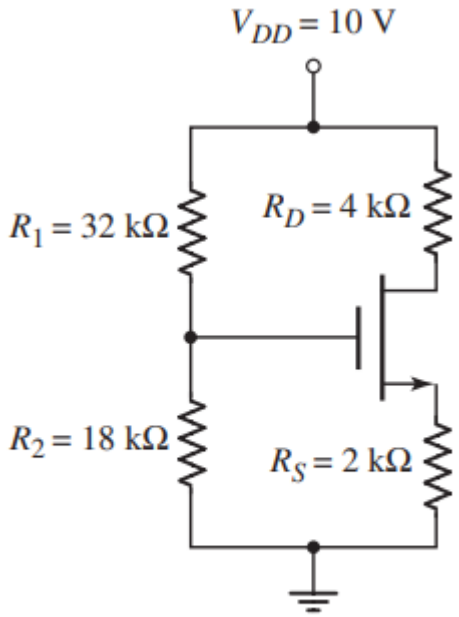
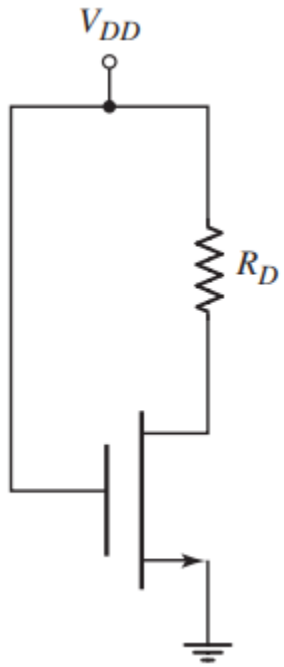


Figure P3.26



$V_{DD} = 5V, R_D = 5k, 2k, 10k$

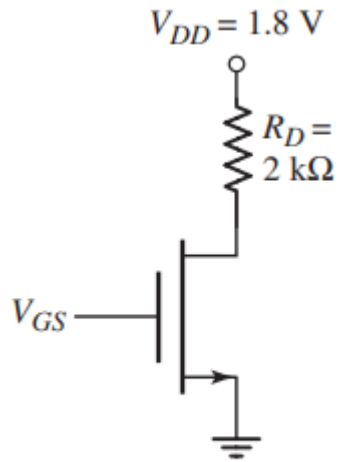
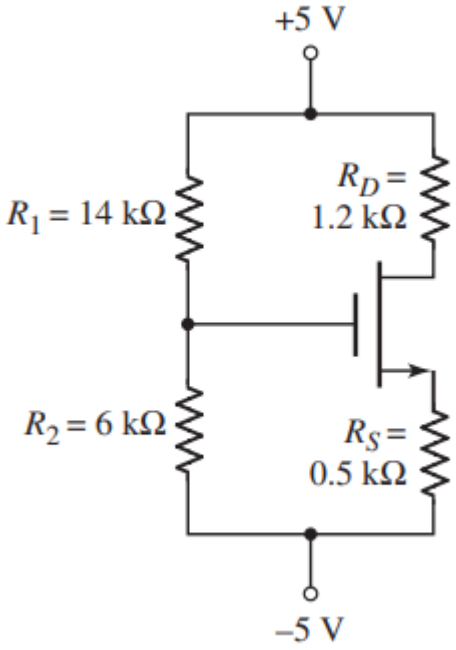


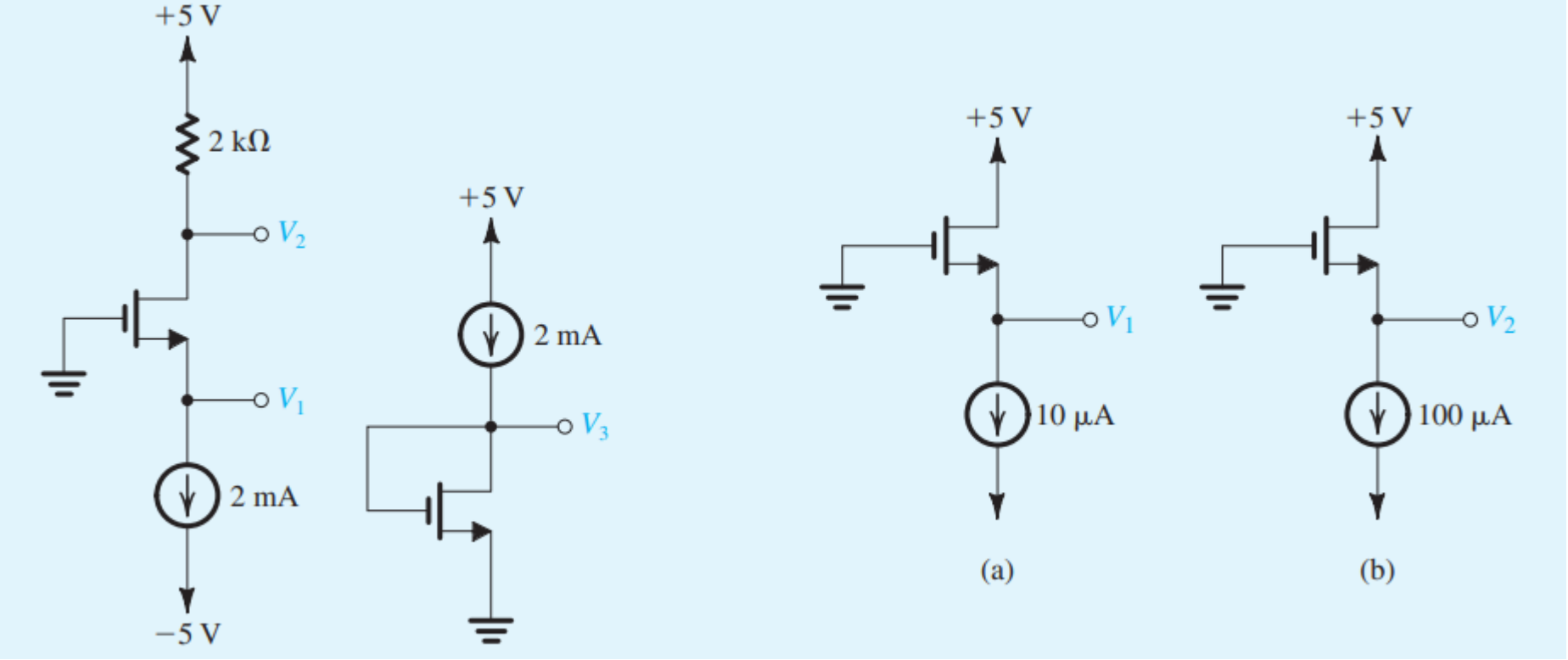
Figure P3.34

$V_{GS} = 5V$

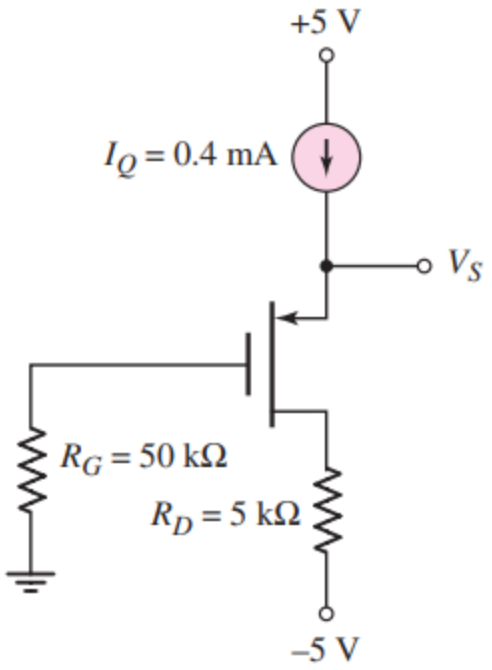


$k_n = 0.4\ {}^{mA}/_{V^2}, V_t = 1V$, *Determine* I_D, *and the labeled voltages*

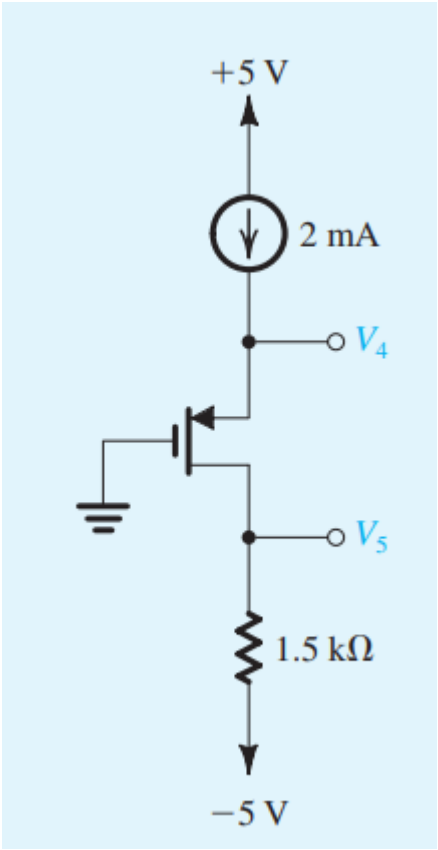
Determine the region of operation



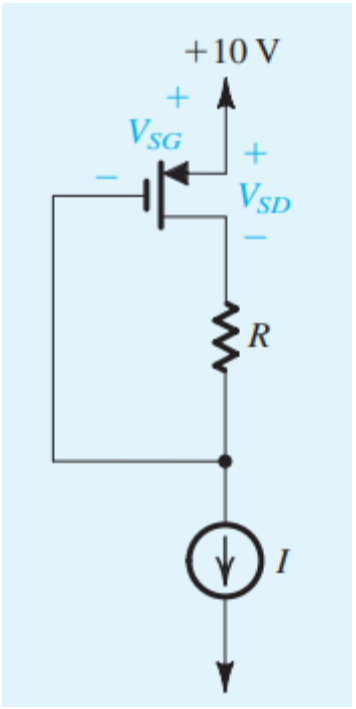
For the circuit (a)and (b), determine the labeled voltages.
$k_p = 0.4\ {}^{mA}/_{V^2}, V_{tp} = -0.8V.$
Determine the region of operation



(a)



(b)

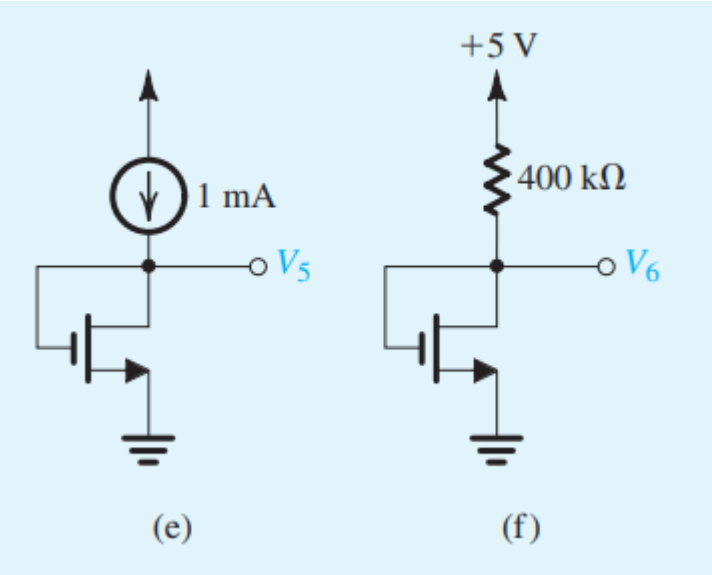


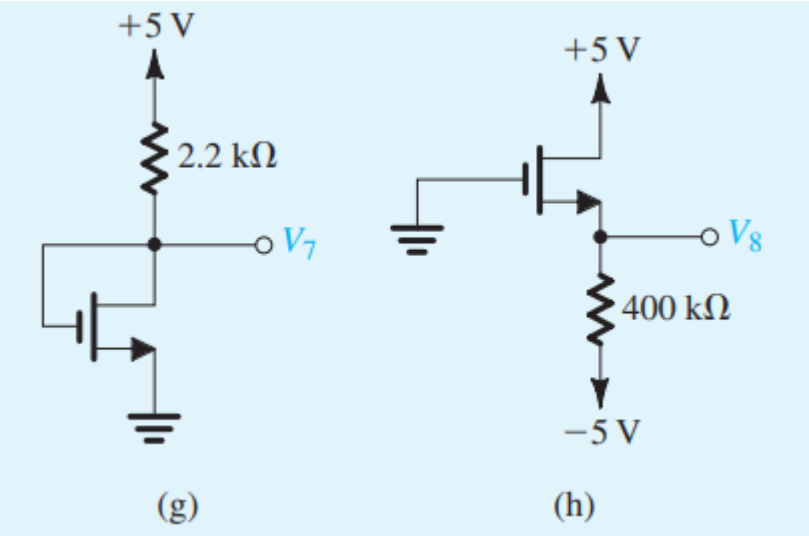
If the transistor is specified to have $|V_{tp}| = 1$ V and $k_p = 0.2$ mA/V^2, and for $I = 0.1$ mA, find the voltages V_{SD} and V_{SG} for $R = 0$, 10 kΩ, 30 kΩ, and 100 kΩ.

(c)

$$k_n = 0.5\ {}^{mA}/_{V^2}, V_t = 0.8V, \textit{Determine } I_D, \textit{and the labeled voltages}$$

Determine the region of operation





3.29 The transistor in the circuit in Figure P3.29 has parameters $V_{TP} = -0.8$ V and $K_p = 0.20$ mA/V^2. Sketch the load line and plot the Q-point for (a) $V_{DD} = 3.5$ V, $R_D = 1.2$ kΩ and (b) $V_{DD} = 5$ V, $R_D = 4$ kΩ. What is the operating bias region for each condition?

3.30 Consider the circuit in Figure P3.30. The transistor parameters are $V_{TP} = -0.8$ V and $K_p = 0.5$ mA/V^2. Determine I_D, V_{SG}, and V_{SD}.