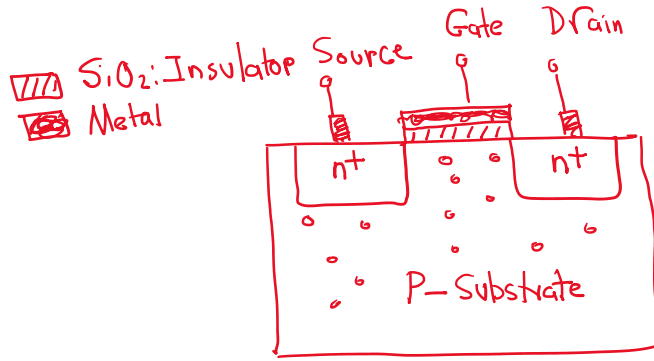
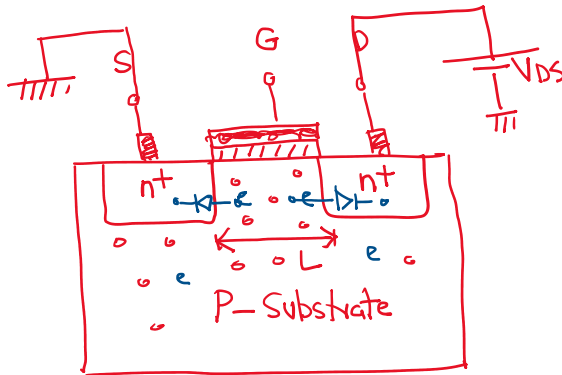
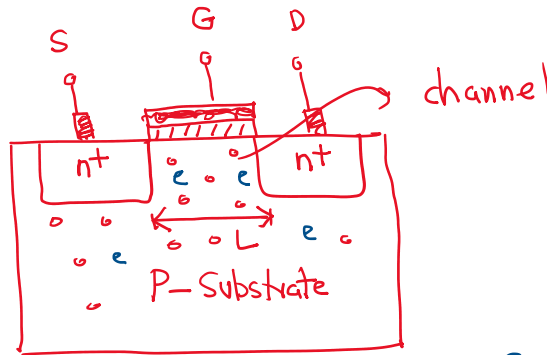


MOSFET: Metal Oxide Semiconductor Field Effect Transistor

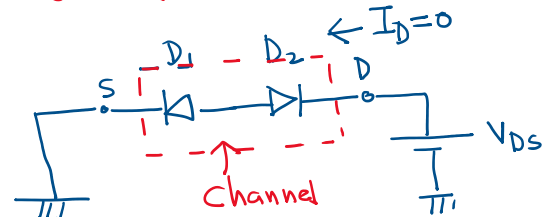


$1B \rightarrow 1 \text{ hole}$
 P: Hole Max
 e: Electron Min.
 n+: Heavily doped (Huge amount of P are added)

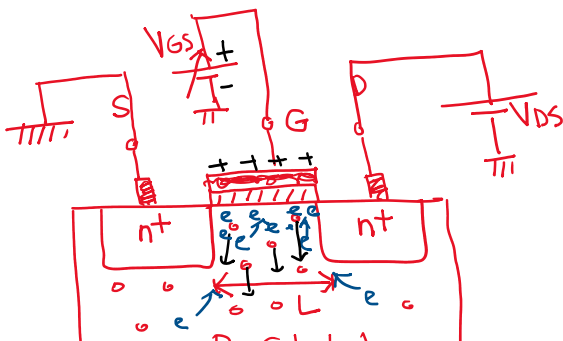
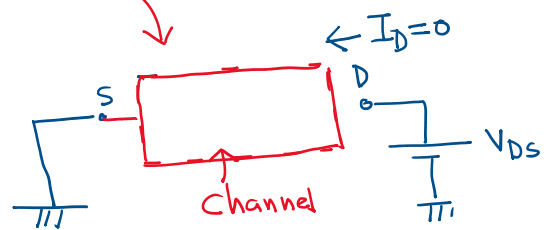


Case I.

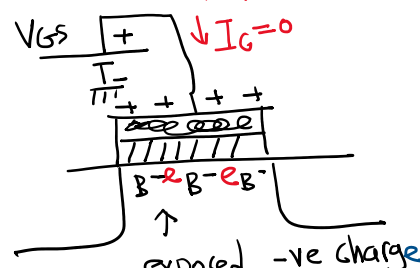
Gate: (No voltage)



Insulator (No free electrons)

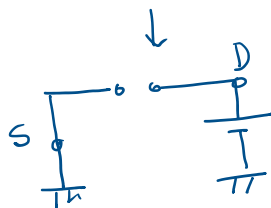
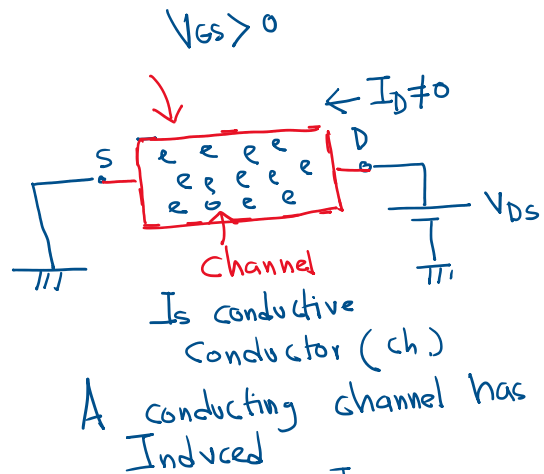
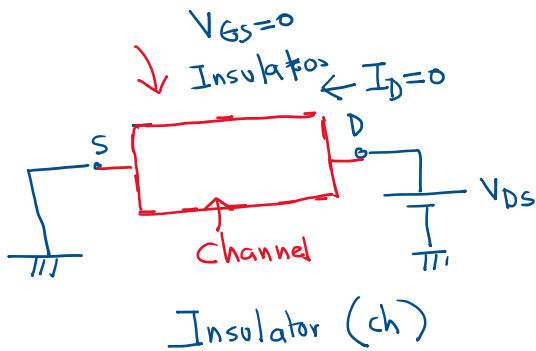
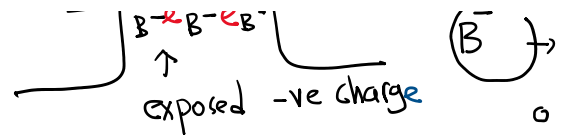
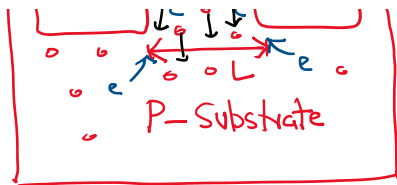


Case II: Apply V_{GS} : (+ve)

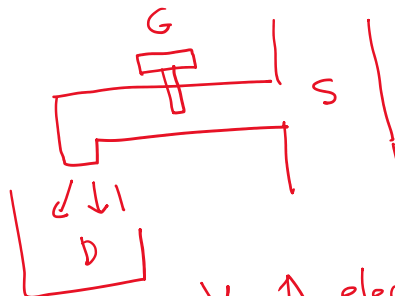
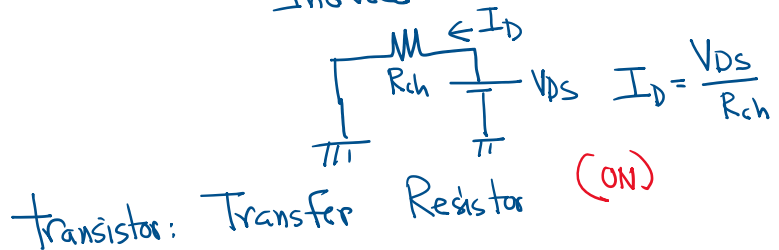


$B^- \rightarrow$ Neutral

$B^- \rightarrow$



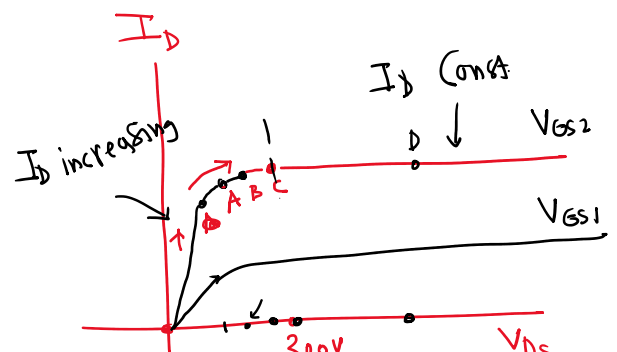
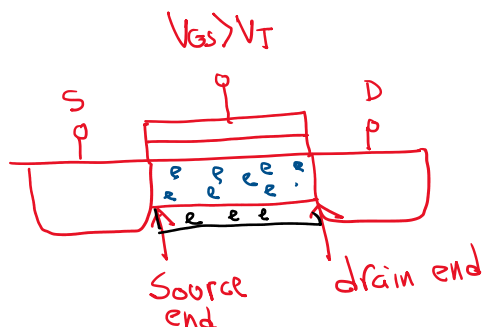
⊗ Cut-off



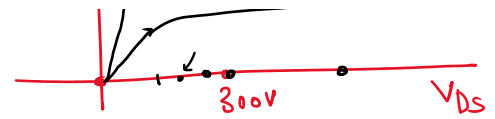
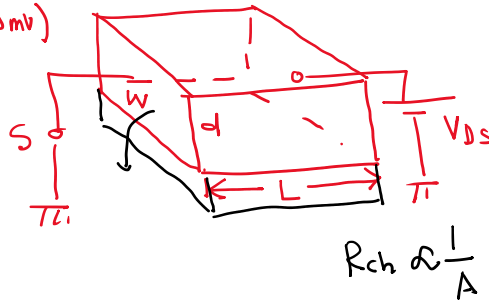
$V_{GS} \uparrow$, electron Accumulation at Oxide/Semiconductor Interface (ch region) \uparrow

V_T (threshold Voltage).

Value of V_{GS} at which sufficient # of electrons accumulate under the oxide layer to create a conducting channel is known as V_T .

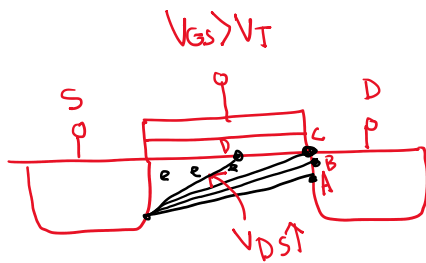


Source end drain end
Small V_{DS} ($\sim 300\text{mV}$)



$$I_{D1} = \frac{V_{DS1}}{R_{ch1}}, \quad I_D \propto V_{DS}$$

$$I_{D2} = \frac{V_{DS}}{R_{ch2}}, \quad R_{ch2} < R_{ch1}$$

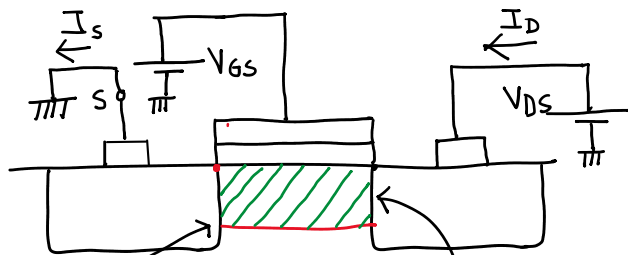


Position: C; pinch off: Maximum drain current

Position D: ch. ~~does~~ doesn't exist at the drain end.

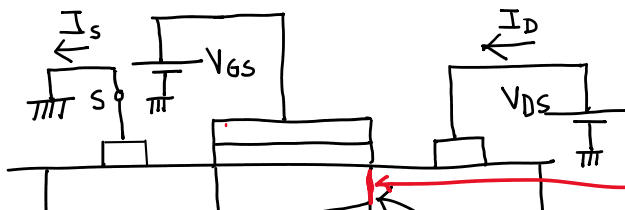
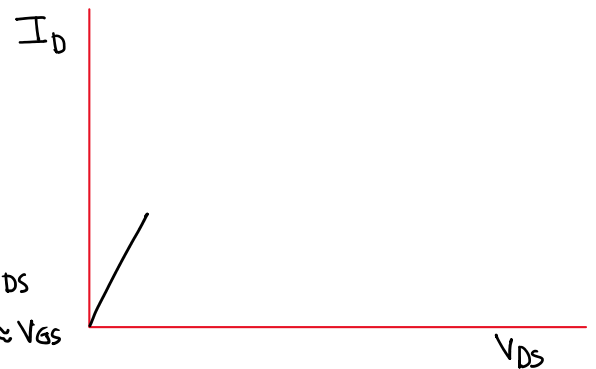
I_D increasing \rightarrow Having channel at the drain end (A, B, C)

I_D Constant \rightarrow channel doesn't exist at the drain end (D)

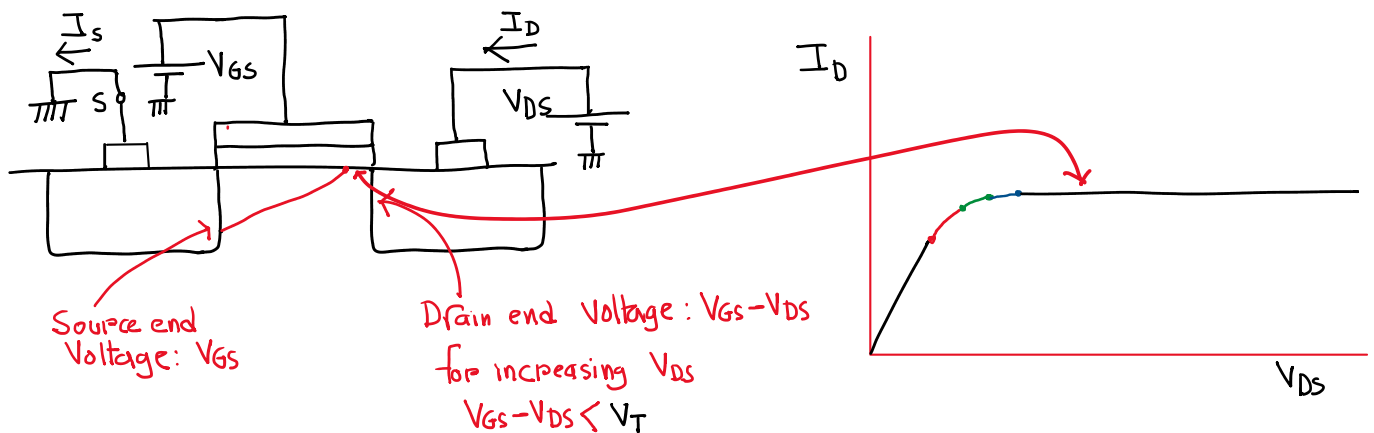
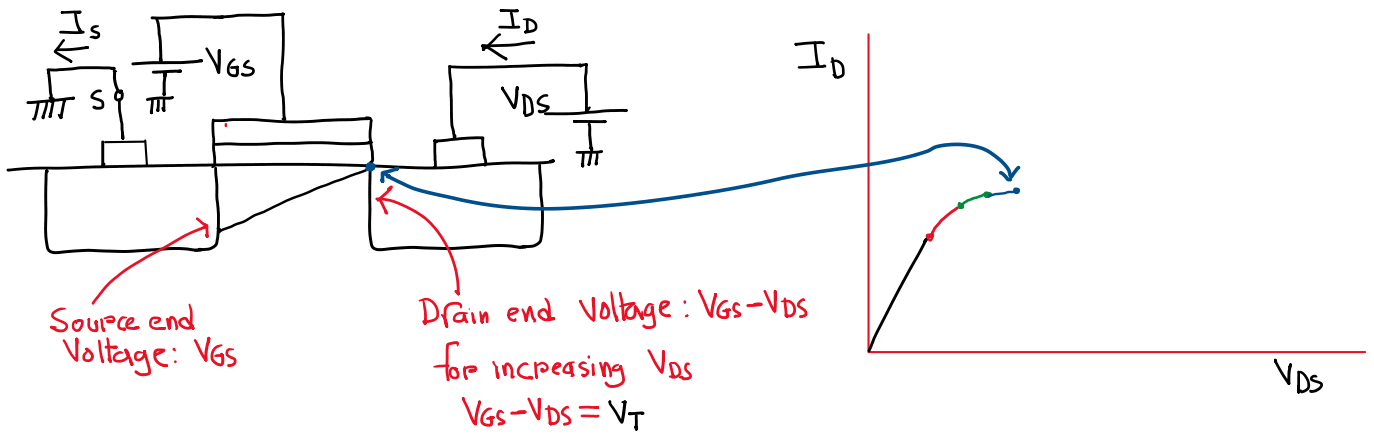
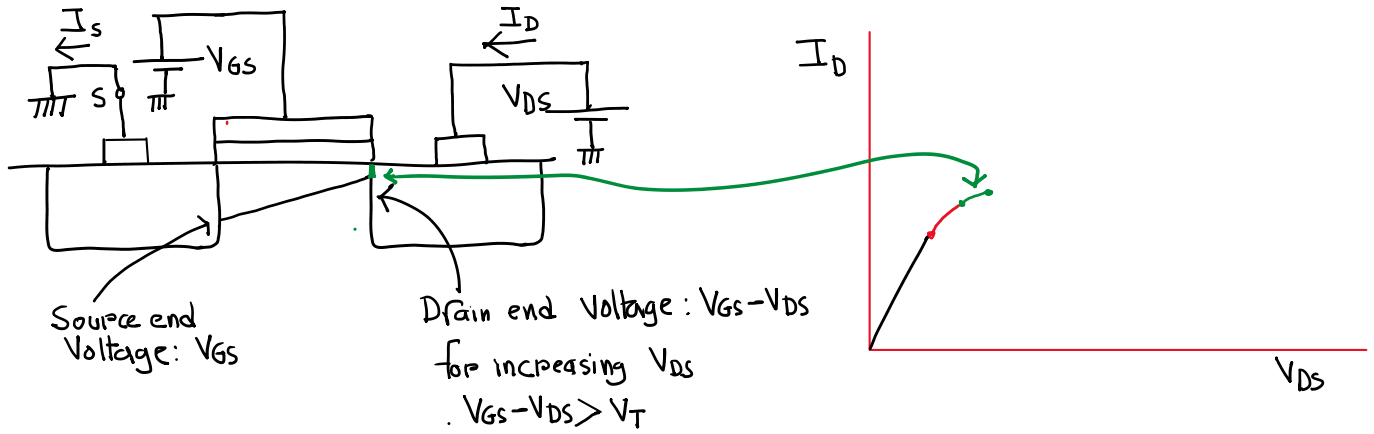
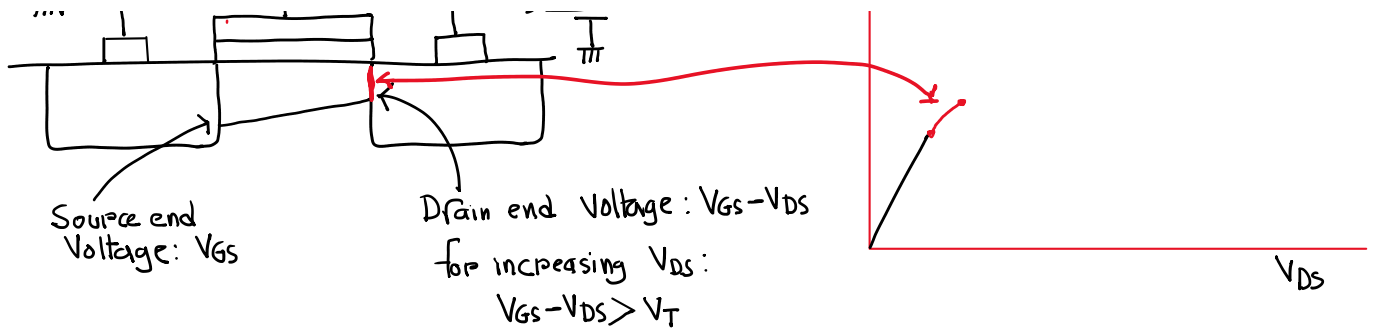


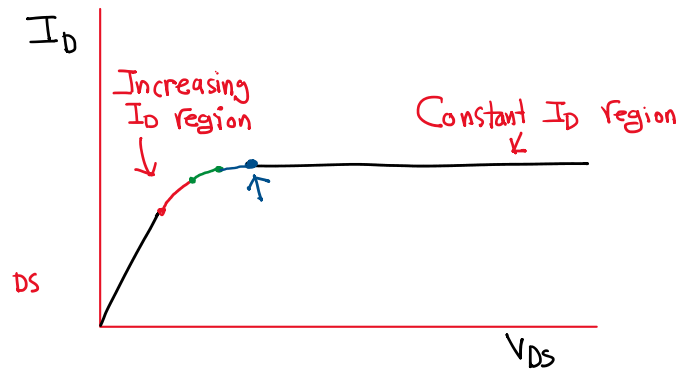
Source end Voltage: V_{GS}

Drain end Voltage: $V_{GS} - V_{DS}$
for small V_{DS} : $V_{GS} - V_{DS} \approx V_{GS}$



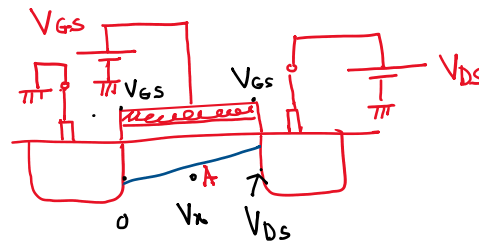
I_D





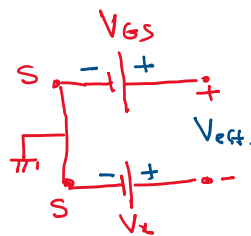
Increasing I_D region $\rightarrow V_{GS} - V_{DS} > V_T \rightarrow$ channel exists at drain end

Constant I_D region $\rightarrow V_{GS} - V_{DS} < V_T \rightarrow$ No channel exists at drain end



← Voltage V_{DS} drops along the channel, V_{DS} at drain end and 0 at source end.

lets consider, at position A the voltage along the channel is V_x , so the effective voltage betⁿ gate and position A. can be shown in the following way:



Applying KVL around the loop:

$$+V_{GS} - V_{eff} - V_x = 0$$

$$\Rightarrow \boxed{V_{eff} = V_{GS} - V_x}$$

at the source end: $V_x = 0$ [ground.] $\rightarrow V_{eff} = V_{GS} - 0 = V_{GS}$

at the drain end: $V_x = V_{DS} \rightarrow V_{eff} = V_{GS} - V_{DS}$

Since, channel depth $\propto V_{eff}$ [effective voltage betⁿ gate and ch.]

at source end: $V_{eff} = V_{GS} \uparrow$, ch. depth maximum (d_1)
 at drain end: $V_{eff} = (V_{GS} - V_{DS}) \downarrow$, ch. depth min. (d_2)

at source end: $V_{GS} = V_{GS}$ ↑, ch. depth maximum (d_1)
 at drain end $V_{GD} = (V_{GS} - V_{DS})$ ↓, ch. depth min. (d_2)

