EEE205L (Electronic Circuits I Laboratory)

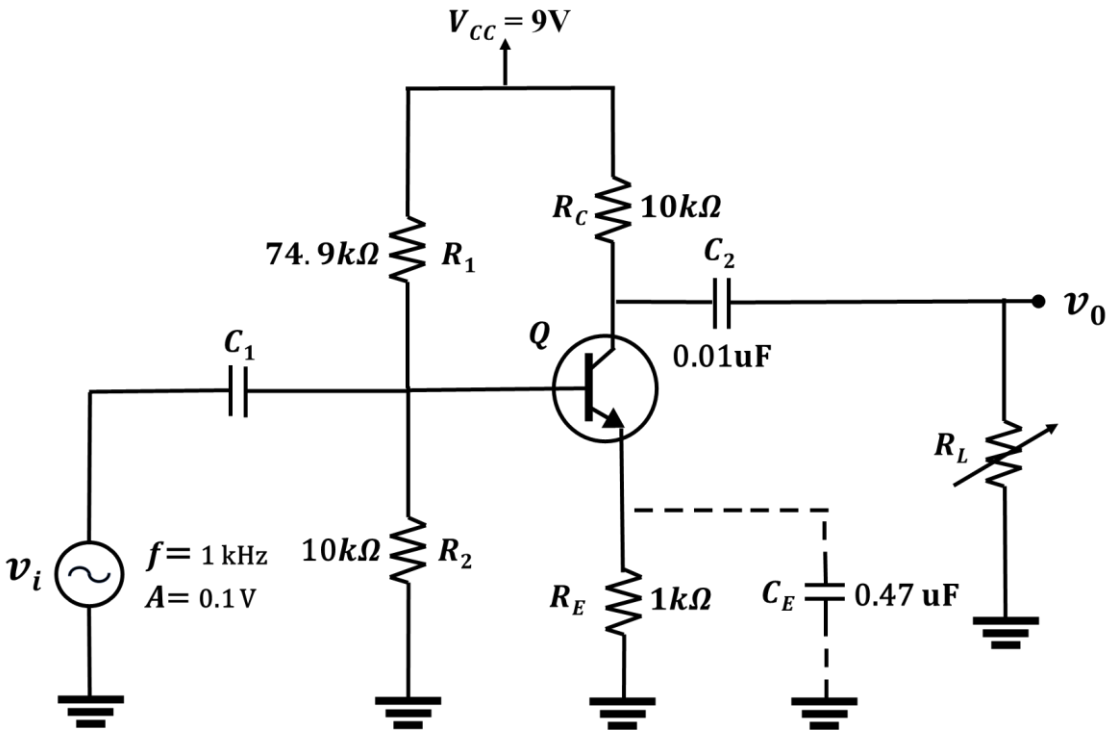
Department of EEE, Brac University

Open-Ended Problem

Marks: 60

Problem

The objective of this problem is to observe the effect of a load resistor on the gain of a BJT amplifier. Additionally, the problem looks into the impact of the presence and absence of an emitter bypass capacitor. Consider the following circuit.



Show the above figure in the report. Determine the coupling capacitance C_1 such that the lower cutoff frequency of the amplifier is 18 Hz. The problem involves software and hardware tasks.

Software Implementation

Use PSpice and Excel to find the effect of the load resistor on the amplifier's gain. Additionally, look into the impact of the presence and absence of the emitter bypass capacitor. Follow the steps below.

1. **Without the Emitter Bypass Capacitor**
    a. Set up the circuit using PSpice and show it in the report. Provide the screenshot of the transient and parametric analysis also.
    b. Vary the load resistance from 1 kΩ to 10 kΩ in steps of 0.5 kΩ. Plot a graph showing Gain vs. Time.

c. Plot a graph showing Gain vs. Load Resistance using Excel.

2. **With the Emitter Bypass Capacitor**

   a. Set up the circuit using PSpice and show it in the report. Provide the screenshot of the transient and parametric analysis also.
   b. Vary the load resistance from 1 kΩ to 10 kΩ in steps of 0.5 kΩ. Plot a graph showing Gain vs. Time.
   c. Plot a graph showing Gain vs. Load Resistance using Excel.

Hardware Implementation

Investigate the effect of the load resistor on the amplifier's gain. Additionally, look into the impact of the presence and absence of the emitter bypass capacitor. Follow the steps below.

1. **Without the Emitter Bypass Capacitor**

   a. Set up the circuit on a breadboard and show its picture in the report.
   b. Vary the load resistance from 1 kΩ to 10 kΩ in steps of 1 kΩ. Take necessary measurements to calculate the gain for each load resistance and show the data in a table.
   c. Plot a graph showing Gain vs. Load Resistance and interpret their relation.

2. **With the Emitter Bypass Capacitor**

   a. Set up the circuit on a breadboard and show its picture in the report.
   b. Vary the load resistance from 1 kΩ to 10 kΩ in steps of 1 kΩ. Take necessary measurements to calculate the gain for each load resistance and show the data in a table.
   c. Plot a graph showing Gain vs. Load Resistance and interpret their relation.

3. **Comparison**

   Synthesize the impact of the presence and absence of the emitter bypass capacitor on the gain of the amplifier.

4. **Troubleshooting**

   Detect mistakes occurred during the implementation, troubleshoot them and mention in the report.

Deliverables

1. A report (Google Docs)
2. Software files (.sch)

Marks Distribution

Criteria	Marks	KPI
Design	5	
Software 1. a. + 2. a.	5	e3
Software 1. b. + 2. b.	10	
Software 1. c. + 2. c.	10	
Hardware 1. a. + 2. a.	5	d1
Hardware 1. b. + 2. b.	10	d2
Hardware 1. c. + 2. c.	5	d4
Hardware 3.	5	d5
Hardware 4.	5	d3

Course Outcome Assessment Information

CO	CO Description	PO	Tool	KP	CEP / CEA
4	**Investigate** the effect of different circuit parameters including load resistance on the Amplifier performances in terms of Gain, input/output impedance, faithful reproducibility, stability in biasing etc.	d	Open-Ended Problem – Hardware Part	K8	P1, P3, P4
5	**Use** simulation tool to construct electronic circuits and simulate in schematic level	e	Open-Ended Problem – Software Part	K6	