Course Details	
Course Code	**EEE 283 (Section 5)**
Course Title	**Digital Logic Design**
Credit + Contact Hours	3+3 (CORE)
Prerequisites	EEE 205 Electronic Circuit I EEE 205L Electronic Circuit I Laboratory
Instructor	A K M **Anindya** Alam (B.Sc.), Lecturer, EEE
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Office Location	Desk 4E-C58 , Department of EEE, Level 4, BRAC University
Office Hours	**Saturday** (9:30 AM - 10:50 AM) **Sunday** (8:00 AM - 9:20 AM) [Please Email First!] **Tuesday**(11:00 AM -1:50 PM)

Course Outcomes (COs):

Sl.	CO Description	Assessment tools
CO1	**Apply** the concept of digital logic design to solve the problem using gates to replicate logic functions	Assignment, Quiz, Exam
CO2	**Analyze** combinational and sequential logic circuits built with various logic gates, flip-flops, registers, counters etc. represented through schematic diagram or hardware description language	Assignment, Quiz, Exam
CO3	**Design** combinational and sequential logic circuits using various logic gates, flip-flops, registers, counters as building blocks	Assignment, Project

Reference Books:

Title	Author(s)	Year	Edition	Publisher
Fundamentals of Digital Logic with Verilog Design	Stephen Brown & Zvonko Vranesic	2014	3rd Ed	McGraw Hill
Digital Systems: Principles & Applications	Neal S. Widmer, Gregory L. Moss & Ronald J. Tocci	2018	12th Ed	Pearson
Fundamentals of Logic Design	Charles H. Roth Jr., Larry L. Kinney & Eugene B. John	2019	7th Ed	Cengage
Digital Logic & Computer Design	M. Morris Mano	2004	4th Ed	Pearson

Course Outline:

1. **Fundamental Logic Gates:** Introduction to Digital Logic, Concept of Logic Gates, NOT Logic, AND Logic, OR Logic, Universal Logic Gates, NAND Logic, NOR Logic, XOR Logic, XNOR Logic, Logic Gate Network, NAND/NOR implementation, Cost of Logic Circuit.

2. **Boolean Algebra**: Boolean Operators, Logic Functions, Truth Table, DeMorgan's Theorem, Maxterms & Minterms, SOP vs. POS Logic, Karnaugh Map, Cost Minimization.

3. **Combinational Logic:** Multiplexer, Look-Up Table, Encoder, Decoder, Demultiplexer, Shannon's Expansion Theorem, Binary Coded Decimal, Seven Segment, Comparator.

4. **Binary Arithmetic:** Binary Number Representation, Carry Flag, Half Adder, Full Adder, Ripple Carry Adder, Binary Multiplication, Binary Negative Numbers, Adder-Subtractor Unit, Overflow Flag, Binary Coded Decimal Adder, Hexadecimal Number System.

5. **Sequential Logic:** Memory Circuits, S-R Latch, D Latch, Master-Slave Flip-Flop, D FlipFlop, T Flip-Flop, J-K Flip-Flop, Hold & Setup Time, Counter, Asynchronous vs. Synchronous Counter, Ring Counter, Johnson Counter, BCD Counter, Shift Register.

6. **Finite State Machines:** Moore and Mealy Implementation, Synchronous Finite State Machines, Logic Gate implementation.

7. **CMOS Implementation:** Introduction to CMOS technology, CMOS vs NMOS technology, Implementation of NOT, NAND and NOR logic gates, Implementation of AND, OR, XOR & XNOR Logic, Implementation of complex logic via NAND/NOR, Integrated Implementation of Complex Logic, Transmission Gates, Programmable Logic Array.

8. **Hardware Description Language:** Introduction to Verilog, Boolean Function in Verilog, Coding via Wire Command, Coding via Assign Command, Coding via Always Command, Blocking vs. Non-Blocking Procedure, Coding for Combinational vs Sequential Logic.

Tentative Course Plan:

Wk#	Topic
1	Review of Number Systems, Basic Binary Arithmetic (HSC/ O&A-level equivalent concepts
2	Fundamental Logic Gates
3	Boolean Algebra
4	Combinational Logic
5	Combinational Logic

Midweek	Mid-Term
6	Binary Arithmetic & **Project Proposal**
7	Binary Arithmetic
8	Sequential Logic
9	Sequential Logic
10	Finite State Machines
11	CMOS Implementation
12	Hardware Description Language & **Project Submission**
Finals Week	Final Exams

Tentative Assessment Plan:

- ***Quiz 1:*** *Fundamental Logic Gates & Boolean Algebra*
- ***Quiz 2:*** *Combinational Logic*
- ***Quiz 3:*** *Sequential Logic and FSM*
- ***Assignment 1:*** *Binary Arithmetic*
- ***Assignment 2:*** CMOS implementation and Verilog HDL

➢ ***Project:*** *Based on Proposals with Proteus Simulation*

❖ ***Midterm:*** *Fundamental Logic Gates, Boolean Algebra & Combinational Logic*

❖ ***Final:*** *Binary Arithmetic, Sequential Logic, FSM, CMOS Implementation & Verilog HDL*

Tentative Course Assessment:

Assessment Tools	Weightage (%)
Attendance	10
Quiz (Best 2 out of 3)	20
Assignment (2)	10
Project	15
Midterm Exam	20
Final Exam	25
Total	**100**