Arsh Sharma

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Education

- **National Institute of Technology** — Hamirpur, India
  B.Tech & M.Tech in Electronics and Communication Engineering(VLSI); Current GPA: 8.56 — *Aug 2018 - May 2023*
- **Mount Carmel School**
  12th - ISC; Percentage: 91% — *2018*
- **Mount Carmel School**
  10th - ICSE; Percentage: 93% — *2016*

Projects

- **Masters Dissertation**
  Studied the physical design flow from RTL(logic) to GDSII(layout).
  - Designed the datapath and ISA for the MIPS Single-Cycle CPU Architecture.
  - Planned a Julia based tool for the Analytical Placement method with an overall goal of improving the performance of Place & Route in mind.
  - Performed steps such as floorplanning, placement, routing etc. using tools like qflow, openroad etc. for various digital circuits.
- **Major Project**
  B.Tech - Group Project
  - Wrote a verilog Implementation of 8-Channel Cosine Modulated FIR Filter Banks for the Nexys 4 DDR FPGA board.
  - Used Xilinx vivado for high level synthesis.
  - Leveraged the DSP.jl package in Julia to generate the filter coefficients for the FIR filter banks.
- **Miscellaneous**
  Projects for self-learning
  - Designed FSM and HDL(verilog) implementation for adders, counters, memory, ALU etc.
  - Performed verification by writing testbench for the verilog modules.
  - High Level Synthesis of a 2nd order Differential Equation solver.
  - **IBMQJulia.jl** A set of scripts to parse Yao.jl based quantum circuits to the IBM-Quantum spec(actual quantum computers). Implemented the OpenQasm specifications paper composing two major units, the REST API and the Yao IR to QObj parser.

Skills

- **Languages:** Verilog(RTL Coding), System Verilog, Julia, Python, C/C++, Matlab, Shell scripting
- **Tools:** Physical Design flow tools from Cadence/Synopsys, GTKWave, Quartus, Linux, GIT(Version Control), ArduinoIDE, VSCode
- **Interests:** ASIC Design Flow, Verification Techniques, FPGAs, TCL(Tool command language), Digital Electronics, Computer Architecture

Professional Experience

- **Zellerfeld R&D GmbH** — Hamburg, Germany
  Intern
  - Developed tools in Python & Julia Language to support processing, slicing and GCODE generation of complex footwear 3D models and a backend to expose the tooling for a no-code interface.
  - Wrote scripts using FFMPEG for realtime video monitoring and analysis of the 3D printers including the overall print process.

Side Quests

- **Speaker at ECEConnect 2022:** Gave a talk on software development and open-source software in the context of Electrical Engineering.
- **Speaker at JuliaCon 2021:** Presented my work on Javis.jl to a global community of Julia enthusiasts, developers, scientists and industry. Link to the talk