

# Arsh Sharma

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## EDUCATION

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### National Institute of Technology(NIT) Hamirpur

*Integrated B.Tech & M.Tech in Electronics and Communication Engineering(VLSI)*

*CGPI: 8.56/10*

### Mount Carmel School

*12th(High School) - ISC; Percentage: 91%*

## EXPERIENCE

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### NVIDIA

*ASIC Engineer*

- Ownership of power controller modeling that keeps products within power budget - AI/server/desktop GPUs
  - Developed test and validation plans for hardware bring-up, post-silicon performance validation of the model.
  - Designed automation frameworks (Python, Shell) for power measurement, data collection, regression-based modeling.
  - Calibrated the models keeping clock gating, power states, voltage-frequency scaling in mind.
  - Collaborated with architects, pre-silicon design and software teams to define and achieve Pnp Targets
  - Hardware setup on Linux/Windows and Ground truth comparison using DAQ/on-board sensors
  - Perform regular exploratory studies/experiments:
    - PM signals analysis for benchmark/workload-specific(DL/ML/LLM) activity patterns
    - Performed post-silicon power/performance debug and correlation, deriving accuracy metrics for models
    - Provided feedback to architects, design and software teams regarding methodology improvements
  - Supervised a group of contractors/lab technicians to assist with silicon bring-up
- Contributed to the open-source DAQ library maintained by Ni.
- Automated the flows for power, temperature measurement and data collection for NVIDIA's In-System Test architecture(DFT hardware) to leverage power as a service for internal users.

### Zellerfeld R&D GmbH

*Hamburg, Germany*

*Software Developer*

- Developed tools to support feed measurement, processing and GCODE generation for state-of-the-art 3D printers
- Created a backend with user authentication, database etc. to expose a slicing tool for a no-code interface.
- Wrote scripts using FFMPEG for realtime video monitoring and analysis of the 3D printers including the overall print process.

## PROJECTS

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### CPU Performance Modeling, Analysis & Optimization

*Implemented simple Matrix Mul code(C++) with focus on CPU architecture based optimization*

- Optimized the code based on cache-aware memory access patterns and used SIMD-vectorized matrix multiplication to improve runtime
- Conducted performance profiling using AMD uProf to analyze cache hit/miss rates, memory bandwidth, and CPU pipeline utilization

### Cache Modeling

*Implemented the functional model of a n-way set associative cache using C++ and OOP concepts*

- Added support for large trace parsing, inclusivity, prefetching and reporting key performance metrics. [Blog link](#)

## ACHIEVEMENTS & SIDE QUESTS

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- **Speaker at JuliaCon 2021:** Presented the GSoC work on Javis.jl to a global community of **1 million+** Julia enthusiasts, developers, scientists and industry. [Link to the talk](#)
- **Skills & Interests:** Computer Architecture, Performance Analysis, Cache/Interconnect/Memory Subsystems, Modeling, RTL, Python, C++, Julia, Shell, Open-Source Software