Lab 5 – Modulo-n Counters

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March 2, 2021

Code:

```
/*
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   This code will incremented count up if ONLY up is asserted, decrement count down
   if ONLY down is asserted. Count will be set to 0 if up and down are BOTH asserted.
   If neither are asserted count will not change.



*/

module modncount

       (
       input logic up, down, clock,       // up/down controls, cloc,
       output logic [3:0] count,          // modulo-n count value
        output logic carry, borrow         // carry/borrow
        ) ;

        // my solution is here

       logic [3:0] count_next ;

       assign carry =
           (count == 4'd4 && up )&& !down ? '1 :
           (count == '0 && !up )&& down ? '0 :
           up && down ? '1 : '0 ;

       assign borrow =
           (count == 4'd4 && up) && !down ? '0 :
           (count == '0 && !up) && down ? '1 :
           up && down ? '1 : '0 ;

       always_ff@(posedge clock) count = count_next ;

       assign count_next =
           !up && !down ? count :
           up && !down ? (count == 4'd4 ? 4'b0000 : count + 1'b1 ) :
           down && !up ? (count == 4'b0000 ? 4'd4 : count - 1'b1 ) :
           '0 ;
```
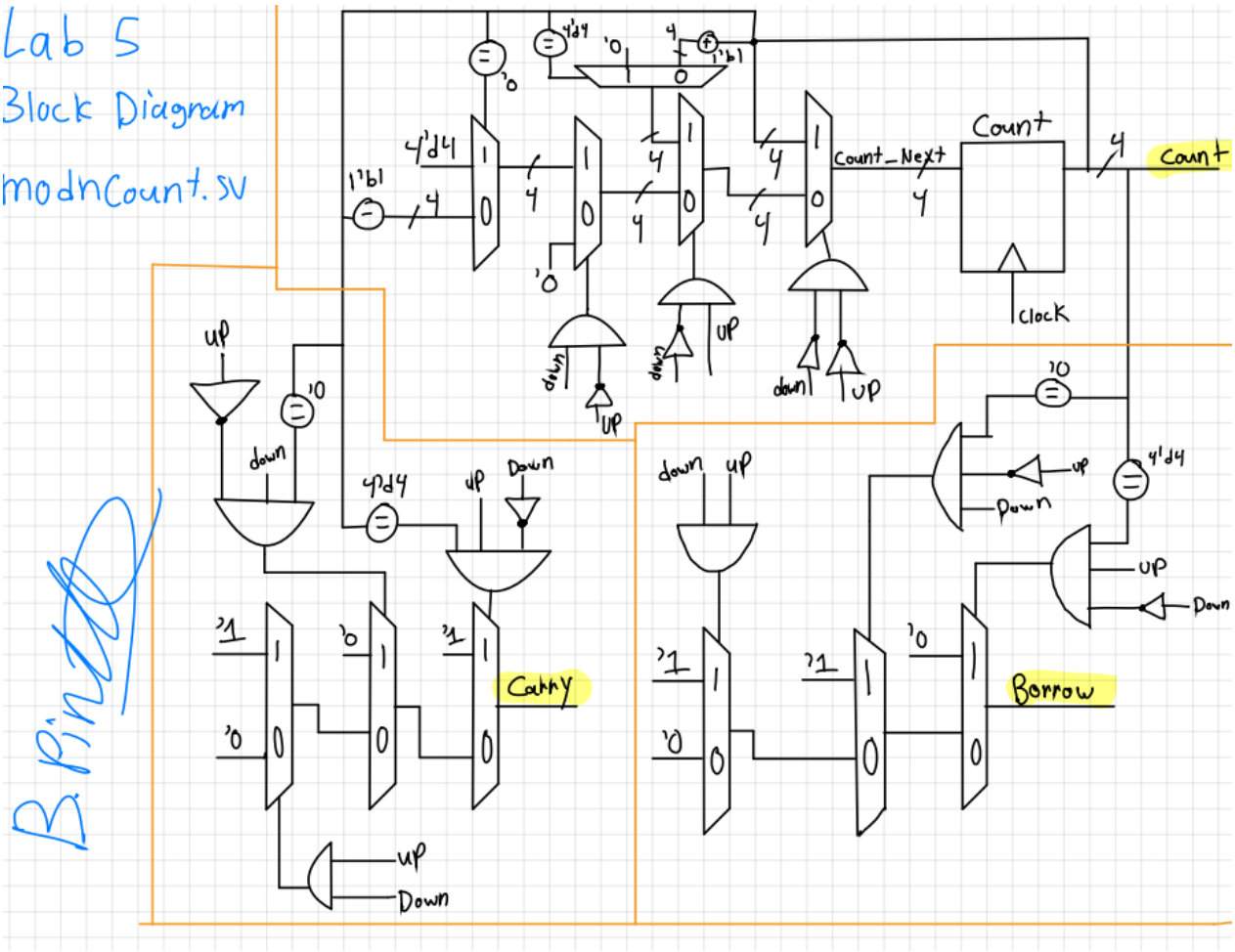

```
endmodule
```

Block Diagram:



Compilation Report:

dncount.sv | Compilation Report - lab5

Flow Summary

<<Filter>>

Flow Status	Successful - Tue Mar 02 19:05:00 2021
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	lab5
Top-level Entity Name	lab5
Family	MAX II
Device	EPM240T100C5
Timing Models	Final
Total logic elements	146 / 240 (61 %)
Total pins	15 / 80 (19 %)
Total virtual pins	0
UFM blocks	0 / 1 (0 %)

RTL: