ELEX – 2117

Lab 1 - Combinational Logic Design with Verilog

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January 27, 2021

```
/*
    Brennan Pinette
    January 27th 2021
    Lab1.sv

    This code will display 4 digits, the last
    4 digits of my student number, 1 digit at a time.
    The digit displayed will depend on the 2 bit
    combination logic inputs. The digits will be
displayed
    on a 4 display 7 segement LED. Each digit
    will illuminated on a different display.

*/


module Lab1 (

    input logic [1:0]x,
    output logic e, d, dp, c, g, b, f, a,
    output logic [3:0] en ) ;

    assign {en,a,b,c,d,e,f,g} =

    x == 2'b11 ? {4'b1000,7'h06} : ( x == 2'b10 ?
{4'b0100,7'h04} :
    ( x == 2'b01 ? {4'b0010,7'h12} : {4'b0001,7'h01}
) ) ;

endmodule
```

Compilation Report - Lab1

Flow Summary

<<Filter>>

Flow Status	Successful - Wed Jan 27 11:10:47 2021
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	Lab1
Top-level Entity Name	Lab1
Family	MAX II
Device	EPM240T100C5
Timing Models	Final
Total logic elements	4 / 240 (2 %)
Total pins	14 / 80 (18 %)
Total virtual pins	0
UFM blocks	0 / 1 (0 %)