ELEX – 2117

Lab 2 - Sequential Logic Design with Verilog

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A01073920

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Code

```
module lab2

    /*
      lab2.sv
      Displays successive digtis of my BCIT ID A01073920,
    staying on the last digit because it is even.
    Brennan Pinette, 2021-02-3

    */

    (
    input logic reset_n, clock_in, clock50,
    output logic a, b, c, d, e, f, g, dp,
    output logic [3:0]en ) ;

    logic clock;
    logic [2:0] digit_next, digit=0;

    assign digit_next //adder
    = reset_n ?  (digit == 3'b111 ? 3'b111 : digit+1'b1) : 1'b0 ;

    debounce debounce0 ( clock_in, clock50, clock );

    always_ff @(posedge clock) digit = digit_next ; //flip flop

    assign {en,a,b,c,d,e,f,g} = //PLD display

    digit == 3'b000 ? {4'b1000,7'h01} :
    digit == 3'b001 ? {4'b0100,7'h4f} :
    digit == 3'b010 ? {4'b0010,7'h01} :
    digit == 3'b011 ? {4'b0001,7'h0f} :
    digit == 3'b100 ? {4'b1000,7'h06} :
    digit == 3'b101 ? {4'b0100,7'h04} :
    digit == 3'b110 ? {4'b0010,7'h12} :
    {4'b0001,7'h01} ;

endmodule
```

Compilation Report and Diagram

Compilation Report - lab2

Flow Summary

<<Filter>>

Flow Status	Successful - Wed Feb 03 13:23:03 2021
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	lab2
Top-level Entity Name	lab2
Family	MAX II
Device	EPM240T100C5
Timing Models	Final
Total logic elements	51 / 240 (21 %)
Total pins	15 / 80 (19 %)
Total virtual pins	0
UFM blocks	0 / 1 (0 %)