

ELEX 2117

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Lab 4 – Multiplexed Display

Code:

```
module lab4
(
    input logic clock,
    output logic a, b, c, d, e, f, g, test,
    output logic [3:0]en
);

    logic [19:0] count, count_next, n ;
    logic [1:0] digit, digit_next ;

    assign n = 20'h196E4 ;

    always_ff @(posedge clock) count = count_next ;

    always_ff @(posedge clock) digit = digit_next ;

    assign count_next =
    count ? count - 1 : n - 1 ;

    assign digit_next =
    count ? digit :
    digit == 2'b11 ? 0 : digit + 1 ;

    assign {en, a, b, c, d, e, f, g} =

    digit == 2'b01 ? { 4'b0001, 7'h01} : // 0
    digit == 2'b10 ? { 4'b0010, 7'h12} : // 2
    digit == 2'b11 ? { 4'b0100, 7'h04} : // 9
    { 4'b1000, 7'h06} ; // 3

endmodule
```

Math:

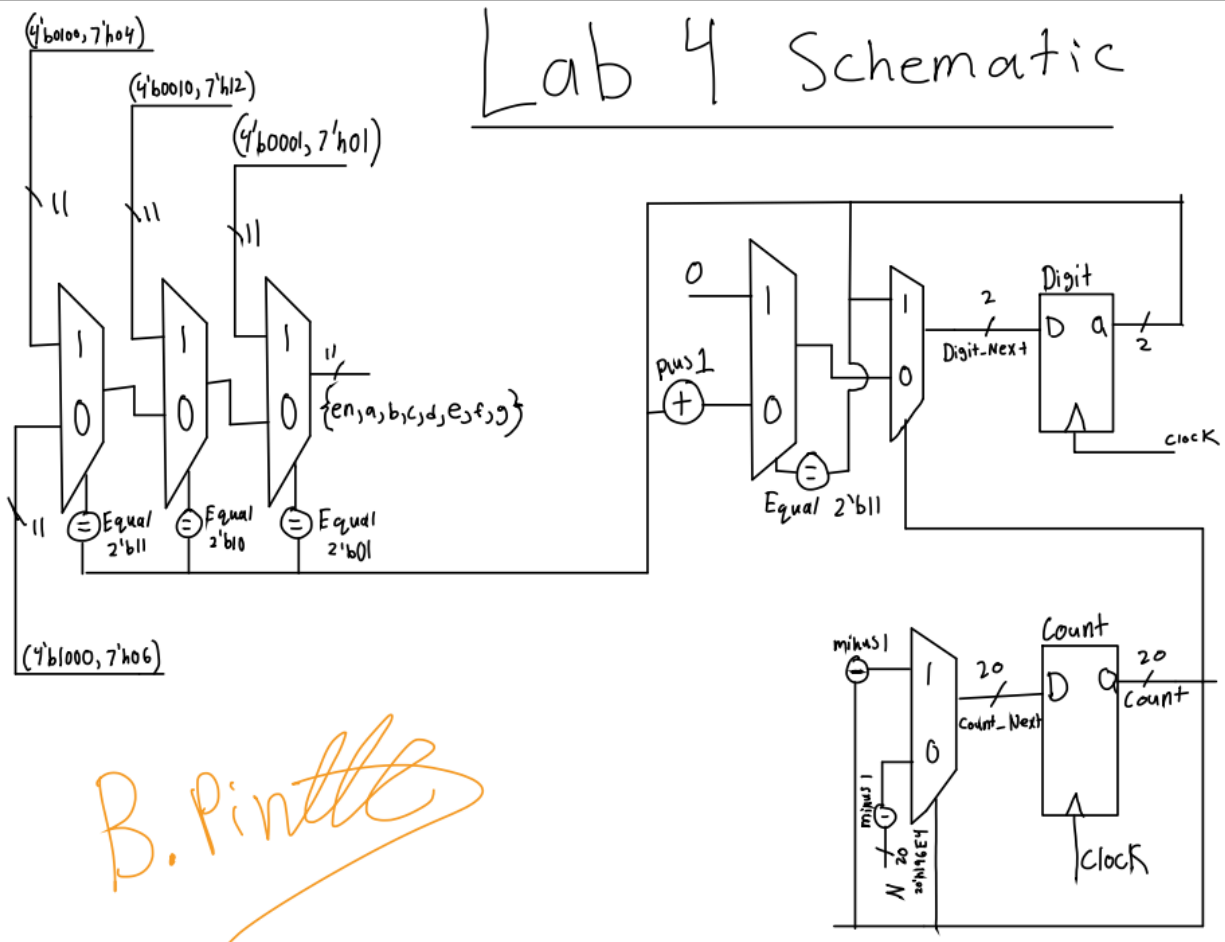
Clock Divider

$$\frac{50 * 10^6}{4 * (100 + 20)} = 104167$$

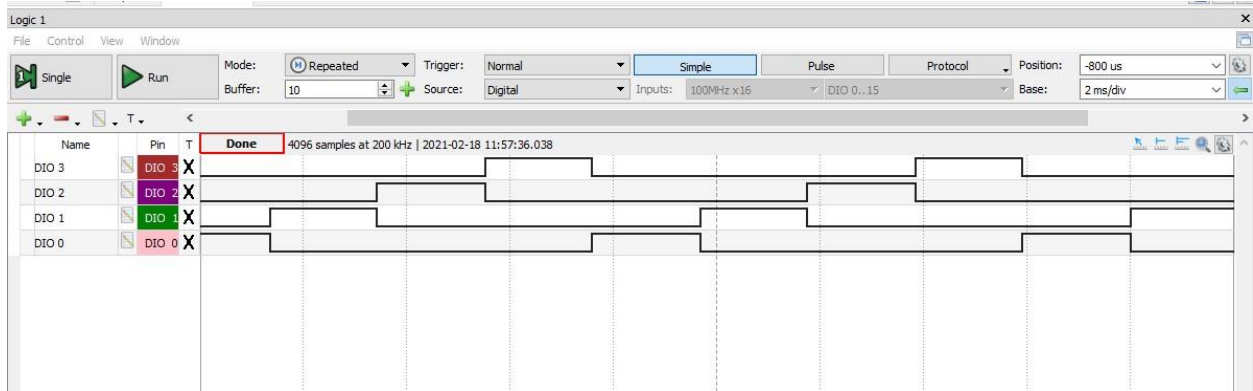
EN Sequence:

4'b1000 (EN[3]) -> 4'b0001 (EN[0]) -> 4'b0010 (EN[1]) -> 4'b0100 (EN[2])

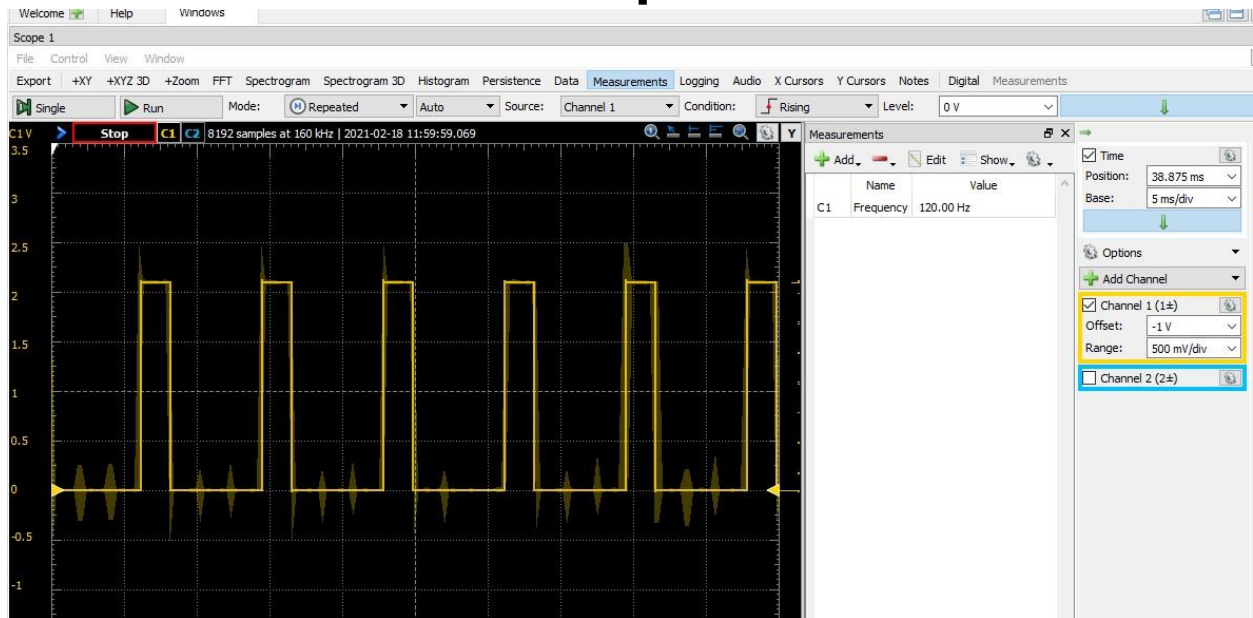
Block Diagram:



Logic Sequence:



Scope:



Compilation Report:

Flow Summary	
<<Filter>>	
Flow Status	Successful - Sun Feb 21 16:10:22 2021
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	lab4
Top-level Entity Name	lab4
Family	MAX II
Device	EPM240T100C5
Timing Models	Final
Total logic elements	48 / 240 (20 %)
Total pins	13 / 80 (16 %)
Total virtual pins	0
UFM blocks	0 / 1 (0 %)

Photo of Breadboard:

