

ELEX 2117

Lab 7 –
Asynchronous Serial Interface

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March 21, 2021

A01073920

Code:

```
/* Brennan Pinette
   March 21, 2021

   Purpose: This program will send my BCIT number serially.
*/

module uart
( input logic clk, reset_n,
  input logic nextbit, nextchr,
  input logic [7:0] char,
  output logic txd ) ;

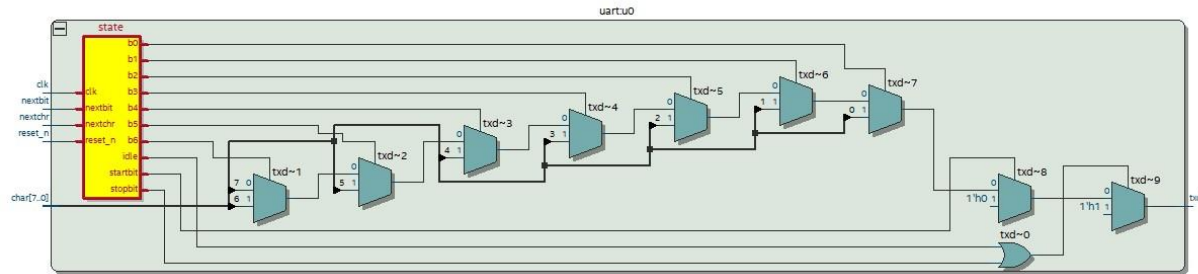
  typedef enum int unsigned
    { idle, startbit, b0, b1, b2, b3, b4, b5, b6, b7, stopbit } state_t ;
  state_t state = idle, state_next ;

  always_ff@(posedge clk) state = state_next ;

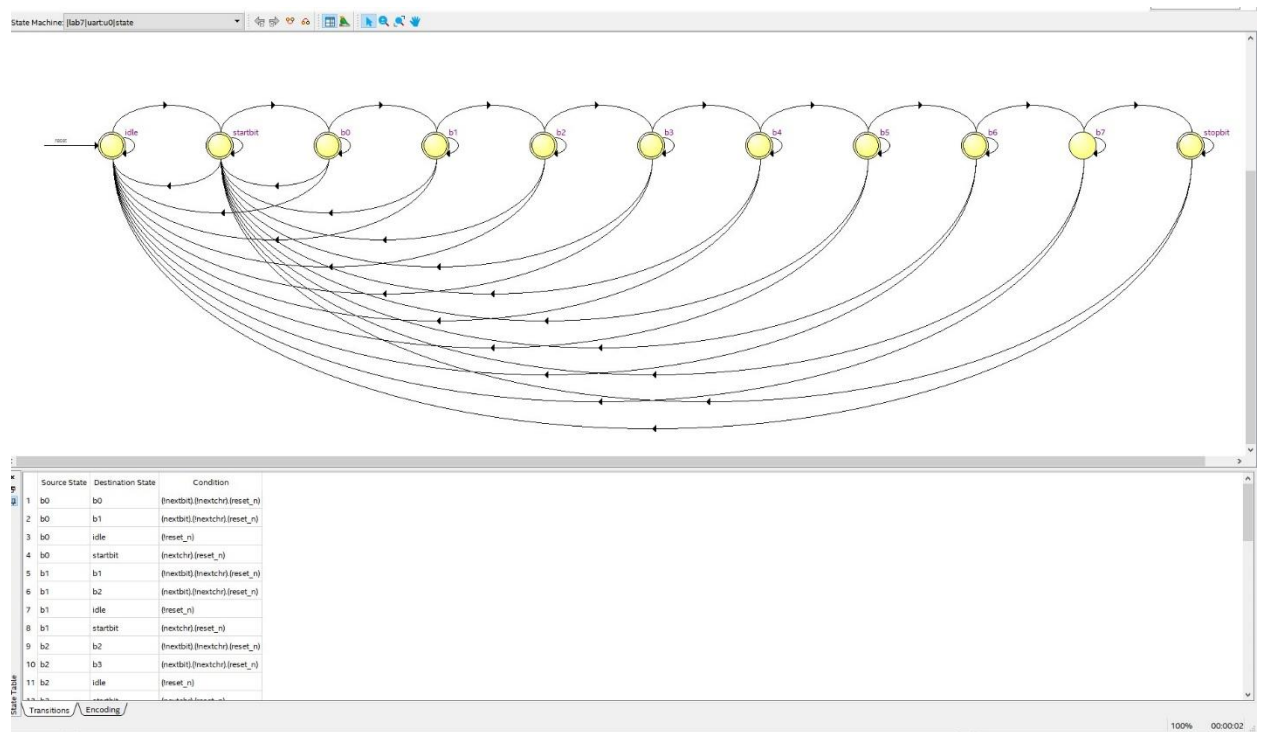
  assign state_next =
    !reset_n ? idle :
    nextchr ? startbit :
    nextbit ?
      (
        state == startbit ? b0 :
        state == b0 ? b1 :
        state == b1 ? b2 :
        state == b2 ? b3 :
        state == b3 ? b4 :
        state == b4 ? b5 :
        state == b5 ? b6 :
        state == b6 ? b7 :
        state == b7 ? stopbit :
        state
      ) :
    state ;

  assign txd =
    state == idle || state == stopbit ? 1 :
    state == startbit ? 0 :
    state == b0 ? char[0] :
    state == b1 ? char[1] :
    state == b2 ? char[2] :
    state == b3 ? char[3] :
    state == b4 ? char[4] :
    state == b5 ? char[5] :
    state == b6 ? char[6] :
    char[7] ;
endmodule
```

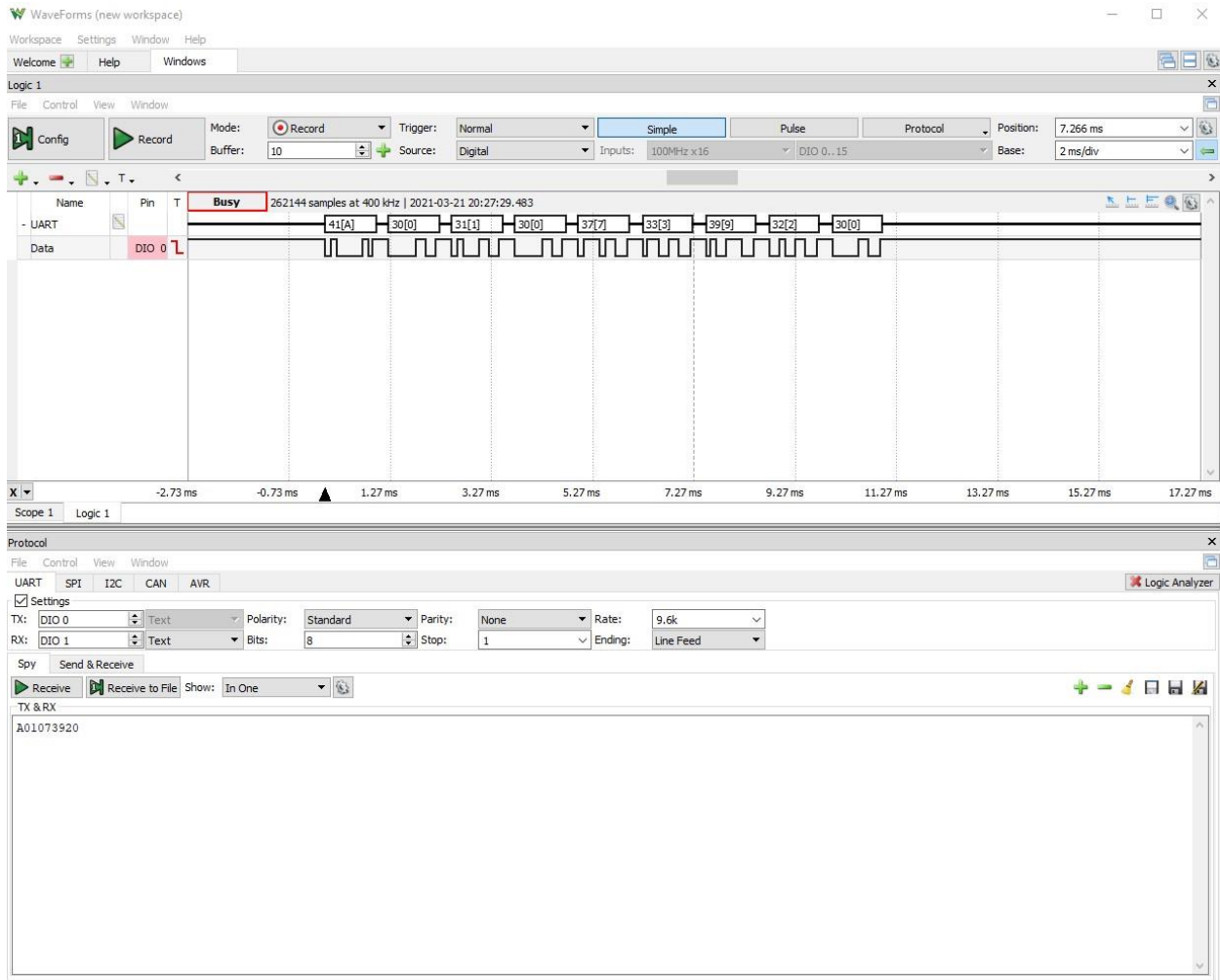
RTL:



State Transition:



Logic Analyzer:



Compilation Report:

Flow Summary	
<<Filter>>	
Flow Status	Successful - Sun Mar 21 20:27:01 2021
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	lab7
Top-level Entity Name	lab7
Family	MAX II
Device	EPM240T100C5
Timing Models	Final
Total logic elements	123 / 240 (51 %)
Total pins	3 / 80 (4 %)
Total virtual pins	0
UFM blocks	0 / 1 (0 %)