ELEX – 2117

Lab 3 – Timers and Frequency Dividers

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```
module lab3
	/*
	lab2.sv

	This program will produce a sound
	at a frequency determined by my student ID

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	right 500hz - N = 50000
	left 700hz - N = 35714
	both 1400hz - N = 17857

	*/

	(
	input logic [1:0]x,
	input logic clk50,
	output logic speaker ) ;

	logic timeout, timeout_next, stop ;
	logic [15:0]count, count_next, N ;


	assign count_next =
	stop ? N - 1 :
	count ? count - 1 : N - 1 ;

	assign stop =
	x == 2'b11 ? '1 : '0 ;

	always_ff @(posedge clk50) count = count_next ;

	assign N =
	x == 2'b10 ? 16'hC350 :
	x == 2'b01 ? 16'h8B82 :
	16'h45C1 ;

	assign timeout_next =
	stop ? '0 :
	count ? timeout :
	timeout ? '0 : '1 ;

	always_ff @(posedge clk50) timeout = timeout_next ;

	assign speaker = timeout;

endmodule
```
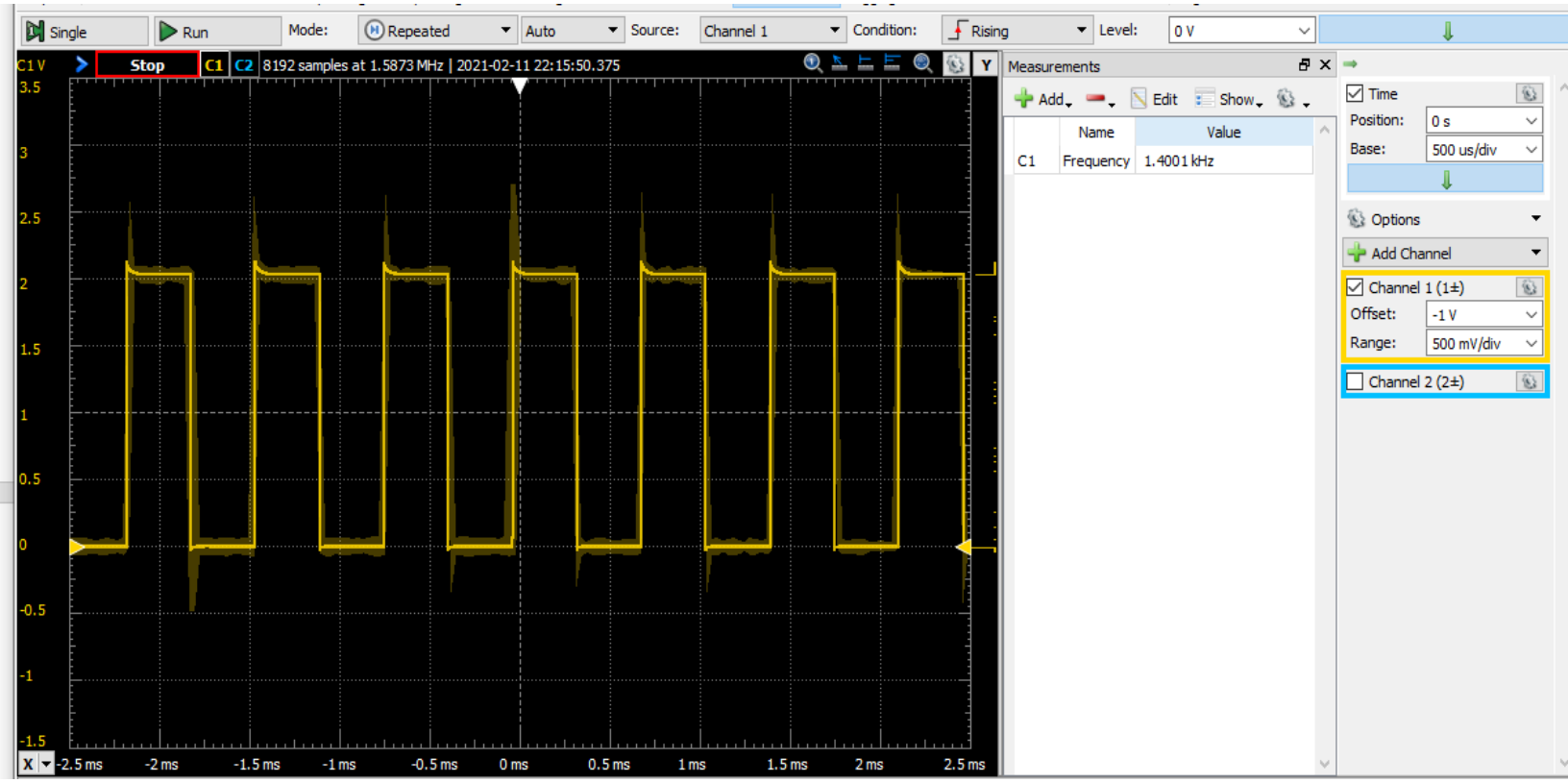

Compilation Report - lab3

Flow Summary

<<Filter>>

Flow Status	Successful - Thu Feb 11 22:03:38 2021
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	lab3
Top-level Entity Name	lab3
Family	MAX II
Device	EPM240T100C5
Timing Models	Final
Total logic elements	46 / 240 (19 %)
Total pins	4 / 80 (5 %)
Total virtual pins	0
UFM blocks	0 / 1 (0 %)


Single
Run
Mode:
Repeated
Auto
Source:
Channel 1
Condition:
Rising
Level:
0 V
Stop
C1
C2
8192 samples at 1.5873 MHz | 2021-02-11 22:15:50.375
C1 V
3.5
3
2.5
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2.5 ms
-2 ms
-1.5 ms
-1 ms
-0.5 ms
0 ms
0.5 ms
1 ms
1.5 ms
2 ms
2.5 ms
Measurements
Add
Edit
Show
Name
Value
C1
Frequency
1.4001 kHz
Time
Position:
0 s
Base:
500 us/div
Options
Add Channel
Channel 1 (1±)
Offset:
-1 V
Range:
500 mV/div
Channel 2 (2±)