

The RHEA- Λ Reversible Gate Family: A Multi-Radix Binary–Ternary–Pentary Cell for Hamiltonian Symbolic Computation in the RHEA-UCM Framework

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Abstract

This paper introduces the *RHEA- Λ* family of reversible multi-radix logic gates developed for the RHEA-UCM (Recursive Homeostatic Evolutionary Algorithm – Universal Cell Model) symbolic computation framework. A single physical gate topology supports binary, ternary, and pentary modes, with a 3-bit glyph/entropy register enabling local symbolic memory and internal phase evolution. In higher-radix modes the transitions form strictly bijective, triangular maps over $\mathbb{Z}_3 \times \mathbb{Z}_3 \times \mathbb{Z}_5$ and \mathbb{Z}_5^3 , providing discrete Hamiltonian, measure-preserving dynamics aligned with the RHEA-UCM entropy model. Binary mode retains CMOS drop-in compatibility for hybrid reversible–irreversible scheduling under the Lorenz entropy controller. A full mathematical specification, inverse mappings, commutative diagrams, truth tables, and verification code are provided.

1 Introduction

Reversible computation provides the only known mechanism for computation consistent with the thermodynamic requirement that information erasure produces irreducible heat via $kT \ln 2$. The RHEA-UCM framework embeds symbolic recursion into Hamiltonian dynamics, ensuring divergence-free computation except at explicitly scheduled entropy events.

To bridge theory to hardware, a unified reversible computational cell is required. The RHEA- Λ gate introduced here satisfies four constraints:

1. Binary behavior for CMOS compatibility.
2. Reversible ternary operations over \mathbb{Z}_3 .
3. Reversible pentary operations over \mathbb{Z}_5 .
4. Local glyph/entropy register supporting RHEA symbolic memory.

This produces the first reversible gate topology explicitly aligned with RHEA-UCM symbolic Hamiltonian flows.

2 Definition of the RHEA- Λ Gate Family

The gate processes a triple (A, B, G) where:

A, B are operands, G is a glyph/entropy register.

A mode parameter $M \in \{00, 01, 10\}$ selects:

$$\begin{cases} M = 00 & \text{Binary irreversible face (CMOS)} \\ M = 01 & \text{Ternary reversible face } (\mathbb{Z}_3 \times \mathbb{Z}_3 \times \mathbb{Z}_5) \\ M = 10 & \text{Pentary reversible face } (\mathbb{Z}_5^3) \end{cases}$$

3 Binary Λ_2 Gate

Define the reversible binary operator:

$$A' = A, \quad B' = A \oplus B, \quad G' = G \oplus B.$$

Inverse:

$$A = A', \quad B = A' \oplus B', \quad G = G' \oplus B.$$

Truth table is included in Table 1.

A	B	G	A'	B'	G'
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Table 1: Truth table of the RHEA- Λ_2 gate.

4 Ternary Λ_3 Gate

For $A, B \in \mathbb{Z}_3$ and $G \in \mathbb{Z}_5$:

$$A' = A, \quad B' = (B + A) \bmod 3, \quad G' = (G + B) \bmod 5.$$

Inverse:

$$A = A', \quad B = (B' - A') \bmod 3, \quad G = (G' - B) \bmod 5.$$

$$\begin{array}{ccc} (A, B, G) & \xrightarrow{\Lambda_3} & (A', B', G') \\ & \searrow & \\ & & (A', (B' - A') \bmod 3, (G' - B) \bmod 5) \end{array}$$

5 Pentary Λ_5 Gate

For $A, B, G \in \mathbb{Z}_5$:

$$A' = A, \quad B' = (B + A) \bmod 5, \quad G' = (G + B) \bmod 5.$$

Inverse:

$$A = A', \quad B = (B' - A') \bmod 5, \quad G = (G' - B) \bmod 5.$$

6 Hamiltonian Interpretation

All Λ gates are triangular, so their Jacobian determinant is:

$$\det D\Lambda = 1.$$

Thus they are finite-state analogues of discretized symplectic maps. Binary mode corresponds to explicitly scheduled entropy release.

7 Python Reversibility Verification

```
def ternary_step(A,B,G): return A,(B+A)%3,(G+B)%5
def pentary_step(A,B,G): return A,(B+A)%5,(G+B)%5
def check(step,dom):
    seen={}
    for A in range(dom[0]):
        for B in range(dom[1]):
            for G in range(dom[2]):
                out=step(A,B,G)
                if out in seen: print("Collision:",out); return
                seen[out]=(A,B,G)
    print("Bijective over",len(seen),"states.")
```

8 Conclusion

The RHEA- Λ family provides a unifying reversible gate topology that is multi-radix, strictly bijective, Hamiltonian-compatible, and ready for implementation across CMOS or emerging reversible technologies.

References

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