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A Reversible Multi-Radix Computational Cell 2 for Hamiltonian Symbolic Processing in the 3 RHEA-UCM Framework

4

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5

Abstract

6 We introduce a reversible multi-radix computational gate designed for integration into the
7 RHEA-UCM (Recursive Homeostatic Evolutionary Algorithm – Universal Cell Model) frame-
8 work. The construction provides a single hardware-level cell that dynamically supports bi-
9 nary, ternary, and pentary symbolic arithmetic under a unified reversible mapping. In binary
10 mode the cell behaves as a standard irreversible CMOS-compatible gate for drop-in usability;
11 in higher-radix modes it implements strictly bijective operators over finite state spaces, en-
12 abling zero-erasure computation consistent with Hamiltonian dynamics and Landauer–Bennett
13 thermodynamic bounds.

14 We present: (1) the conceptual RHEA-UCM gate behavior, (2) formal reversible mappings
15 on $\mathbb{Z}_3 \times \mathbb{Z}_3 \times \mathbb{Z}_5$ and \mathbb{Z}_5^3 , (3) proofs of bijectivity using triangular embeddings, (4) a behavioral
16 Verilog specification suitable for synthesis and hardware exploration, and (5) a Python-based
17 reversibility checker for exhaustive verification. This cell forms a concrete substrate for future
18 RHEA-IC designs, enabling Hamiltonian, measure-preserving symbolic transformations atop
19 CMOS-compatible reversible primitives such as Z.E.L.-class devices.

20

1 Introduction

21 Reversible computation provides the only thermodynamically admissible route toward large-scale,
22 ultra-low-dissipation digital systems. Following Landauer, the destruction of information is the
23 sole operation with a fundamental energy cost. Bennett showed that logically reversible mappings
24 incur no such penalty.

25 In the RHEA-UCM framework, symbolic recursion rules are embedded into divergence-free,
26 measure-preserving Hamiltonian flows. Irreversible events must therefore be isolated, scheduled, or
27 clustered using Lorenz-type entropy modulators.

28 A missing component has been a unified computational cell that simultaneously:

- 29
- behaves as a CMOS-compatible binary gate,

30

 - supports reversible ternary arithmetic over \mathbb{Z}_3 ,

31

 - supports reversible pentary arithmetic over \mathbb{Z}_5 ,

- 32 • maintains a local symbolic/entropy register, and
 33 • guarantees strict bijectivity in all non-binary modes.

34 The present work introduces such a cell.

35 2 A Multi-Radix Reversible RHEA-UCM Cell

36 We define a computational cell with inputs A, B , an internal register G , and a mode selector
 37 $M \in \{00, 01, 10\}$ governing binary, ternary, or pentary operation:

Mode M	Domain	Behavior
00	$\{0, 1\}$	Binary irreversible (e.g., NAND)
01	$\mathbb{Z}_3 \times \mathbb{Z}_3 \times \mathbb{Z}_5$	Fully reversible
10	\mathbb{Z}_5^3	Fully reversible

39 Binary mode ensures drop-in CMOS compatibility. The higher-radix modes implement Hamiltonian-
 40 like reversible transformations suitable for symbolic recursion, entropy tracking, and glyptic mod-
 41 ulation.

42 3 Reversible Mappings

43 3.1 Ternary Core on $\mathbb{Z}_3 \times \mathbb{Z}_3 \times \mathbb{Z}_5$

44 Let

$$45 \quad A, B \in \{0, 1, 2\}, \quad G \in \{0, 1, 2, 3, 4\}.$$

46 Define the forward map:

$$47 \quad A' = A, \tag{1}$$

$$48 \quad B' = (B + A) \bmod 3, \tag{2}$$

$$49 \quad G' = (G + B) \bmod 5. \tag{3}$$

50 **Invertibility.** Given (A', B', G') :

$$51 \quad A = A', \tag{4}$$

$$52 \quad B = (B' - A') \bmod 3, \tag{5}$$

$$53 \quad G = (G' - B) \bmod 5. \tag{6}$$

54 Because the system is triangular, bijectivity is immediate. Thus the map is a permutation of
 55 the 45-state domain.

56 **3.2 Pentary Core on \mathbb{Z}_5^3**

57 Let

58 $A, B, G \in \{0, 1, 2, 3, 4\}.$

59 Forward:

60 $A' = A,$ (7)

61 $B' = (B + A) \bmod 5,$ (8)

62 $G' = (G + B) \bmod 5.$ (9)

63 Inverse:

64 $A = A',$ (10)

65 $B = (B' - A') \bmod 5,$ (11)

66 $G = (G' - B) \bmod 5.$ (12)

67 Again the triangular structure guarantees bijectivity.

68 **4 Hamiltonian Interpretation within RHEA-UCM**

69 The ternary/pentary reversible mappings serve as discrete analogues of:

- 70 • divergence-free vector fields,
71 • symplectic transformations,
72 • measure-preserving Hamiltonian flows.

73 In the RHEA-UCM architecture:

- 74 • A, B encode symbolic operands (the Ψ and Φ channels),
75 • G encodes local glyph/entropy/trust phase,
76 • the reversible core enforces zero-erasure dynamics,
77 • the Lorenz scheduler determines when binary mode may be entered to cluster entropy.

78 Thus the reversible cell forms a discrete Hamiltonian unit in the UCM sense.

79 **5 Behavioral Verilog Specification**

```
80 // =====
81 // RHEA-UCM Reversible Gate (Binary / Ternary / Pentary)
82 // =====
83 module rheas_reversible_gate #((
84     parameter DATA_WIDTH_BIN = 1
85 ))
```

```

86     input wire [1:0] mode,      // 00=binary, 01=ternary, 10=pentary
87     input wire [2:0] A_in,
88     input wire [2:0] B_in,
89     input wire [2:0] G_in,
90     output reg [2:0] A_out,
91     output reg [2:0] B_out,
92     output reg [2:0] G_out
93   );
94
95 // mod-3 arithmetic
96 function [1:0] add_mod3;
97   input [1:0] x, y;
98   reg [2:0] s;
99 begin
100   s = x + y;
101   add_mod3 = (s >= 3) ? s - 3 : s[1:0];
102 end
103 endfunction
104
105 // mod-5 arithmetic
106 function [2:0] add_mod5;
107   input [2:0] x, y;
108   reg [3:0] s;
109 begin
110   s = x + y;
111   add_mod5 = (s >= 5) ? s - 5 : s[2:0];
112 end
113 endfunction
114
115 always @* begin
116   case (mode)
117     2'b00: begin
118       A_out = {2'b00, ~(A_in[0] & B_in[0])};
119       B_out = 3'b000;
120       G_out = G_in;
121     end
122     2'b01: begin
123       A_out = {1'b0, A_in[1:0]};
124       B_out = {1'b0, add_mod3(B_in[1:0], A_in[1:0])};
125       G_out = add_mod5(G_in, {1'b0, B_in[1:0]});
126     end
127     2'b10: begin
128       A_out = A_in;
129       B_out = add_mod5(B_in, A_in);
130       G_out = add_mod5(G_in, B_in);
131     end
132     default: begin
133       A_out = A_in;
134       B_out = B_in;
135       G_out = G_in;
136     end

```

```

137     endcase
138 end
139
140 endmodule

```

141 6 Python Reversibility Checker

```

142 def ternary_step(A, B, G):
143     return A, (B + A) % 3, (G + B) % 5
144
145 def pentary_step(A, B, G):
146     return A, (B + A) % 5, (G + B) % 5
147
148 def check_bijection(step_fn, sizes):
149     nA, nB, nG = sizes
150     seen = {}
151     for A in range(nA):
152         for B in range(nB):
153             for G in range(nG):
154                 out = step_fn(A, B, G)
155                 if out in seen:
156                     print("Collision:", (A, B, G), "vs", seen[out])
157                     return
158                 seen[out] = (A, B, G)
159     print("Mapping is bijective over", nA*nB*nG, "states.")
160
161 if __name__ == "__main__":
162     print("Ternary:")
163     check_bijection(ternary_step, (3, 3, 5))
164     print("Pentary:")
165     check_bijection(pentary_step, (5, 5, 5))

```

166 7 Conclusion

167 We introduced a reversible, multi-radix symbolic gate suitable for the RHEA-UCM computational
 168 architecture. The gate supports binary compatibility, reversible ternary and pentary arithmetic,
 169 glyph/entropy tracking, and strictly bijective transition rules. Its Hamiltonian interpretation aligns
 170 with the RHEA-UCM framework, providing a concrete path toward RHEA-IC hardware capable
 171 of reversible symbolic cycles with controlled entropy production.

172 References

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