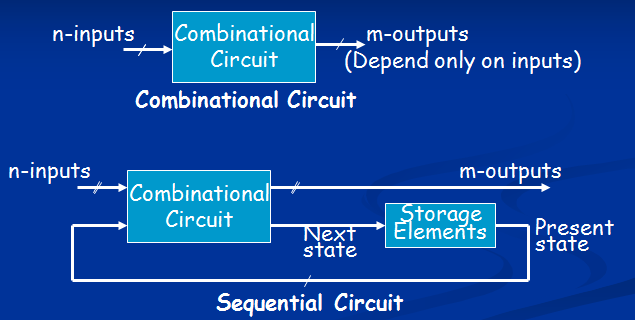
**Combinational Circuits**

* A combinational circuit consists of logic gates whose outputs, at any time, are determined by combining the values of the inputs.
* For n input variables, there are 2n possible binary input combinations.
* For each binary combination of the input variables, there is one possible output.
* Hence, a combinational circuit can be described by: A truth table that lists the output values for each combination of the input variables, or *m* Boolean functions, one for each output variable



**Combinational vs. Sequential Circuits**

* Combinational circuits are memory-less. Thus, the output value depends ONLY on the current input values.
* Sequential circuits consist of combinational logic as well as memory elements (used to store certain circuit states). Outputs depend on BOTH current input values and previous input values (kept in the storage elements).



**Integrated Circuits**

* Integrated circuit (a chip) is a semiconductor crystal (most often silicon) containing the electronic components for the digital gates and storage elements which are interconnected on the chip.
* Terminology - Levels of chip integration

SSI (small-scale integrated) - fewer than 10 gates

MSI (medium-scale integrated) - 10 to 100 gates

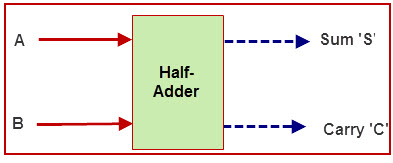
LSI (large-scale integrated) - 100 to thousands of gates

VLSI (very large-scale integrated) - thousands to 100s of millions of gates

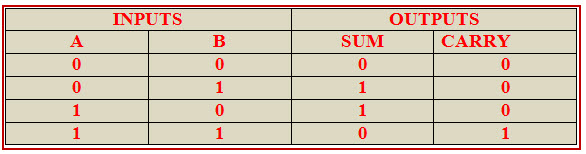
**Design Procedure for combinational circuit**

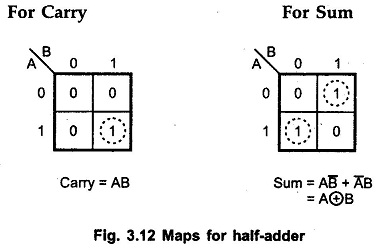
* Problem Stated
* Identify Input and output variables and assgin labels
* Derive truth table
* Derive boolean function for each output
* Draw logic diagram

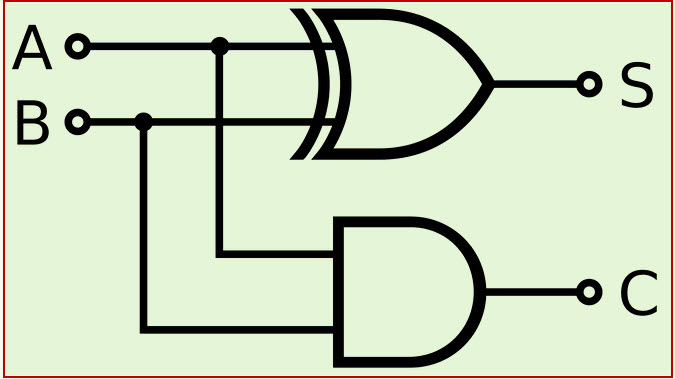
**Half Adder**



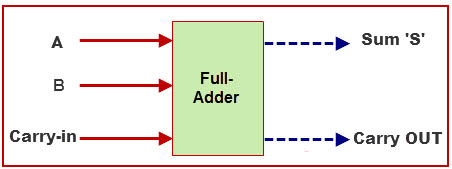
0+0 = 0  
0+1 = 1  
1+0 = 1  
1+1 = 10

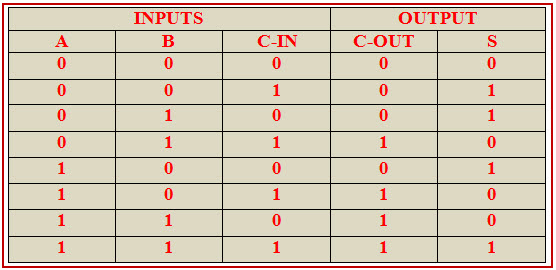


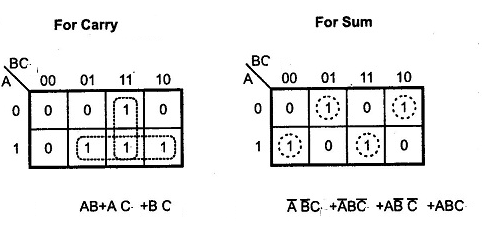
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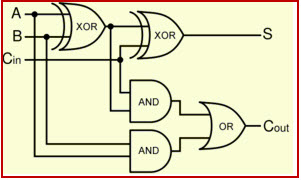


**Full Adder**



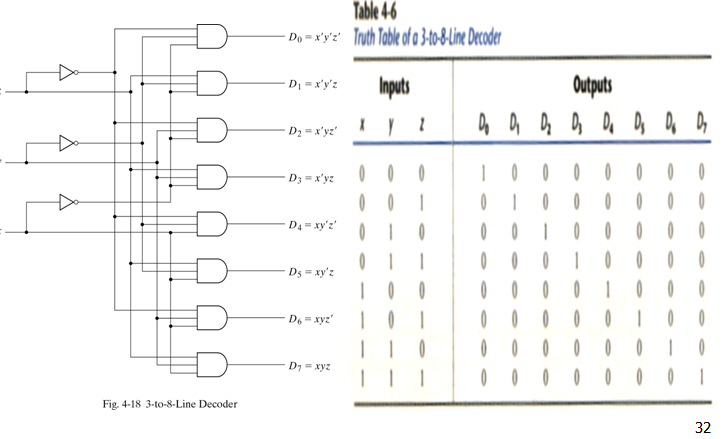




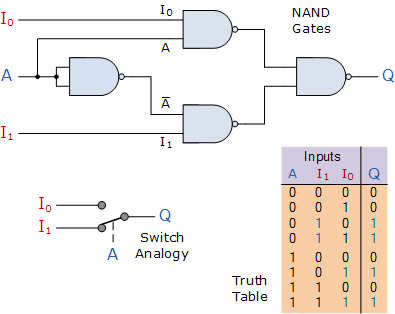


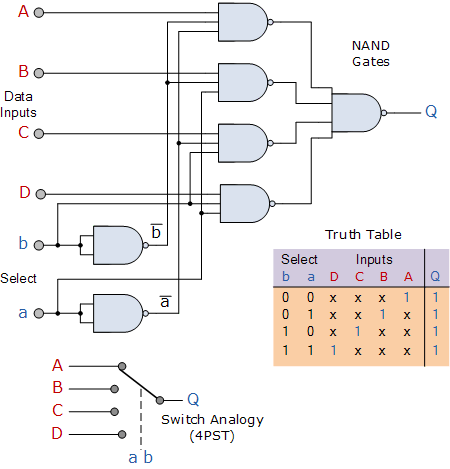
**Decoder**

* The decoder is called n-to-m-line decoder, where m≤2n .
* the decoder is also used in conjunction with other code converters such as a BCD-to-seven\_segment decoder.
* 3-to-8 line decoder: For each possible input combination, there are seven outputs that are equal to 0 and only one that is equal to 1.



**Multiplexer**

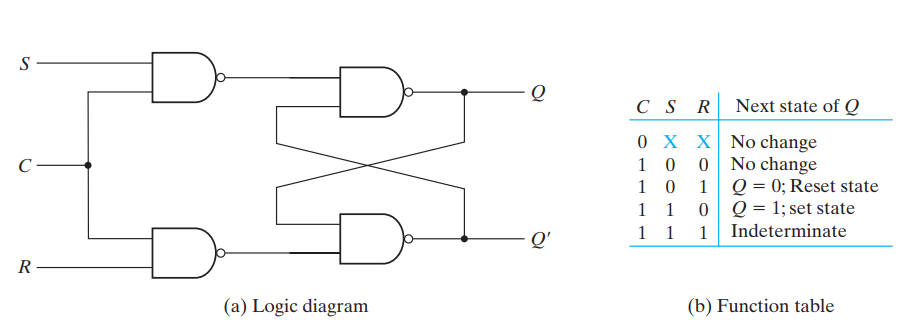
* The multiplexer, shortened to “MUX” or “MPX”, is a combinational logic circuit designed to switch one of several input lines through to a single common output line by the application of a control signal.
* 
* Q = A’.I1 + A.I0



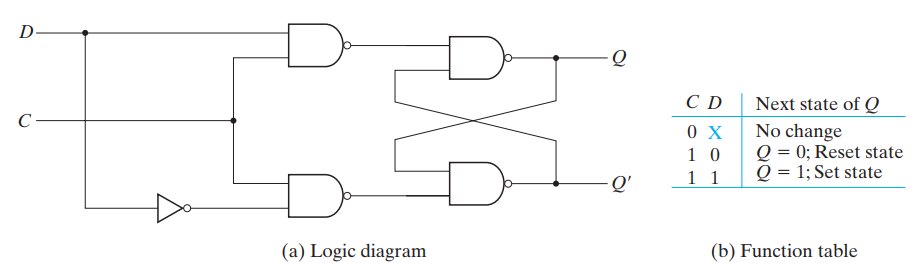


**Flip Flops**

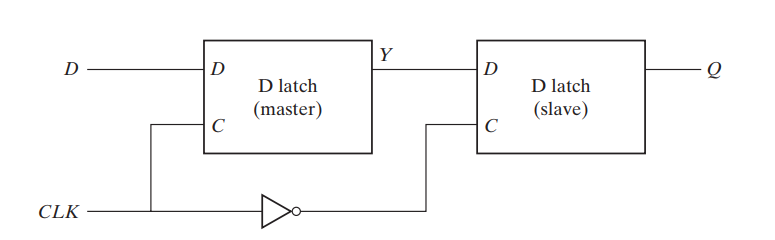
**SR Flip Flop**

****

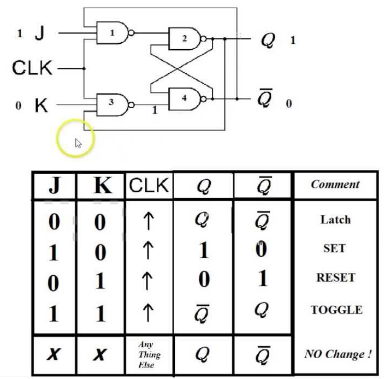
D-Flip Flop



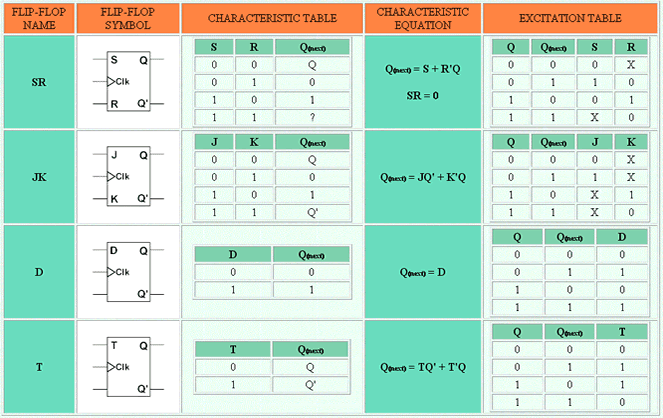
Master \_Slave Flip Flop



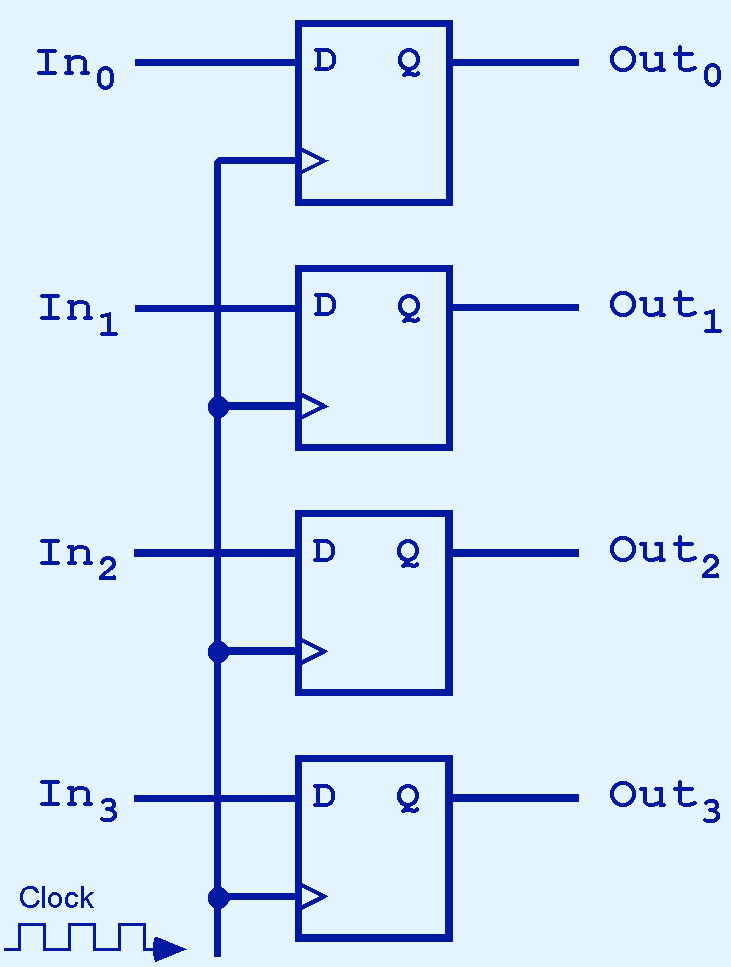
JK Flip Flop



Flip Flop chacterstic equation & excitation table



Register

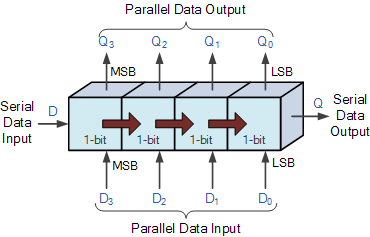
Collection of flip flops



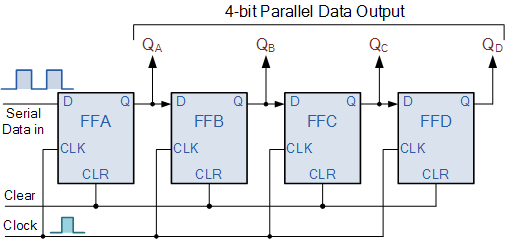
**Shift Register**

The **Shift Register** is another type of sequential logic circuit that can be used for the storage or the transfer of data in the form of binary numbers

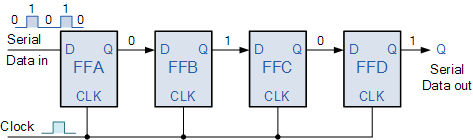
* Serial-in to Parallel-out (SIPO) - the register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form.
* Serial-in to Serial-out (SISO) - the data is shifted serially “IN” and “OUT” of the register, one bit at a time in either a left or right direction under clock control.
* Parallel-in to Serial-out (PISO) - the parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.
* Parallel-in to Parallel-out (PIPO) - the parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.



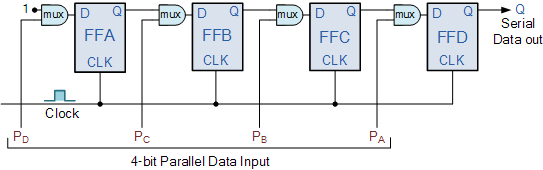
**Serial-in to Parallel-out (SIPO) Shift Register**



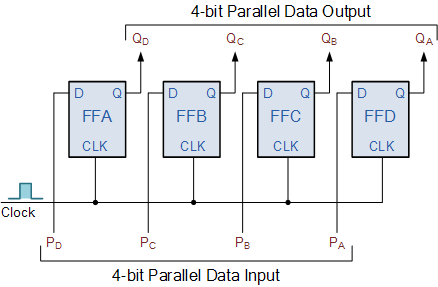
**Serial-in to Serial-out (SISO) Shift Register**



**Parallel-in to Serial-out (PISO) Shift Register**



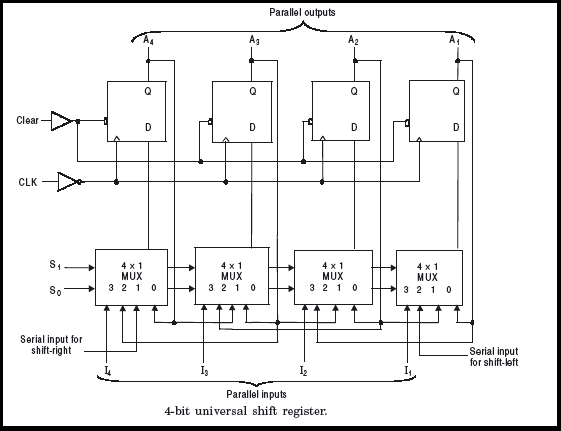
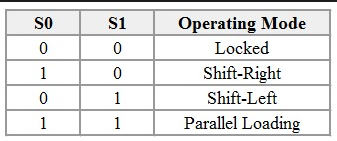
**Parallel-in to Parallel-out (PIPO) Shift Register**



**Universal Shift Register**

A unidirectional shift register is a register that can capable of transferring data in only one direction. Whereas the register that is capable of transferring data in both left and right direction is called a ‘bidirectional shift register.’ we have a register which can capable to transfer data in both the shift-right and shift-left, along with the necessary input and output terminals for parallel transfer, then it is called a shift register with parallel load or ‘universal shift register.’

* A shift-right control to enable the shift-right operation and the serial input and output lines associated with the shift-right.
* A shift-left control to enable the shift-left operation and the serial input and output lines associated with the shift-left.
* A parallel-load control to enable a parallel transfer and the n input lines associated with the parallel transfer.
* n parallel output lines.
* A clear control to clear the register to 0.
* A CLK input for clock pulses to synchronize all operations.
* A control state that leaves the information in the register unchanged even though clock pulses are continuously applied

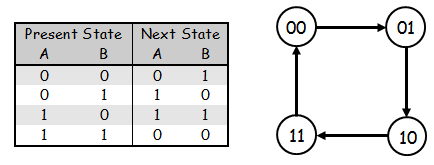
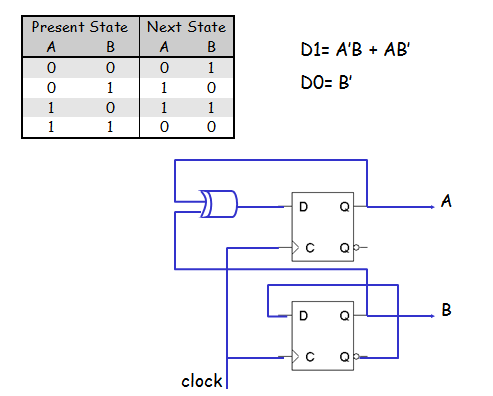


**Binary Counter**

A counter that follows the binary number sequence is called a binary counter. n-bit binary counter: n flip-flops, count in binary from 0 to 2ⁿ-1. Counters are available in two types: Synchronous Counters,Ripple Counters.Synchronous Counters-A common clock signal is connected to the C input of each flip-flop.

**Synchronous Binary Up Counter**

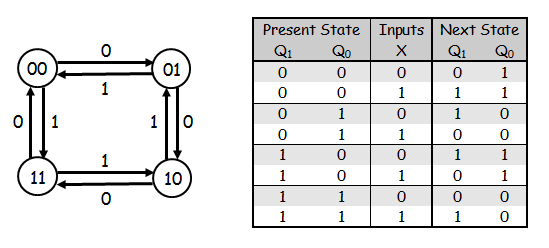
The output value increases by one on each clock cycle. After the largest value, the output “wraps around” back to 0.Using two bits, we’d get something like this:

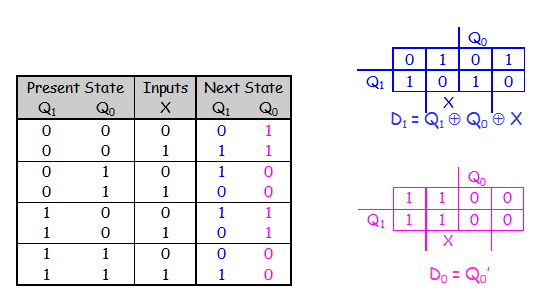


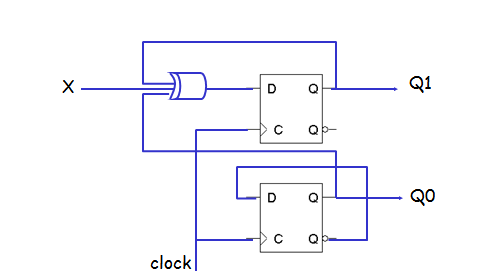
**Synch Binary Up/Down Counter**

2-bit Up/Down counter Counter outputs will be 00, 01, 10 and 11. There is a single input, X.

> X= 0, the counter counts up and > X= 1, the counter counts down







**Ripple Counter**

