Project Report (Group No.7)

Cascaded H-bridge Converter

(EE-560 Power Electronics Converters)

Submitted By

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List of Figures

1 Contribution

Name : Shuchi Pathak

Report Preparation using Latex.

Studied the applications and working of Cascaded Multi level converter and Phase Locked Loop (PLL) Technique.

Name : Vikas Pal

Studied the applications and working of Cascaded Multi level converter and Phase Locked Loop (PLL) Technique.

Figures and Block Diagram by Visio.

Name : Vinay Pandey

Studied the applications and working of Cascaded Multi level converter and Phase Locked Loop (PLL) Technique.

Matlab Simulation.

2 Input and Output Parameters

Input DC Voltage: 800 V

Output DC Voltage: 650 V

Power Rating: 20 kW

Switching Frequency = 50 KHz

3 Objective

The objective of our project is to obtain Nine-level output voltage using three phase 4 cell multi-level converter. The key objectives are to gain high voltage using low rating of IGBT and to reduce harmonics and improve efficiency of the output.

4 Introduction

The cascaded H-bridge converter was proposed for high voltage, high-power applications such as FACTS , or electric vehicles , due to that it can reach high voltage and reduce harmonics .And the main difference between the other multilevel converter to H bridge is modularity which can be achieve by cascading of H bridge. There are separate H-bridge circuits in this system for each phases A, B, and C, respectively Each phase consists of 4 H-bridge cells connected in series, forming a "cluster". The clusters are connected to the medium-voltage (MV) grid with load. The 50 Hz, MV grid is modelled as an ideal AC voltage source with a line to-line RMS voltage of 11 kV. The H-bridge cells utilize conventional IGBTs. These are modelled as ideal switches in MATLAB to achieve high speed and robustness for system-level simulation.

Main objective of multilevel inverter is to reduce the Total Harmonic Distortion(THD) in the operating system.

Normally it is achieved by increasing the number of the DC source and the switch. However, this method will increase the power losses.That is why the new topology will try to reduce the component without reducing the quality output of converter.

4.1 Types of Topologies

There are three different types of topologies of Cascaded H-Bridge multi-level Inverter:

Diode clamped converter, Flying capacitors and Cascaded H-bridge.

4.1.1 Diode Clamped Converter:

Neutral-point-clamped(NPC) PWM topologies the first practical multilevel topology. Diode clamped multilevel inverters use clamping diodes. It helps to limit the voltage stress of power electronic devices.

An m level diode clamped inverter needs-
Switching devices (2m−2),
Input voltage source (m − 1)

Key Characteristics of a Diode Clamped Converter:-

Multilevel Structure: In a diode clamped converter, the voltage is divided across multiple levels, which reduces the voltage stress on each semiconductor device and allows for higher power ratings.
Diodes for Clamping: Diodes are strategically placed to clamp certain points within the circuit to fixed voltage levels. This allows for the creation of intermediate voltage levels, such as three-level, five-level, or higher structures, depending on the design.
Reduced Harmonic Distortion: By generating multiple voltage levels, diode clamped converters produce waveforms that are closer to sinusoidal, which minimizes harmonic distortion. This is particularly advantageous in AC applications.
Commonly Used in AC Drives: Diode clamped multilevel converters are widely used in medium- and high-voltage AC motor drives due to their efficiency, reliability, and ability to handle high power levels.

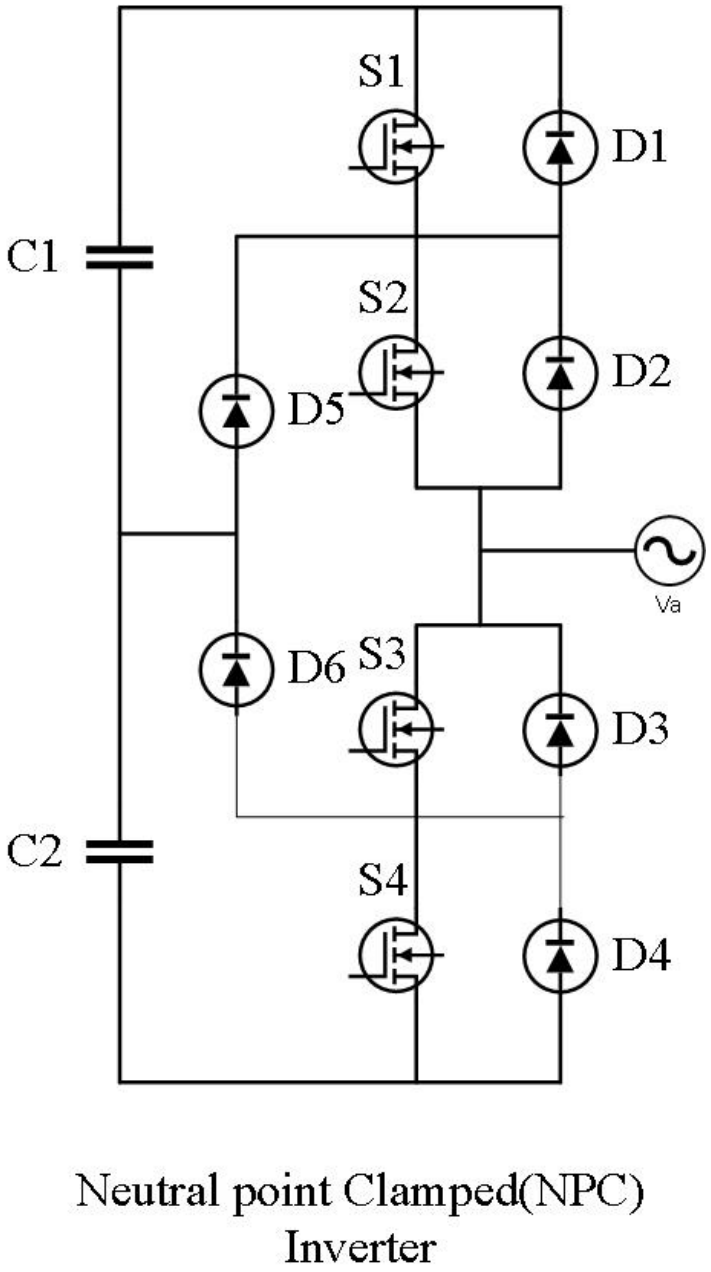

Figure 2: Diode Clamped Converter(or NPC)

4.1.2 Flying Capacitor Multilevel Inverter Topology:

It is an alternative to the diode-clamped MUI topology. Here capacitors are used to limit the voltage. The presence of capacitors makes it different from that of diode clamped MLI where diodes are used. Capacitors divide the input DC voltages. The voltage across each capacitor and switch is V dc.

The main feature of the FCMLI is the use of capacitors to achieve multiple voltage levels, reducing the harmonic content in the output waveform and enabling higher power quality.

An m level flying capacitor inverter needs-

Switches: $(2m - 2)$

Number of capacitors: $(m - 1)$

Key Features of a Flying Capacitor Multilevel Inverter:

Capacitor-Based Voltage Levels: Unlike diode clamped multilevel inverters, the FCMLI relies on floating capacitors to create the different voltage levels in the output. These capacitors are connected in series with the power semiconductors, allowing intermediate voltage levels to be generated.

Multilevel Output: The inverter can produce multiple voltage steps (e.g., 3-level, 5-level, or higher), depending on the number of capacitor levels and switches used. This multilevel structure reduces the total harmonic distortion (THD) of the output voltage, providing a smoother AC waveform.

Independent Control of Each Voltage Level: The flying capacitors allow for independent control of voltage levels, which can provide more flexibility in operation. By adjusting the switching sequence, the voltage across each capacitor can be controlled to maintain the desired output.

Self-Balancing Capability: Through careful switching, the flying capacitor topology has an inherent self-balancing ability, meaning the voltages across each capacitor tend to balance over time. This reduces the need for complex control mechanisms to balance the voltage levels.

High Efficiency and Reliability: FCMLIs are generally more efficient due to their lower switching losses and reduced electromagnetic interference (EMI). They are also known for reliability in high-power applications.

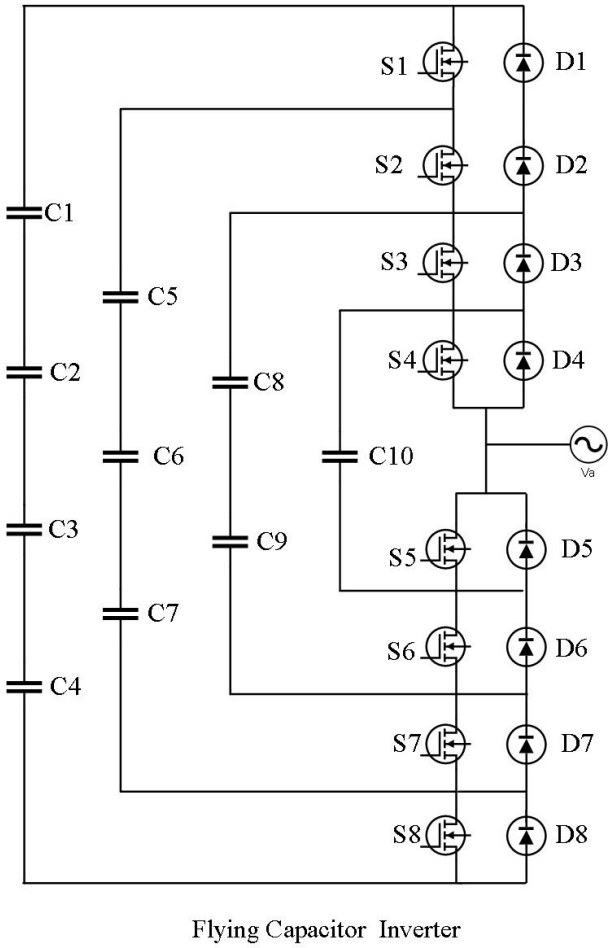

Figure 3: Flying Capacitor MLC

4.1.3 Cascaded Voltage H Bridge Multilevel Inverter Topology:

The cascaded H-bridge inverter uses separate Dc sources or capacitors .It requires only less number of components in each level. There is a series connection of power conversion cells.

The H-bridge consists of capacitors and switches pair combination. For each H Bridge, separate input DC voltage is obtained. It generates a sinusoidal output voltage. The inverter uses series connected H-bridge cells, each providing three different levels of Dc voltages (zero, positive DC and negative DC voltages). The output voltage is the sum of all the generated voltages from each H Bridge cell.

If m cells are present, the numbers of output voltage levels will be 2m+1.

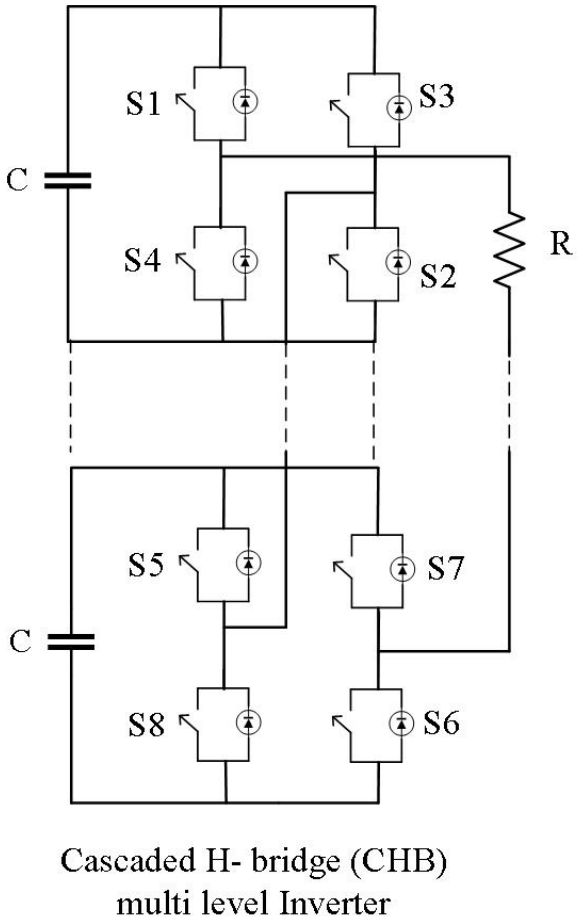

Figure 4: Cascaded H -Bridge

Key Features of Cascaded H-Bridge Multilevel Inverters:

Modular Structure: The CHBMLI consists of multiple H-bridge inverter units connected in series, each typically powered by a separate DC source (e.g., batteries, photovoltaic panels, or rectified sources). This allows the inverter to create multiple voltage levels by adding or subtracting the DC source voltages in different configurations.

Reduced Harmonic Distortion: With more levels in the output waveform, the CHB inverter approximates a sinusoidal waveform more closely, reducing total harmonic distortion (THD). This results in a high-quality output voltage, suitable for high-power applications.

Separate DC Sources: Each H-bridge cell typically requires an independent DC source. This is ideal for renewable energy applications where sources like solar panels or battery banks provide natural, separate DC supplies for each cell.

5 Converter Structure

A three-phase schematic of the generalized structure of the proposed MLC system and the configuration of three leg is shown in Fig. 2, respectively. the output of the power cell gets access to the dc-link MP potential and, hence,becomes capable of generating nine output voltage levels ±4Vdc , ±3Vdc , ±2Vdc, ±Vdc and 0, where Vdc is the dc-link voltage of a power cell. This nine-level power cell is termed "transistor-clamped H-bridge" (TCHB) power cell. other bidirectional switch configurations, such as back-to-back IGBTs in common emitter or common collector configurations or reverse blocking IGBT.

The proposed configuration is termed symmetric and hybrid because the cell dc-link voltages are equal for all the power cells.With equal cell dc-link voltage,the voltage stress on all the HB switches is the same; hence, the switch voltage rating is equal for all the HB switches.

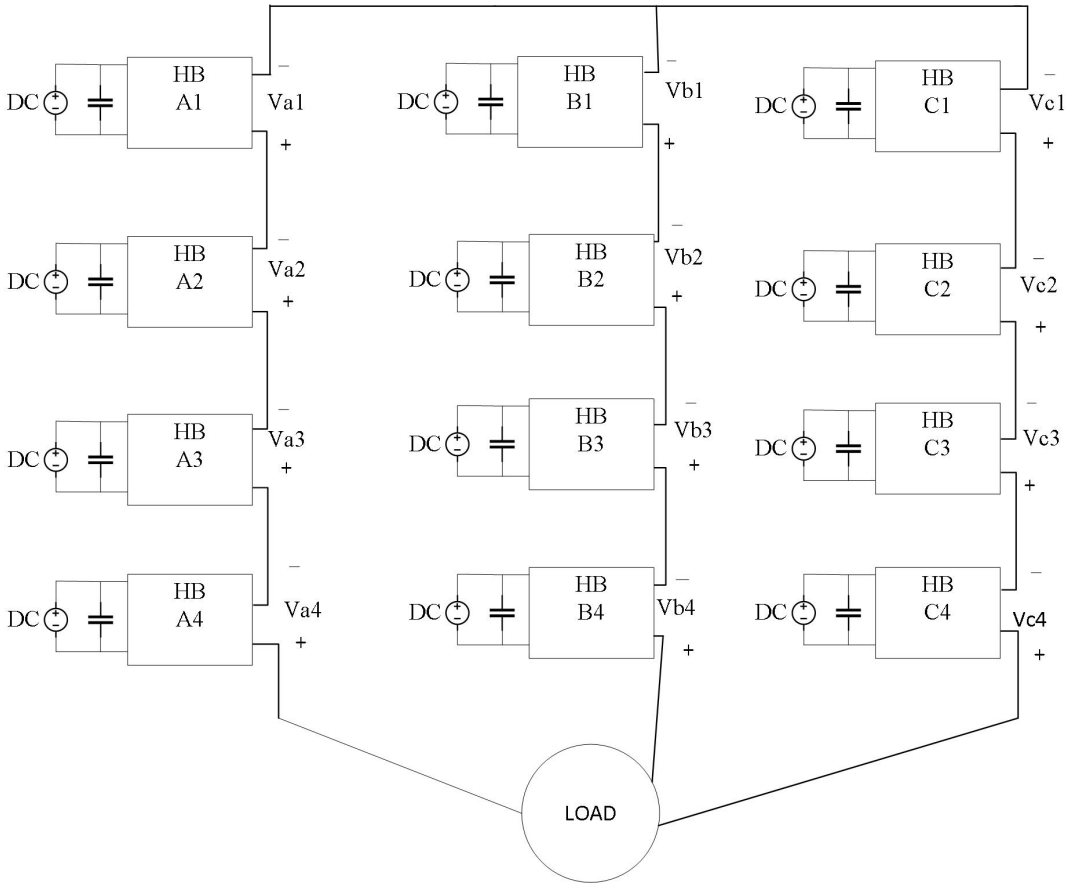

Figure 5: Schematic Circuit

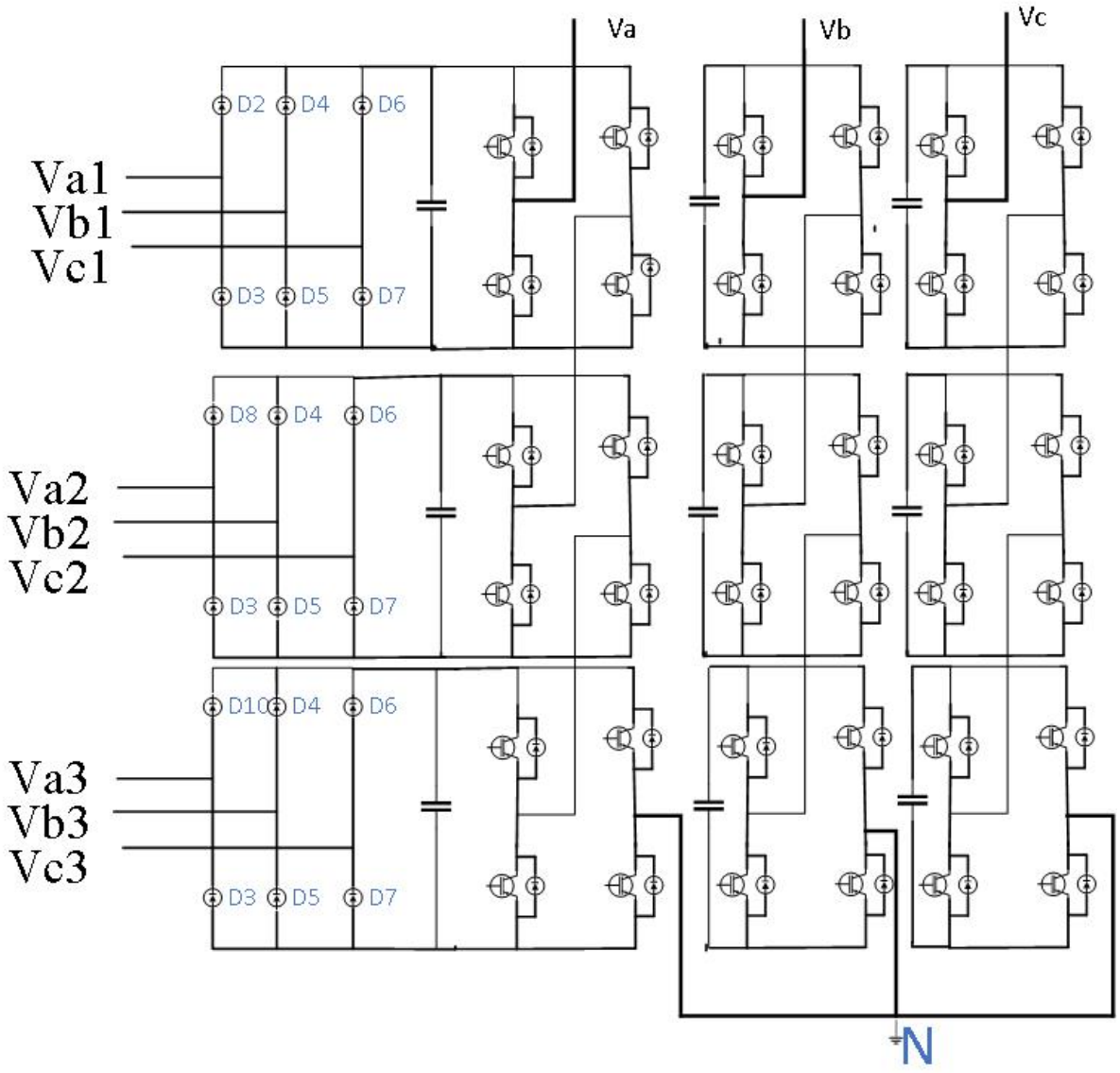

Figure 6: Three phase Cascaded H bridge Circuit Diagram

6 Operating Principle

The converter works by combining the output of each H-bridge inverter in a series configuration to form a multilevel voltage waveform. The converters use pulse width modulation (PWM) or other control techniques to regulate the output voltage and current. The switching pattern determines the output waveform quality and the harmonic content.

6.1 Switching Scheme:

Each H-bridge generates three possible voltage levels: $+Vdc$, 0, or Vdc, depending on the switching states. By controlling the switches appropriately, different voltage levels can be synthesized at the output.

The switching operation is described below:

For four cells we will get nine level of output voltages.

1. To get $4Vdc$ as the output voltage level we need Vdc from each cell.

2. To get $3Vdc$ as the output voltage level we need Vdc from three cells and 0 from one cell.

3. To get $2Vdc$ as the output voltage level we need $2Vdc$ from two cells and 0 from the other two cells.

4. To get Vdc as the output voltage level we need Vdc from one cell and 0 from the other cells.

5. To get 0 as the output voltage level we need 0from each cell or Vdc from two cells and $-Vdc$ from the other two cells.

6. To get $-Vdc$ as the output voltage level we need $-Vdc$ from one cell and 0 from the other cells.

7. To get $-2Vdc$ as the output voltage level we need $-Vdc$ from two cells.

8. To get $-3Vdc$ as the output voltage level we need $-Vdc$ from three cells.

9. To get $-4Vdc$ as the output voltage level we need $-Vdc$ from all the cells.

6.2 PWM Generation:

PWM Pulse Generation Process can be understood through the following points:

1. For each phase, a reference sine wave is applied that represents the desired output voltage waveform.

2. The frequency of this waveform corresponds to the fundamental frequency of the output voltage (e.g., 50 Hz or 60 Hz).

3. A triangular or sawtooth waveform (carrier signal) is used for modulation.

4. The intersections of these two waveforms determine when the inverter switches are turned on and off.

5. When the reference signal is above the carrier, the switch is turned on; otherwise, it is off.

6. Each phase (A, B, C) will have its own reference sine wave, typically phase-shifted by 120 degrees.

7. The Carrier wave will be different for each desired level of output voltage. For example- To produce first output voltage level, the reference wave is compared with the carrier wave having amplitude 0 to 1 then for second level of output voltage,the reference wave is compared with carrier wave having amptlitude varying from 1 to 2 and so on for higher levels.

8. The resulting output waveform is a stepped approximation of a sinusoidal wave, with multiple voltage levels depending on the number of H-bridge cells used.

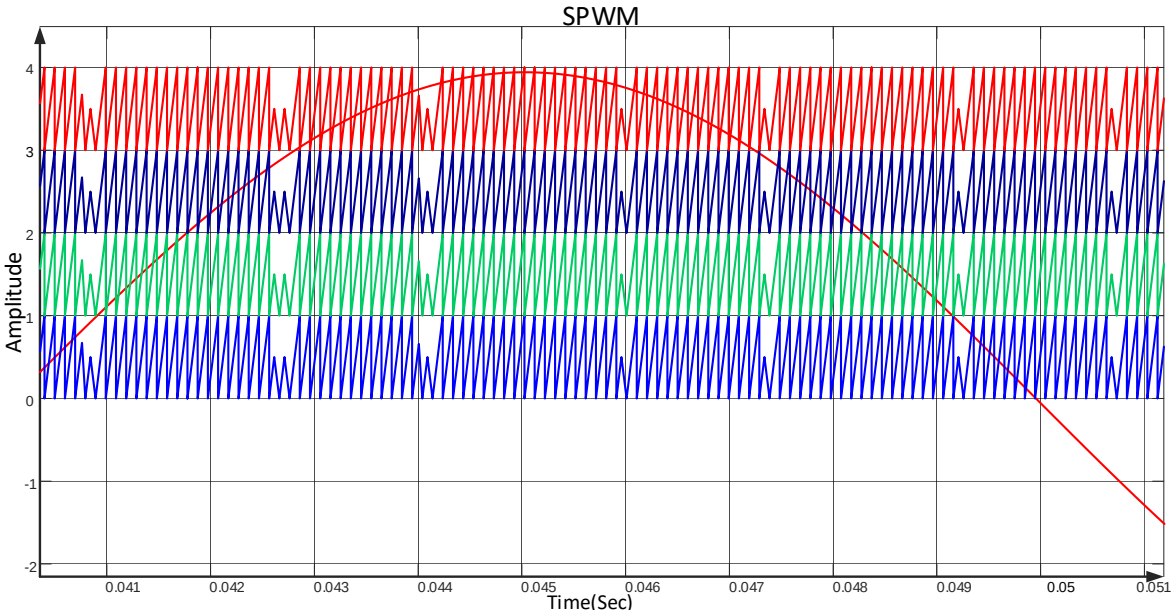

Figure 7: PWM Pusle Generation

6.3 Phase Locked Loop (PLL):

A phase-locked system (PLL) is a closed-loop system in which an internal oscillator is controlled to keep the time of some external periodical signal by using the feedback loop. It is a technique used to align the frequency and phase of an output signal with that of the grid.

6.3.1 Key Components:

1. Phase Detector- Compares the phase of the incoming grid signal with the output signal from the PLL.

2. Loop Filter- Smooths the output of the phase detector to reduce noise and stabilize the control signal.

3. Voltage-Controlled Oscillator(VCO)-- Generates a signal that can be adjusted in Frequency and phase based on the filtered output.

6.3.2 Process:

1. Signal Detection- The PLL continuously monitors the grid signal.

2. Phase Comparison- The phase detector identifies any differences between the grid signal and the output signal.

3. Error Correction- The loop filter processes this error to adjust the VCO, aligning the output signal's frequency and phase with that of the grid.

4. Feedback Loop- This process repeats, maintaining synchronization as grid conditions change.

6.3.3 Use of PLL in Power Electronics:

In power electronics a phase-locked loop(PLL) is a feedback control circuit that synchronizes a signal with a grid or other input signal.

A Phase-Locked Loop (PLL) is essential for synchronizing the inverter's output with the grid's phase and frequency.

Here's how PLLs are generally used in such systems.

Phase and Frequency Synchronization-

A PLL is used to detect the phase angle of the grid voltage and synchronize the CHB inverter's output to match the grid's phase and frequency. This is crucial for applications like grid-connected inverters in renewable energy systems (e.g., solar and wind).

The PLL continuously adjusts to any changes in the grid frequency, helping the CHB inverter maintain synchronization even if there are grid frequency deviations

Overall, PLL-based synchronization is essential for reliable and efficient power systems,enabling smooth integration of various energy sources.

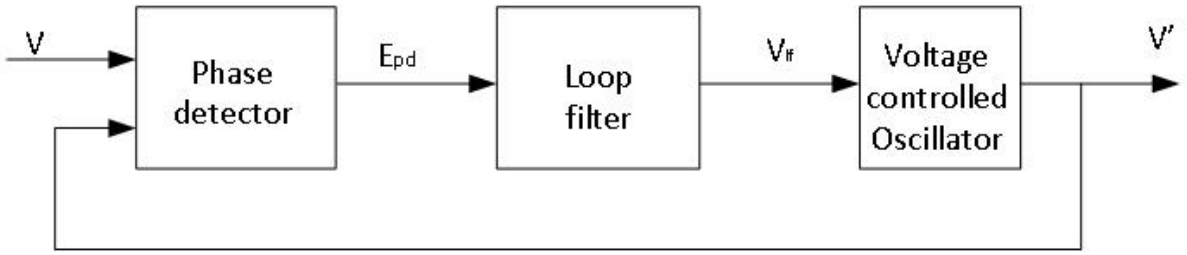

Figure 8: Block Diagram of PLL

6.4 Output Voltage:

The output voltage of the CHB converter is the sum of the output voltages from all H-bridge inverters. If there are N H-bridges, the converter can produce 2N + 1 voltage levels, e.g., here we are using 4 H-bridge cells, it can produce 9 voltage levels.they are $+4Vdc$, $4Vdc$, $+3Vdc$, $3Vdc$, $+2Vdc$,$2Vdc$,$+Vdc$,Vdc or0 The voltage waveform approximates a sinusoidal shape, and as the number of levels increases, the waveform becomes smoother and closer to an ideal sine wave.

6.5 Multilevel Voltage:

The CHB converter's primary advantage is that it generates a stepped output voltage with multiple levels, significantly reducing harmonics and the need for large filters.

7 Simulation Diagram

We have done the simulation for three phase four cell multi-level converter.

The PWM Generation principle as well as the switching schemes applied in the simulation circuit is explained in the above section (Operating Principle).

7.1 The Simulation circuit model(Open Loop)

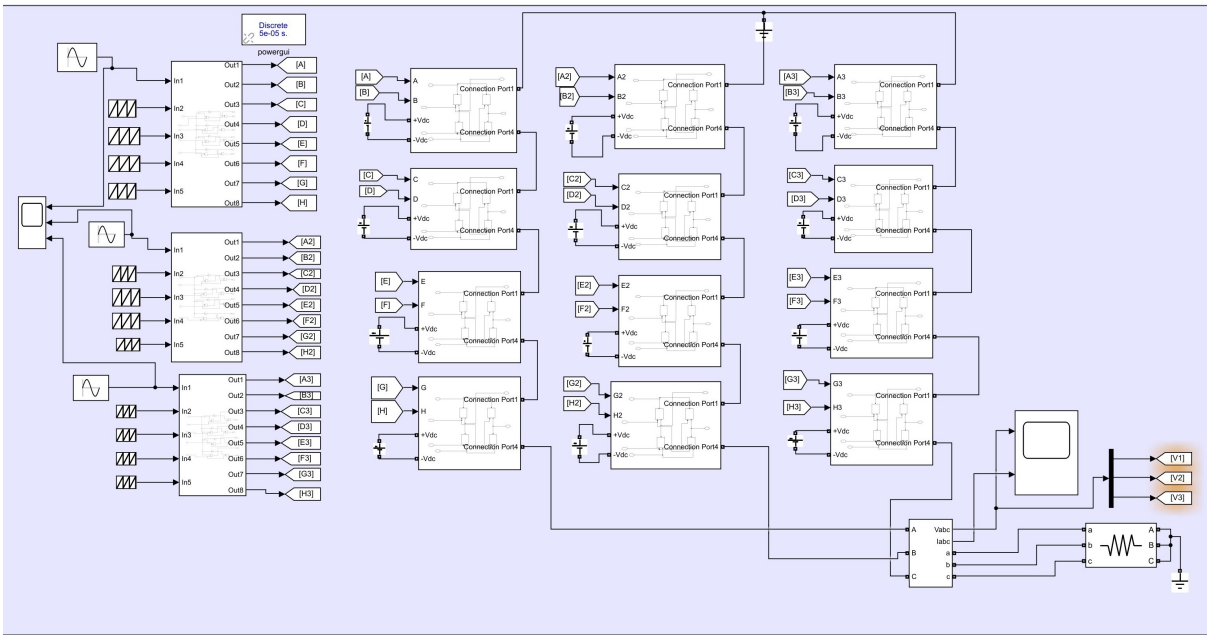

Figure 9: Simulation Circuit Model(Open Loop)

7.2 The Simulation circuit model(Closed Loop)

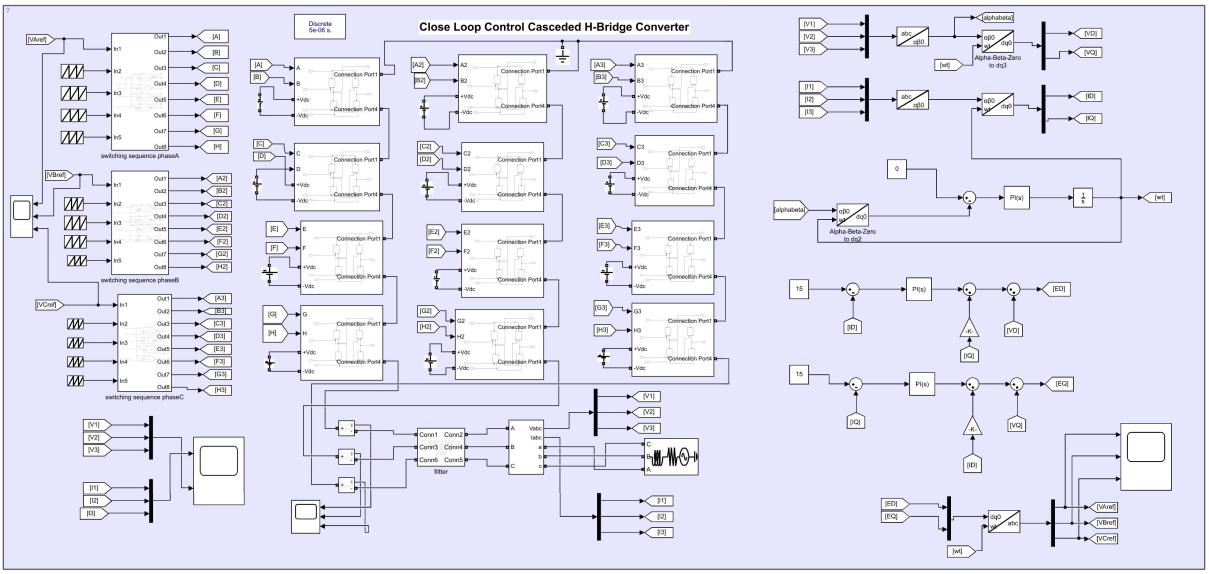

Figure 10: Simulation Circuit Model(Closed Loop)

7.3 The Subsystems in the simulation model

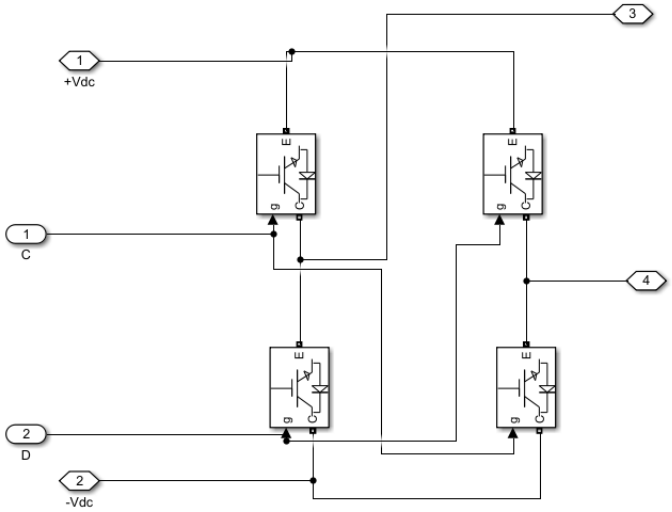

Figure 11: H-bridge Inverter(Subsystem)

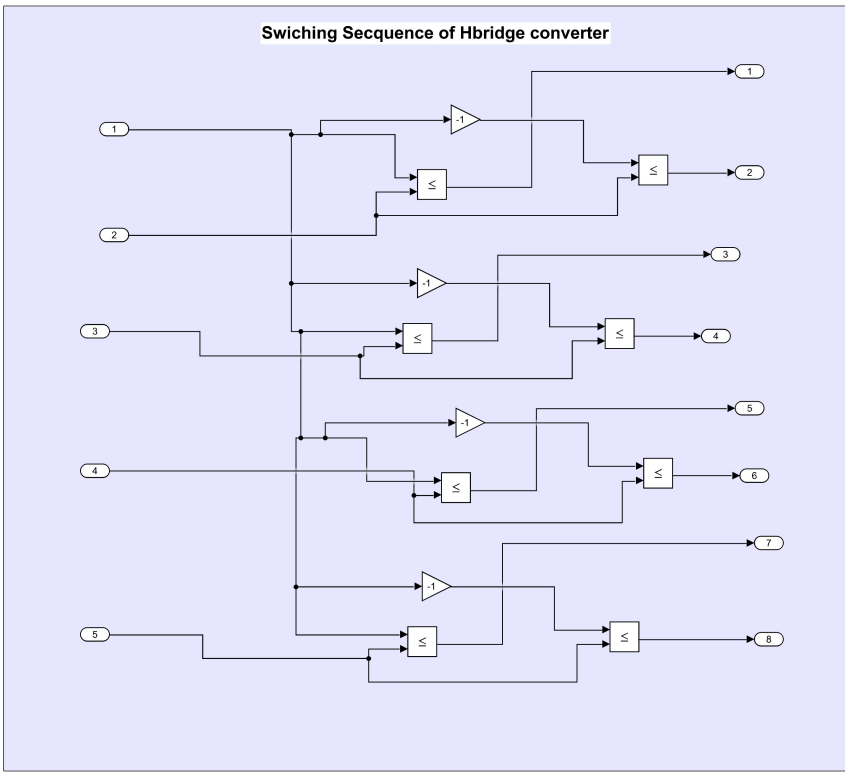

Figure 12: Switching Model(Susbsytem)

7.4 The Phase Locked Loop used in the simulation

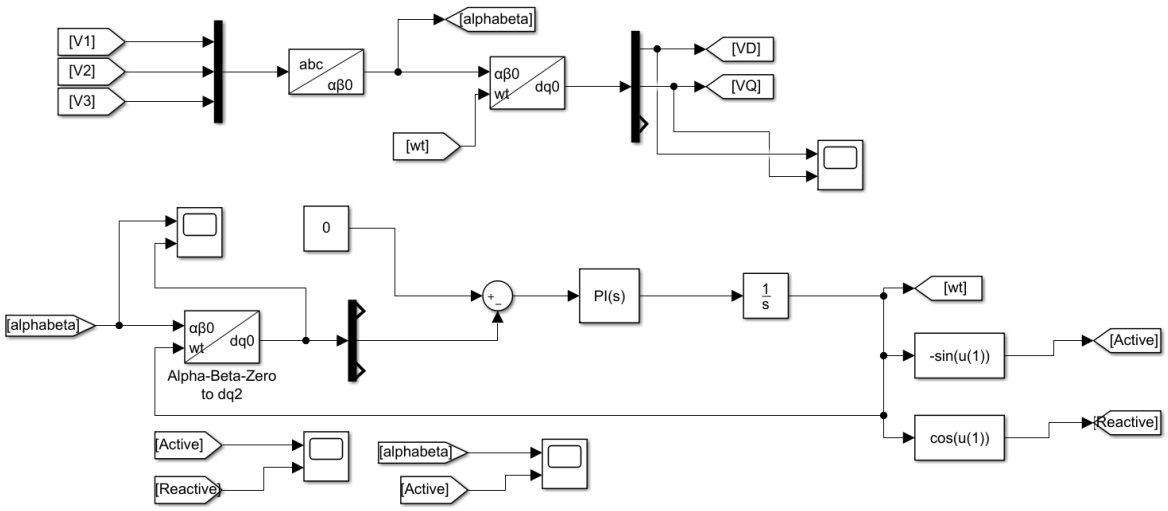

Figure 13: Phase Locked Loop(PLL)

7.5 The output voltage waveform

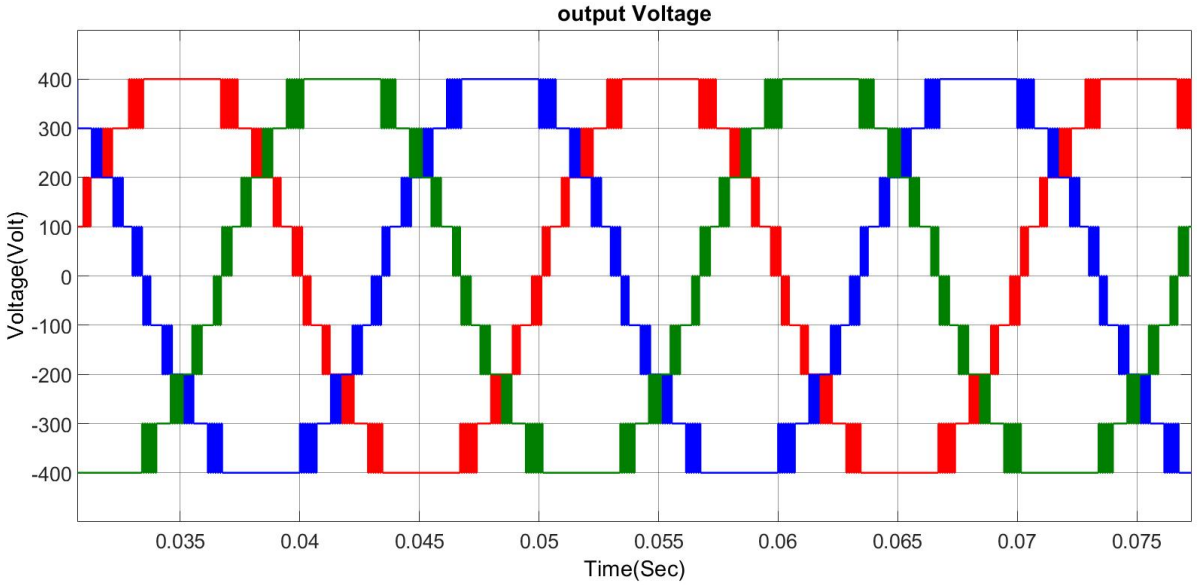

Figure 14: Output Voltage

7.6 Voltage Output with Filter

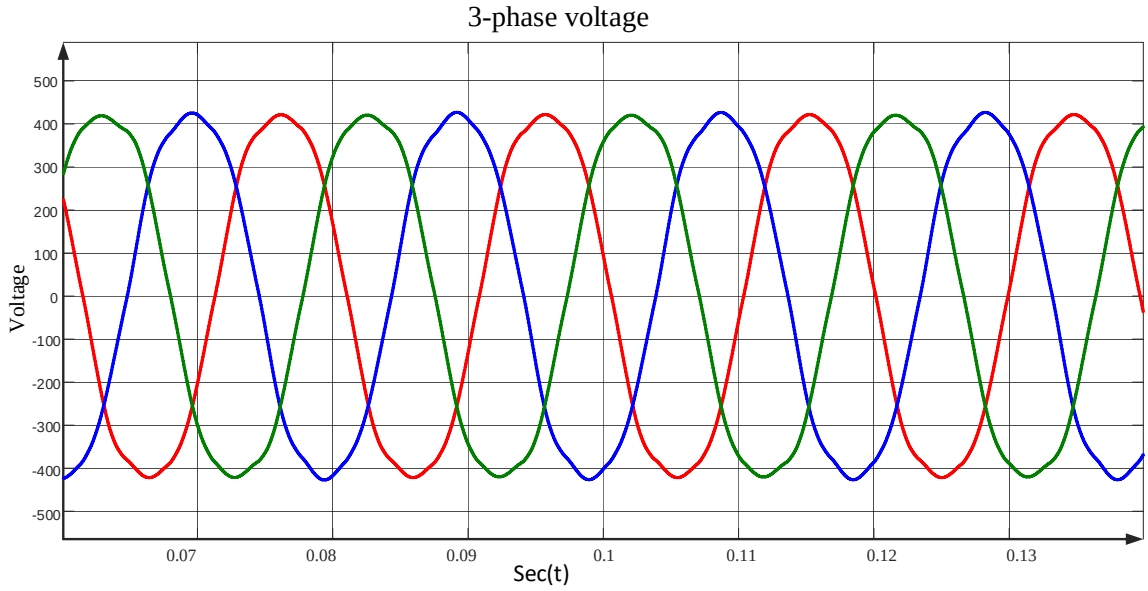

Figure 15: Output Voltage with Filter

7.7 Current Output with Filter

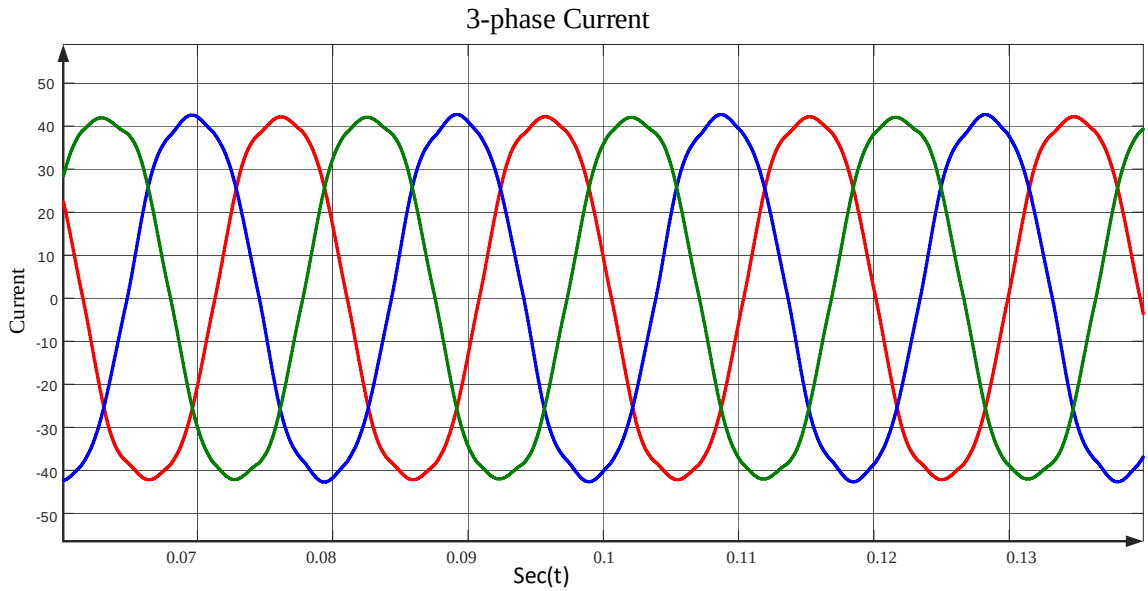

Figure 16: Output Voltage with Filter

8 Conclusion

The Cascaded H-bridge converter is a versatile and essential power electronic device widely used for driving loads in various applications.

We have studied the Phase Locked Loop (PLL) Technique and done the simulation for three phase four cell Multi-level Converter using PLL.

It is suitable for high voltage and high current rating electric drives.

Hybrid Electric Vehicles(HEV) has high current and low voltage rating in order to reduce weight of the batteries.

Cascaded multilevel inverters are switched at low frequency so it will create low noise which can be suppressed and comfortable for driving HEVs.

This converter will have high power factor and also have less EMI and voltage unbalance problem.

References

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