

Changes to V11 SCL and SDA were switched on V10, fixed on V11 Broke out VLOGIC line C2 was mislabled as 10nF, should have been 2.2nF. Added selectable jumpers to CLK, FSYNC and ADO Minor layout changes Played around with IC footprint. Added 4 small tcream squares to middle pad. Rounded and elongated pads. BOM changes C2 is now 2.2nF instead of 10nF New Stencil YES Changes to V12: -0402 --> 0603-Changed Z-Axis symbol to reflect proper orientation from circle with x to circle with dot -Changed NET labels in schematic to flags Second pull-ups are optional VIO VCC VCC Conn_01x10 ___10 VCC C11 VCC **⊸**VCC C13 9 GND **⊸**GND 8 INT TNID-7 FSYNC FSYNC GND VCC 6 SCL GND **⊸**dSCL 5 SDA **⊸**SDA 4 VIO **⊸**01V**□** 3 CLKIN OCLKIN 2 AUX_SCL AUX_SCL AUX_SDA AUX_SDA Populate pull-up if set to open-drain mode -<u>10K</u>-vcć INT SCL 6_AUX_SDA AUX_SDA AUX_SCK 7_AUX_SCL 12C Address Selection* FSYNC 11 FSYNC CP0U1 CLKIN 1 ELKIN 10 REGOUT C14 GND MPU-6050 ______2.2nF GND GND GND * Two MPU-60X0s can be connected to the same I2C bus The LSB bit of the 7 bit address is determined by the logic level on pin ADO. Default Address = 0x68 (pin ADO is logic low) Alternative Address = 0x69 (pin ADO is logic high) Rewritten by Gabe Sparkfun ** Optional external reference clock input. Connected to GND by default. Sheet: /IMU/ Cut trace for external clock File: MP6050.sch Title: MP6050 Breakout Board *** Frame synchronization digital input. Connected to GND by default Size: A Date: Rev: Cut trace for external sync KiCad E.D.A. kicad (5.1.4)-1 Id: 2/2