CSE 3203 CT 4 Assignment Roll No: 1903099

Instruction: Covert this doc to PDF while uploading.

Assignment Problem:

Build CPU based on following requirements:

- 1. Word Size of CPU = 5
- 2. ALU Operations = OR, ADD, ROL (2 bit)
- 3. Register Number = 4
- 4. Size of RAM = 7
- 5. Word size of ISA and RAM = 15 (7x15)
- 6. CPU Instructions = Register, Immediate, JMP, JNC

Solution:

https://youtu.be/_UUmT5XhKJ4

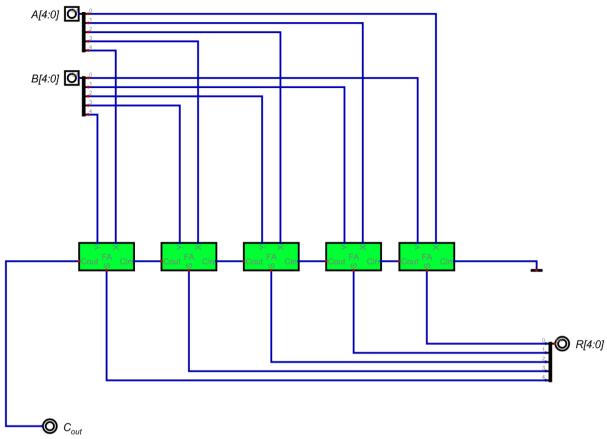
Simulator Design:

1. ALU Circuit (Show all circuits except FA circuit)(Marks 5):

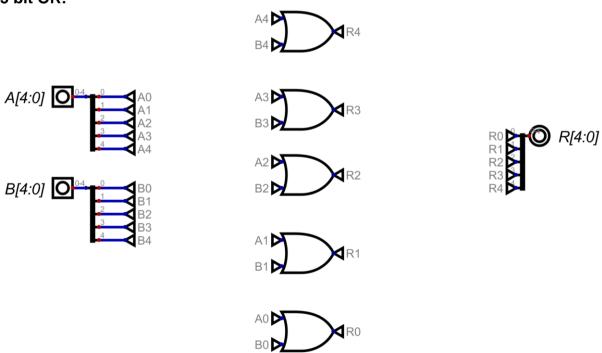
Check List:

Have you added all circuits of ALU from FA to ALU Operations Circuits (ADD, XOR, SHL etc.) to Top Level ALU Circuit?	YES

5 bit Adder:



5 bit OR:

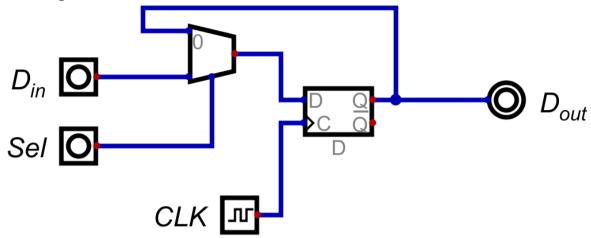


5 bit ROL: Medi 💇 == 5 bit ALU: 5bit_adder A[4:0] R[4:0] **O** R[4:0] 5bit_ROL 5bit_OR OP[1:0]

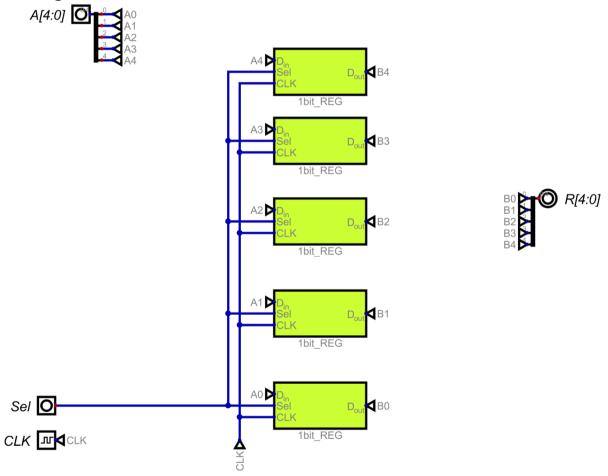
2. Register Set Circuit (Top to Bottom all circuits)(5 Marks): Check List:

Have you added all circuits of Register Set from 1 bit Register to n bit Register to Top Level Register Set Circuit.?	YES

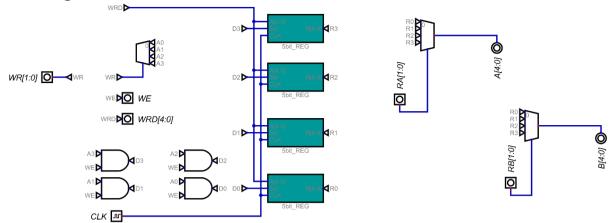
1 bit Register:



5 bit register:



5 bit Register Set:

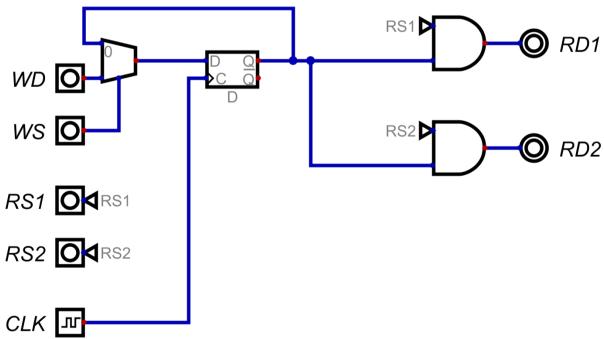


3. RAM Circuit (Top to Bottom all circuits)(5 Marks):

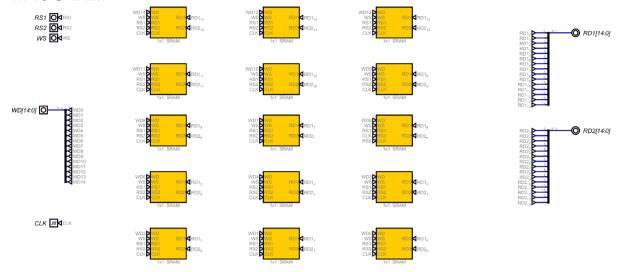
Check List:

Have you added all circuits of RAM from 1x1 RAM to 1xN RAM to MxN RAM?	YES

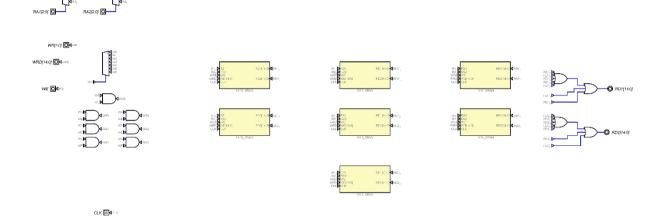
1x1 SRAM:



1x 15 SRAM:



7x15 SRAM:



4. a) ISA (2 Marks)

Check List:

Have you added all ISA of CPU along with its sample machine code to be run on CPU?	YES/

ISA (Register Mode):

Орс	ode (6 bit)	Register 1	Register 2	Unused
2 bits	2 bits	2 bits	2 bits	7 bit
Types of instruction	Operations (ALU selection lines)	Ra (00-11)	Rb (00-11)	X

ISA (Immidiate Mode):

Орс	ode (6 bit)	Register 1	value	Unused
2 bits	2 bits	2 bits	5 bit	4 bit
Types of instruction	Operations (ALU selection lines)	Ra (00-11)	Val(00000- 11111)	Х

Sample Machine Code with assembly code in comments to be run on CPU (You will make a video running this machine code on CPU in order to prove that your CPU is working perfectly)

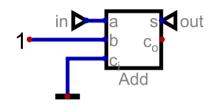
Machine Code	Assembly Code
100100010000000 001001010000000 010001010010	JE START START: OR R1,R1 JMP_TO: ADD R1,5

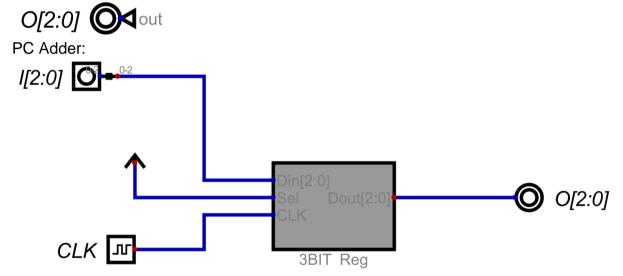
b) CPU (Top to Bottom all circuits)(3 Marks): Check List:

Have you added all circuits of CPU from Program Counter to Control Unit to Top Level CPU Circuit with Output Pins showing contents of ALU, Register Set, RAM etc. (Important for CPU Verification, Check Tutorial Videos for Details)?	YES
Have you made a video running this sample machine code on the CPU (1 instruction at a time in a similar way shown in video) in order to prove that your CPU is working perfectly.	YES

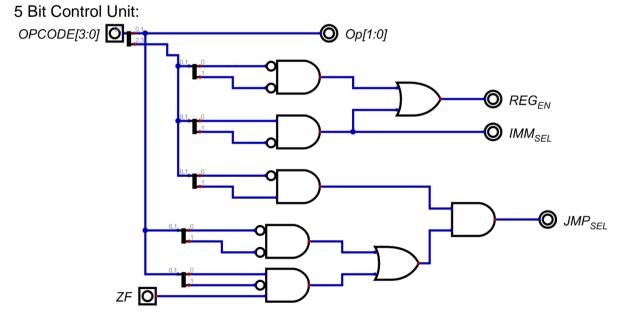
Program Counter:







5bit Control Unit:



Main CPU:

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Register Mode(00) = 2bit (type of operation) + 2bit(op) + 2bit(reg1) + 2bit(reg) + 7bit (don't Care) Immediate Mode(01) = 2bit (type of operation) + 2bit(op) + 2bit(reg1) + 5bit(value) + 4 bit(don't care) jump Mode(10) = 2bit (type of operation) + 2bit(op) + 4bit(add) + 7 bit(don't care) JMP(OP-00), JNC(OP-01) Op(00-01) Op(00) = ADD Op(01) = ROL Op(10) = OR
JE START \Rightarrow 1001000100000
START: OR R1,R1 \Rightarrow 00100101000000
JMP_{TO}: ADD R1,5 \Rightarrow 010001010010100
JMP JMP_{TO} \Rightarrow 1000000100000
                                                                                   WRD WED
                                                                                                 VRD[14:0]
                                   RA2[2:0] ○◀RA2
                                    WR[2:0] ○4WR
                                                                                                                                                                                                                                                                                               ××××× ▶◎ IMM<sub>VAL</sub>[4:0]
                               WRD[14:0] ○4WRD
                                                                                                                                                                                                                                                                                                     R1Þ R1[1:0]
                                            WE O
                                                                                                                                                                                                                                                                                                     R2▶◎ R2[1:0]
                                                                                                                             RD2Þ RD2[14:0]
                                                                                                                                                                                                                                                                                                     R1 Þ WR[1:0]
                                      CLK III CLK
                    PC<sub>EN</sub>
                                                                                                                                                                                                                                                                                                       A▶ A[4:0]
                                                                                                                                                                                                                                                                                                       B▶ B[4:0]
                                                                                                                                                                                                                                                                                                       RÞ⊘ R[4:0]
                                     ZFÞO ZF
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