Joey Negm 4th Year Electrical Engineering Student

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TECHNICAL SKILLS

Engineering Design: Digital Design with HDLs, Hardware Design Validation/Verification, VLSI, ASIC, and SoC Design
Software Proficiency: Linux/Unix, MATLAB, Git, Quartus, Modelsim
Programming Languages: TCL, Python, SystemVerilog, Verilog, C/C++, ARM Assembly
Familiar Concepts : UVM, Digital Circuits (Flip-Flops, Registers, Gates, FSMs), Timing, Operating Systems, Drivers, RISC, Transistors

EDUCATION

University of British Columbia **Expected Graduation May 2027**
Bachelor of Applied Science - Electrical Engineering

TECHNICAL WORK EXPERIENCE

Nokia, Ottawa, ON **September 2025 - Present**
Network Infrastructure Test Software Dev - CPM

- Executing Linux-based regression jobs and developing/debugging TCL/Python automation scripts to validate new hardware and software features for 100+ high-capacity IP routers, ensuring test coverage and system reliability
- Validating secure boot, trust, OS, and firmware mechanisms on CPM (Central Processing Module) testbeds, ensuring firmware authenticity, system integrity, and stable router startup before operation
- Developed a TCL procedure within the secure boot suite to dynamically calculate image file sizes and enforce supported conditions, optimizing test execution while preventing resource overload failures
- Configuring services and accessing network devices via CLI and SNMP, to maintain stable operations across multiple testbeds

NMDC Energy, Abu Dhabi, UAE **Summer 2024**
Electrical Commissioning Intern

- Diagnosed and resolved over 15+ protection function and binary I/O errors by analyzing Digital Logic Diagrams, reducing troubleshooting time by 20% and improving overall system reliability

TECHNICAL PROJECTS

Neural Network Hardware Accelerator, **Individual Project** **December 2024**

- Developed a Nios II SoC with a perceptron for classifying handwritten digits, and displayed results on the FPGA HEX display
- Formulated components to accelerate processing in SystemVerilog, including memory copy and dot product accelerators, with Avalon master and servant interfaces, achieving a 53% reduction in latency
- Created embedded C programs for memory mapped I/O, enabling efficient communication with hardware accelerators
- Enhanced system performance by performing a DMA copy between the SDRAM and SRAM leveraging custom word-copy accelerators, eliminating CPU involvement and freeing up to 10-30% of CPU bandwidth
- Performed validation with ModelSim assertions and Intel Monitor Program to ensure system reliability. Achieved 100% branch/statement test coverage both RTL and Post-Synthesis through mock Avalon interfaces, verifying components

Hardware ARC 4 Decryption Circuit, **Individual Project** **November 2024**

- Designed a hardware implementation of the ARC4 Decryption Algorithm in SystemVerilog. Implemented on the DE1-SOC FPGA using embedded memories and the ready/enable microprotocol, decrypting multiple ciphertexts initialized in memory
- Developed state machines for the Key Scheduling Algorithm and Pseudo-Random Generation Algorithm, implementing complex memory-swapping logic. Validated decryption with 30+ provided encryption keys
- Implemented a brute-force crack algorithm, operating state machines to iteratively search the key space without prior knowledge of the key. Enhanced performance with a parallelized double-crack design, reducing decryption time by 50%
- Validated with ModelSim waveforms and assertions by harnessing RTL and Post-Synthesis testbenches at all stages, achieving 100% branch/statement coverage. Inspected memories with Quartus In-System Memory Editor, ensuring reliability

Simple RISC Machine, **Individual Project** **November 2023**

- Devised a Simple RISC Machine in SystemVerilog with a state machine controlled datapath, integrating 9+ modules such as the ALU, shifter, and registers. Each module was tested, simulated and debugged using ModelSim assertions and waveforms

PID Self-balancing Two-Wheeled Robot, **Group Project** **January 2025 – April 2025**

- Developed a balancing robot with a PID on a microcontroller, achieving ±0.5° tilt accuracy and recovery from 15° disturbances
- Programmed full functionality in embedded C, including Bluetooth communication, complementary filtering for angle estimation, PID motor control, and a graphical dashboard with real-time metrics on dual displays

ENGINEERING DESIGN TEAM

Thunderbikes – Electric Motorbike Design Team, UBC **September 2024 - Present**
Firmware Engineer

- Developed a voltage-sensing function on a STM32 microcontroller using C, allowing for safe operation of the electric motor