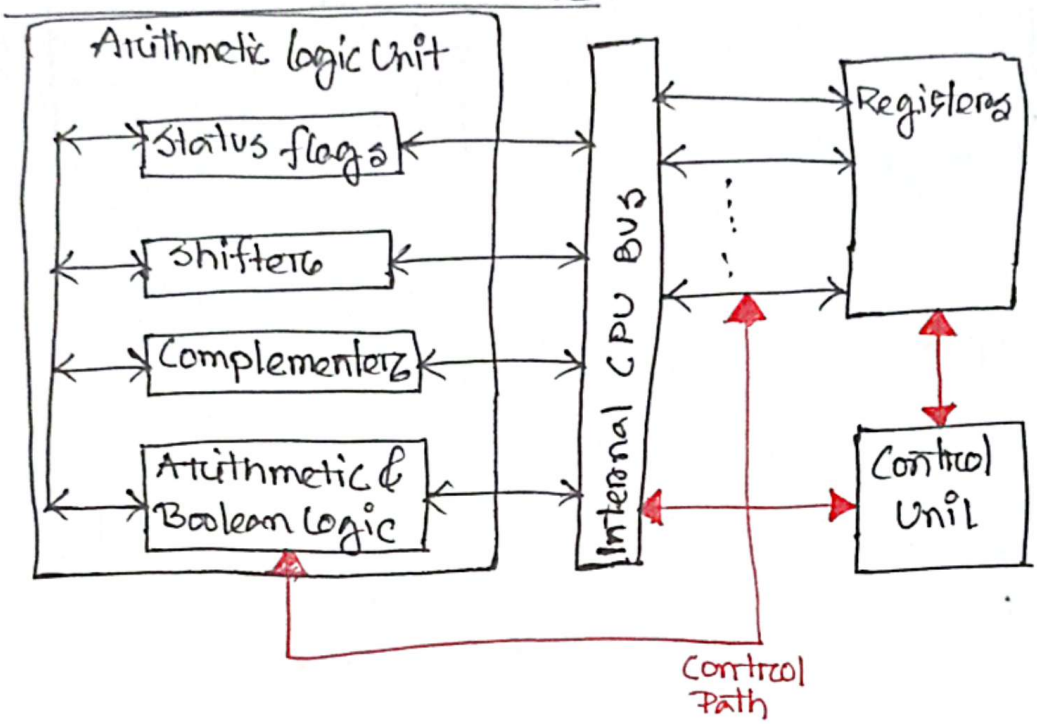
Chap 12 : CPU Structure & Function

☐ CPU — Fetch instruction, Interpret instruction, fetch data, Process data, Write data

CPU internal Structure



☐ Registers

→ CPU must have some temporary storage for work which is called registers.

→ Top level of memory hierarchy (Register, Main memory, Cache memory)

- → User visible register
- → Control & status registers

☐ **User visible Register** — minimize main memory references by optimizing use of registers.

→ General Purpose – can be assigned to a variety of functions
- used for data or addressing
- have restrictions

→ Data Register – only hold data

→ Address Register – segment pointers, Index registers stack pointers

→ Condition Codes – bits set by the processor (flags) - partially visible to the user
-

Control & Status Register is employed to control the operation of the processors (~~Program counter~~)

→ Program Counters – contains the address of the instruction to be fetched

→ Instruction Register – Containes the instruction to be execute.

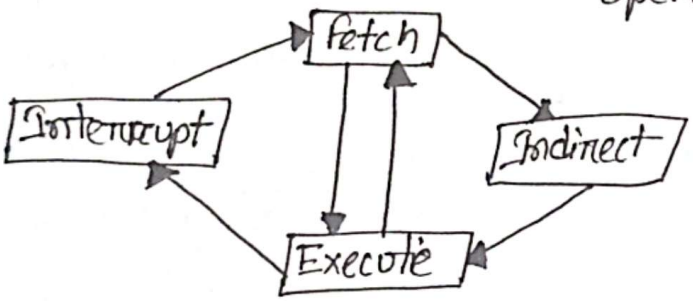
→ Memory Address Register – Contains the address of a location in memory

→ Memory Buffer Register – Contains ~~the~~ data

- Program status words – contains status information
  Sign, Zero, Carry, Equal, Overflow, Interrupt enable/disable, Supervisor

- Supervisor mode – Certain privileged instruction can be executed only in supervisor mode, and certain areas of memory can be accesed only in this mode
  – Used by operating system

- Indirect Cycle – may require memory access to fetch operands



Indirect instruction cycle state diagram:
Slide

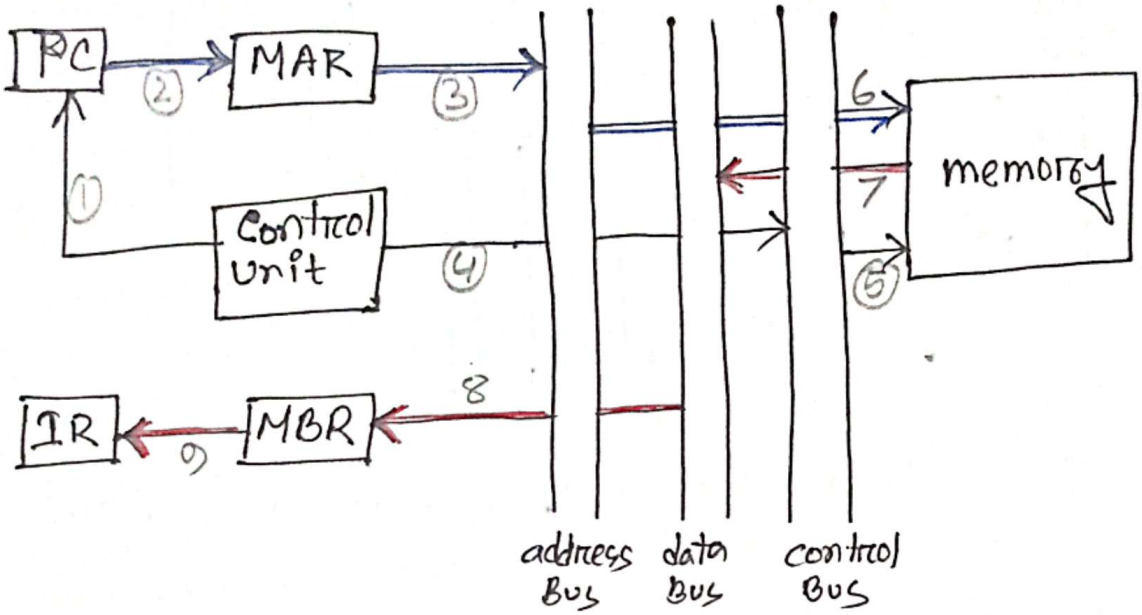
- Data Flow

Instruction fetch = PC contains address of next instruction
→ address moved to MAR → address placed in address bus
→ Control unit requests memory read → Result placed in Data bus → copied to MBR → then to IR
→ PC incremented by 1.

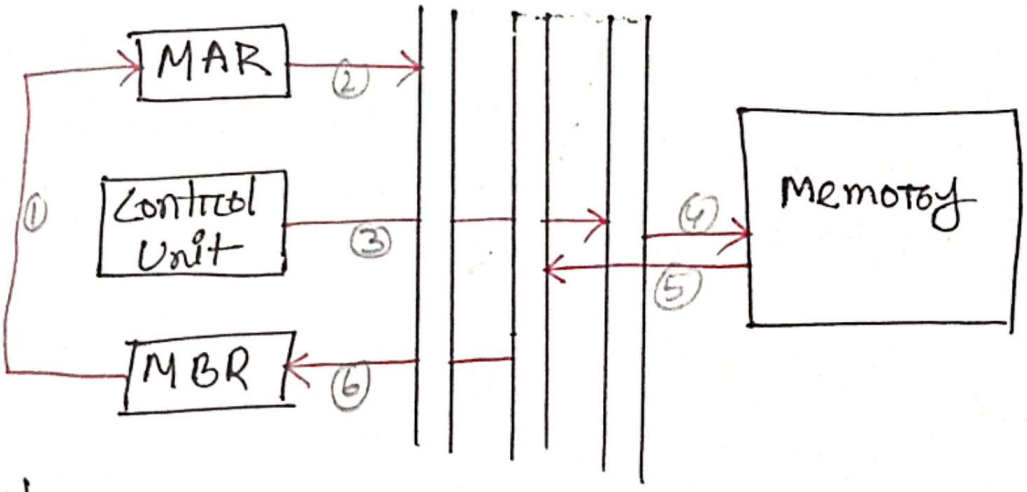
Data fetch = IR is examined, if indirect addressing indirect cycle is performed
→ N most bits ~~are~~ of MBR move to MAR → Control unit

Request memory read → ~~Result~~ result move to MBR

Data flow (fetch diagram)

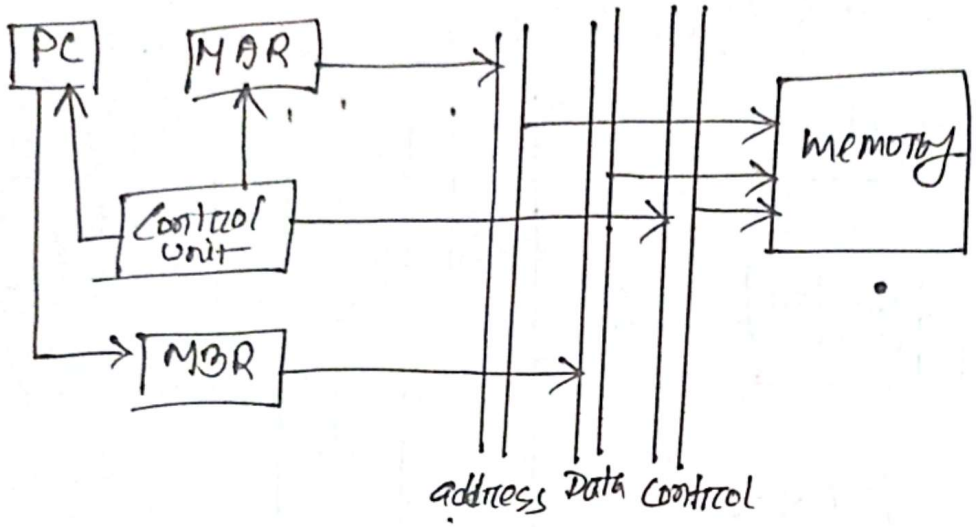


Data flow (indirect diagram)



☐ Execute – Memory Read/Write, Input/Output, Register transfer, ALU operations

□ Data-flow (Interrupt diagram)



PC copied to MBR → MBR written to memory (next instruction saved in memory, so that can resume after handling interrupt)
→ Special memory location loaded in MAR → PC loads with address of interrupt handling routine

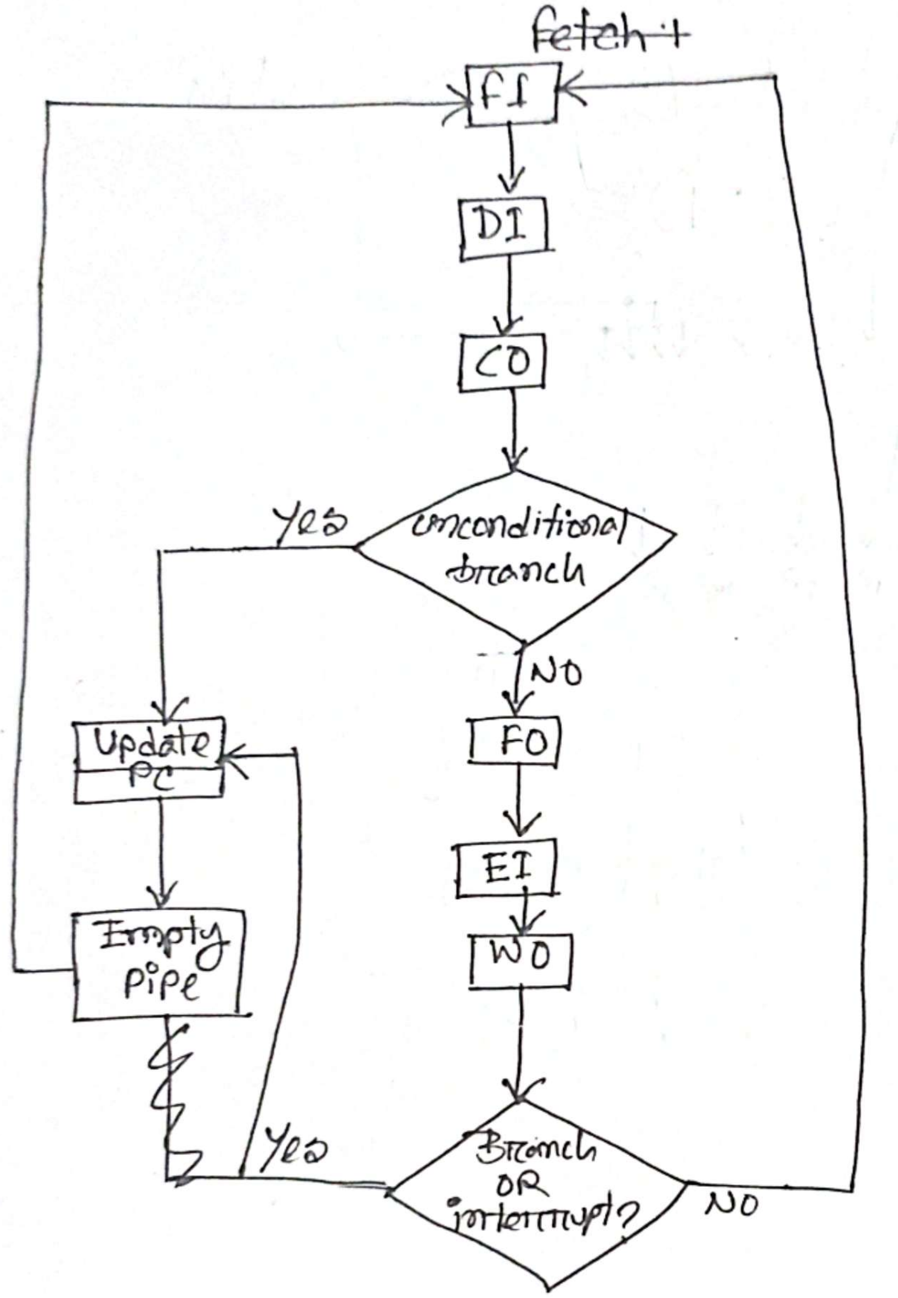
□ Pipelining — fetch instruction (FI), Decode instruction (DI), Calculate operands (CO), fetch operands (FO), Execute instruction (EI), Write result (WR)

1	FI	DI	CO	FO	EI	WO	
2		FI	DI	CO	FO	EI	WO
3			FI	DI	CO	FO	EI	WO

Branch in pipeline — instruction 3 is a conditional Branch to instruction 15,

Diagram (slide)

[1] Six Stage CPU Instruction Pipeline



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