Patuakhali Science and Technology University
Department of Computer Science and Information Technology

4th Semester (Level-2, Semester-I), **Midterm Examination** of **B.Sc. Engg.(CSE)**, July-December/2021, Session: 2019-20

Course Code: CCE-221 Course Title: Digital Logic Design

Full Marks: 15 Duration: 45 minutes

[Figures in the right margin indicate full marks]

Answer all the following questions.

1. Simplify the Boolean function 5

$$F(w, x, y, z) = \sum(1, 3, 7, 11, 15)$$

which has the don't-care conditions

$$d(w, x, y, z) = \sum(0, 2, 5)$$

and show "An expression with the minimum number of literals is not necessarily unique".

2. What are the purposes of arithmetic circuits? Design and describe about a 4-bit full adder with a look-ahead carry generator. 5

3. Design a **logic circuit** to determine a **prime number** ranging **from 0 to 15.** 5

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Patuakhali Science & Technology University (PSTU)
Department of Computer Science and Information Technology(CSIT)
Mid Term Examination: July-December 2022
Course Code: CCE 222 | Course Title: Digital Logic Design Sessional
Session: 2020-21, Program: B.Sc. Engg.(CSE), Semester: 4th

Marks – 15

[Answer all the questions]

1.	Design a circuit that produce output that square of the given input. Use 3 bit input to implement it with NAND gate.	15
2.	*Simplify* $F = A'B'C' + AB'D + A'B'CD'$ and implement it with necessary NOR gates.	15
3.	*Simplify* $F = w'xz + w'yz + x'yz' + wxy'z$ $d = wyz$) *and* implement it with necessary NAND gates.	15
4.	*Simplify* $F(A, B, C, D) = \Pi(0, 2, 3, 5, 7, 8, 9, 10, 11, 13, 15)$ and implement it with necessary logic gates.	15
5.	*Simplify* $F = \Sigma(0, 1, 4, 5, 7, 9, 13)$ *into (a) sum-of-products form, and (b) product-of-sums form* and implement both of its form with necessary logic gates.	15
6.	Show that $A \odot B \odot C \odot D = \Sigma(0, 3, 5, 6, 9, 10, 12, 15)$. and implement it.	15
7	Design a 4 bit full adder .	15

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1. Simplify $F(w, x, y, z) = \Sigma(1, 3, 7, 11, 15)$ which has the don't-care conditions $d(w, x, y, z) = \Sigma(0, 2, 5)$ and show that an expression with the minimum number of literals is not necessarily unique. 7
2. Why code conversion needed? Design a BCD to Excess 5 converter with Boolean function, logic diagram, truth table and proper description. 4
3. Implement following Boolean function using any universal gate $F = ABCD + A'B'C'D + ABC'D' + A'B'CD$. 4

NAND

applying De Morgan's 7

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Dept. of Computer and Communication Engineering
Faculty of Computer Science and Engineering
Patuakhali Science and TechnologyUniversity
Dumki, Patuakhali-8602, Bangladesh

Final Examination of B. Sc. Engineering in CSE Level:2 Semester: II Session: 2020-2021

Course Code	Course Title	July-December	Credit: 03
CCE-221	Digital Logic Design	2022	Time: 03 Hr Marks: 70

Answer any 05 out of 06 Questions (Split answers are highly discouraged)

1 [A.] Simplify $F(w, x, y, z) = \Sigma(1, 3, 7, 11, 15)$ which has the don't-care conditions $d(w, x, y, z) = \Sigma(0, 2, 5)$ and show that an expression with the minimum number of literals is not necessarily unique. 7

[B.] i. Find the complement of the function $F_1=xyz'+x'y'z'$ and $F_2=x(yz'+yz)$ applying De Morgan's theorem. 7

ii. Prove that $f_1=m_1+m_2+m_6+m_7=M_0.M_3.M_4.M_5$.

2 [A.] Consider $F(A, B, C, D) = \Sigma(0, 2, 3, 5, 7, 8, 9, 10, 11, 13, 15)$. Find out and show prime implicants and essential prime implicants by the Karnaugh map from the above expression. 7

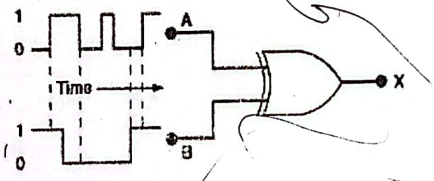
[B.] Simplify the following Boolean function by using the tabulation method: $F = \sum(0, 1, 2, 8, 10, 11, 14, 15)$. 7

3 [A.] A four-bit binary number is represented as $A_3A_2A_1A_0$, where A_3, A_2, A_1, and A_0 represent the individual bits and A_0 is equal to the LSB. Design a logic circuit that will produce a HIGH output whenever the binary number is greater than 0010 and less than 1000. 2

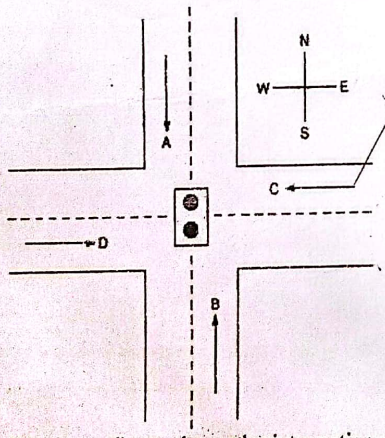
[B.] i. Determine the output waveform for the circuit of figure. 3

ii. Repeat with the B input held LOW.

iii. Repeat with B held HIGH.



[C.] 7



The above figure shows the intersection of a main highway with a secondary access road. Vehicle-detection sensors are placed along lanes *C* and *D* (main road) and lanes *A* and *B* (access road). These sensor outputs are LOW (0) when no vehicle is present and HIGH (1) when a vehicle is present. The intersection traffic light is to be controlled according to the following logic:

i. The east-west (E-W) traffic light will be green whenever *both* lanes *C* and *D* are occupied.
ii. The E-W light will be green whenever *either* *C* or *D* is occupied but lanes *A* and *B* are not *both* occupied.
iii. The north-south (N-S) light will be green whenever *both* lanes *A* and *B* are occupied but *C* and *D* are not *both* occupied.
iv. The N-S light will also be green when *either* *A* or *B* is occupied while *C* and *D* are *both* vacant.
v. The E-W light will be green when *no* vehicles are present.

Using the sensor outputs A, B, C, and D as inputs, design a logic circuit to control the traffic light. There should be two outputs, N-S and E-W, that go HIGH when the corresponding light is to be green. Simplify the circuit as much as possible and show all steps.

[D.] Implement following Boolean function using multilevel NAND gates. 2

$F = A(B + CD) + BC'$

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4. [A.] Define universal gate. Implement a combinational circuit which convert four bit excess 3 code to four bit BCD code. 5

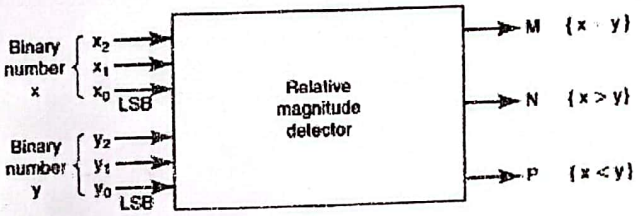
[B.] Define adder. Implement a full-adder circuit with a decoder and two OR gates. From the truth table of the full-adder (Section 4-3), we obtain the functions for this combinational circuit in sum of minterms: S(x, y, z) = ∑(1, 2, 4, 7) 3

$$C(x, y, z,) = \sum(3, 5, 6, 7)$$

[C.] Figure represents a relative-magnitude detector that takes two three-bit binary numbers, $x_2x_1x_0$ and $y_2y_1y_0$, and determines whether they are equal and, if not, which one is larger. There are three outputs, defined as follows: 3

i. M = 1 only if the two input numbers are equal.
ii. N = 1 only if $x_2x_1x_0$ is greater than $y_2y_1y_0$.
iii. P = 1 only if $y_2y_1y_0$ is greater than $x_2x_1x_0$.

Design the logic circuitry for this detector. The circuit has six inputs and three outputs and is therefore much too complex to handle using the truth table approach.

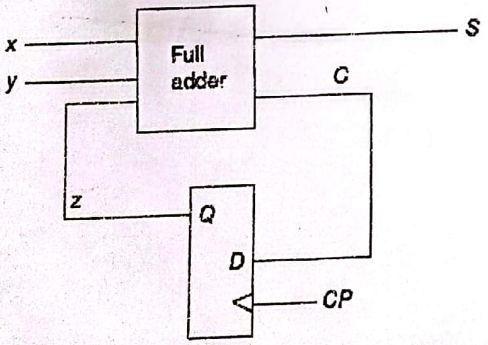


[D.] Define programmable read-only memory. Implement the following function with a multiplexer and demultiplexures and show that the demultiplexure deliveres which was exactly combined by multiplexure. 3

F(A, B,C) = ∑(1,3,5,6)

5. [A.] What is flip-flop? Design a D flip-flop. 2

[B.] 7



The full-adder of figure receives two external inputs *x* and *y*; the third input *z* comes from the output of a *D* flip-flop. The carry output is transferred to the flip-flop every clock pulse. The external *S* output gives the sum of *x*, *y*, and *z*. Obtain the state table and state diagram of the sequential circuit.

[C.] Differentiate between sequential circuit and combinational circuit. What is the problem found in RS flip-flop? Explain how it is solved in JK flip flop. 2

[D.] Bring out the differences between edge triggered and level triggered flip-flip. What is the necessity of mater-slave flip-flop? Explain working of D master-slave flip-flip. Realize with all NOR gates. 3

6. [A.] Define registers. Design a 4-bit register with parallel loading D flip-flops. 3

[B.] What is bidirectional shift register? The content of a 4-bit shift register is initially 1101. The register is shifted six times to the left, with the serial input being 101101. What is the content of the register after each shift? 4

[C.] Define binary ripple counter. Determine and show the count sequence for a binary ripple counter. 3

[D.] Design the basic memory unit architecture showing communication with environment. Show the construction of a Johnson counter. 4

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Patuakhali Science and Technology University

Department of Computer Science and Information Technology

Semester (Level-2, Semester-I), **Midterm Examination** of **B.Sc. Engg.(CSE)**, July-December/2021, Session: 2019-20

Course Code: CCE-221 Course Title: Digital Logic Design

Full Marks: 15 Duration: 45 minutes

[Figures in the right margin indicate full marks]

Answer all the following questions.

1. Simplify the Boolean function 5

$$F(w, x, y, z) = \sum(1, 3, 7, 11, 15)$$

which has the don't-care conditions

$$d(w, x, y, z) = \sum(0, 2, 5)$$

and show "An expression with the minimum number of literals is not necessarily unique".

2. What are the purposes of arithmetic circuits? Design and describe about a 4-bit full adder with a look-ahead carry generator. 5

3. Design a **logic circuit** to determine a **prime number** ranging **from 0 to 15.** 5

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0011
1100

Patuakhali Science & Technology University (PSTU)
Department of Computer Science and Information Technology(CSIT)

Final Examination: July-December 2020

Course Code: CCE 222 | Course Title: Digital Logic Design Sessional

Session: 2018-19, Program: B.Sc. Engg.(CSE), Semester: 4th

Marks – 70

Simulation-10:15

[Answer the marked questions]

Section A (Use Simulator to Implement)

1. Design a combinational circuit which accepts a two-bit number and generates an output binary number equal to the cube of the input number. 20

2. *Implement following Boolean function using exclusive or and AND gates* 20
$F = ABCD + A'B'C'D' + ABC'D' + A'B'CD$

3. With 2 × 1 mux implement XOR gate and AND gate. 20

4. Design a D Flip-flop. 20

5. Design a T Flip-flop. 20

6. Design a circuit that compares two 4-bit numbers, A and B, to check if they are equal. The circuit has one output x, so that x =1 if A = B, and x = 0 if A ≠B . 20

Section B (Use Circuit board to Implement by group work)

7. Design a adder that can add two decimal numbers as following. 30

$$\begin{array}{r} A\,B\,C\,D \\ +P\,Q\,R\,S \\ \hline W\,X\,Y\,Z \end{array}$$

8. Viva-Voce 20

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Patuakhali Science & Technology University (PSTU)

Department of Computer Science and Information Technology(CSIT)

Final Examination: July-December 2021

Course Code: CCE 222 | Course Title: Digital Logic Design Sessional

Session: 2019-20, Program: B.Sc. Engg.(CSE), Semester: 4th

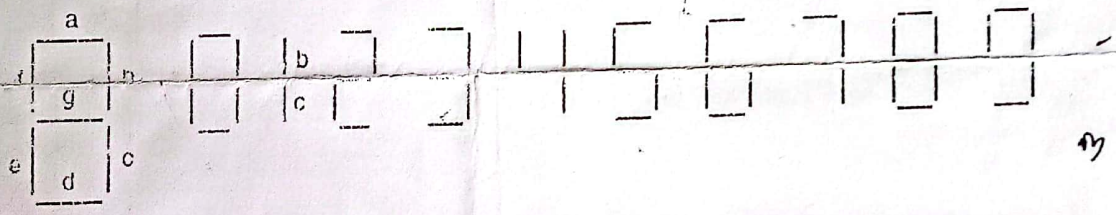
Marks – 70

Section A [Use Circuit board to implement *any questions* by group work]

1. *Implement following Boolean function using NAND or NOR gates*
   $F = ABCD + A'B'C'D' + ABC'D' + A'B'CD$
2. Design a circuit that compares two 4-bit numbers, A and B, to check if they are equal. The circuit has one output x, so that x = 1 if A = B, and x = 0 if A ≠ B .

Section B (Use Circuit board to Implement by group work)

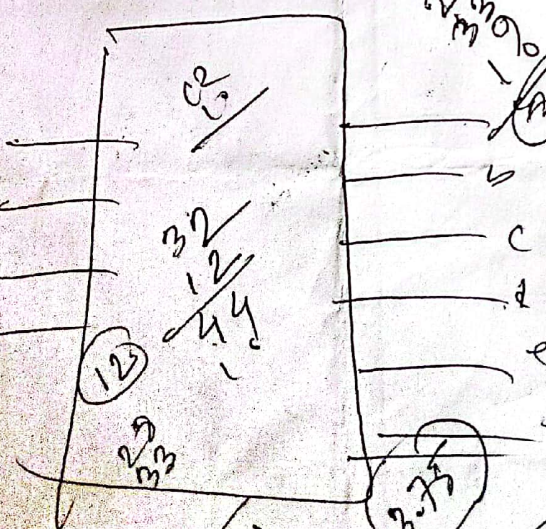
3. Design a BCD-to-seven-segment decoder is a combinational circuit that accepts a decimal digit in BCD and generates the appropriate outputs for selection of segments in a display indicator used for displaying the decimal digit. The seven outputs of the decoder (a, b, c, d, e, f, g) select (a) Segment designation



(b) Numerical designation for display

the corresponding segments in the display as shown in Fig. (a). The numeric designation chosen to represent the decimal digit is shown in Fig. (b). Design the BCD-to-seven-segment decoder circuit.

4. Lab Report
8. Viva-Voce



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Patuakhali Science & Technology University (PSTU)

Department of Computer Science and Information Technology(CSIT)

Mid Term Examination: July-December 2021

Course Code: CCE 222 | Course Title: Digital Logic Design Sessional

Session: 2019-20, Program: B.Sc. Engg.(CSE), Semester: 4th

Marks – 15

[Answer all the questions]

1. A minority gate is a digital circuit whose output is equal to 1 if the minorities of the inputs are 1's.The output is 0 otherwise. By means of a truth table, find the Boolean function implemented by a 3-input minority gate. Simplify the function. 15

2. *Simplify* $F(w, x, y, z) = \Sigma(0, 1, 2, 4, 7, , 8, 9, 12, 13, 15)$ and implement it with necessary logic gates. 15

3. *Simplify* $F = (A'+B+C')(B'+C+D')(A'+B'+C'+D')(A+B'+C')$ and implement it with necessary logic gates. 15

4. *Simplify* $F(A, B, C, D) = \Pi(0, 2, 3, 5, 7, 8, 9, 10, 11, 13, 15)$and implement it with necessary logic gates. 15

5. *Simplify* $F = \Sigma(0, 1, 4, 5, 7, 9, 13)$ *into (a) sum-of-products form, and (b) product-of-sums form* and implement both of its form with necessary logic gates. 15

6. Design a Full-Subtractor. 15

7. Design a 4 bit full adder with look ahead carry generator. 15

9. Design a BCD adder 15

$\boxed{A'C' + C'D + A'BD}$

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Patuakhali Science and Technology University (PSTU)

Department of Computer Science and Communication Engineering (CSE)

Final Examination (LAB), July-December: 2019

Program: B. Sc. Engg.(CSE)

Session: 2017-18

Course Code : CCE-222	Course Title : Digital Logic Design Lab
Full Time: 3 hours	Full Marks: 70

Answer the marked questions

Individual works with Simulator

1.	Design a 4 bit full adder with necessary basic circuit element.	40
2.	Design a BCD to Excess -3 code converter.	40
3.	Design a 4 bit comparator circuit.	40
4.	Design a 4 bit even parity generator circuit.	40
5.	Design a 4 –bit Decimal adder.	40
6.	Design a Hexadecimal to Binary encoder with necessary basic circuit element.	40
7.	Design MUX and DMUX in one board to test the full MUX-DMUX operation.	40
8.	Design a D flip-flop.	40

Group Works

9	A minority gate is a digital circuit whose output is equal to 1 if the minorities of the inputs are 1's. The output is 0 otherwise. By means of a truth table, find the Boolean function implemented by a 3-input minority gate. Simplify the function.	15
10	*Simplify F = Σ (0, 1, 4, 5, 7, 9, 13) into sum-of-products form* implement both of its form with necessary logic gates.	15
11	*Simplify F = Σ (0, 1, 4, 5, 7, 9, 13) into) product-of-sums form* and implement both of its form with necessary logic gates.	15
12	Let F = A'C + A'B + AB'C + BC is a Boolean expression a) Express it in sum of misterms b) Find the minimal sum of products expression and implement both of its form with necessary logic gates.	15
13	Viva-Voce	15

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Dept. of Computer and Communication Engineering
Faculty of Computer Science and Engineering
Patuakhali Science and Technology University
Dumki, Patuakhali-8602, Bangladesh

F-removal Examination of B. Sc. Engineering in CSE Level: 2 Semester: II Session: 2019-2020

Course Code	Course Title	
CCE 221	Digital Logic Design	Credit: 03 Time: 03 Hrs. Marks: 70

Answer any 05 out of 06 Questions (Split answers are highly discouraged)

1 A "An expression with the minimum number of literals is not necessarily unique"-Illustrate the significance of the above statement with appropriate example. 07

1 B 07

I. Convert $(511.4)_{10}$ to base-5 number.

II. Prove that $f_1=m_2+m_1+m_5+m_7=M_0.M_3.M_4.M_6$.

2 A I. What are the advantages and disadvantages of digital techniques over analog technique? 07

II. Simplify the Boolean function $f(w,x,y,z)=\sum(0,1,2,3,4,5,6,7,8,9,10,11,12,14,15)$.

2 B Simplify the Boolean function $F=A'B'C'+B'CD'+A'BCD'+AB'C'$ and implement the resultant using logic gates. 07

3 A I. Define combinational circuit. Design a combinational circuit that accepts a three-bit binary number and generates an output number equal to the square of the input number. 07

$B_1=A_1$ $B_2=B_0$ $B_3=A_2\bar{A}_1$ $B_4=A_2(A_2\oplus A_3)$ $B_5=A_3(A_1+\bar{A}_2)$ $B_6=A_3A_2$

II. Design a full adder using half adder with mathematical backgrounds.

3 B Design and describe the mechanism of a magnitude comparator circuit for 4-bit binary numbers $A=A_3A_2A_1A_0$ and $B=B_3B_2B_1B_0$. The outputs are F, G, and H, I, J, K where F is 1 if A>B, G is 1 if A=B,H is 1 if A<B, I is 1 if A>=B, J is 1 if A<=B, K is 1 if A!=B. 07

4 A Define decoder. Design and describe the mechanism of a BCD adder circuit. 07

4 B Why multiplexer is needed? Design and describe the mechanism of a 4-bit multiplexing and demultiplexing technology with synchronizing control. 07

5 A i. Define Synchronous and Asynchronous sequential circuits with example. 07

ii. Design a JK flip-flop with its characteristics table and equation. pag-208

5 B Define register. Design a 4-bit register with parallel load using D flip-flop. 07

SRnn

6 A i. Design a serial adder using a sequential logic procedure. 07

ii. Design a 4-bit binary ripple counter using flip-flops that trigger on the positive edge.

6 B What is the difference between serial and parallel transfer? The content of a 4-bit shift register is initially 1101. The register is shifted eight times to the right, with the serial input being 101101. What is the content of the register after each shift? 07

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Patuakhali Science & Technology University (PSTU)
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Mid Term Examination: July-December 2021
Course Code: CCE 222 | Course Title: Digital Logic Design Sessional
Session: 2019-20, Program: B.Sc. Engg.(CSE), Semester: 4th

Marks – 15

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6. Design a Full-Subtractor. 1

7. Design a 4 bit full adder with look ahead carry generator. 1

9. Design a BCD adder

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