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Chap of Input/output problems

1/0 Module - is a handwarre interface that connects the CPU and main memoring to peruphenal devices (such as keyboard, printlers, diskets)

Why it is necessarily?

- 1) There are a wide raisety of peraphenals with various methods of operation.
- 2) The data transfer rate of peruphercals is much slowers

 Than that of the processor on memores.
- 3) data transfer of some perciphercals is fasters than that of the memority or porcocessors
- Pripherals often use different data formats and word lengths than the compoters to which they are attached.

It would be improactical to connect perciphercals directly to the system bus.

50 an 1/0 module 95 trequitted.

由 1/0 Module has two major function

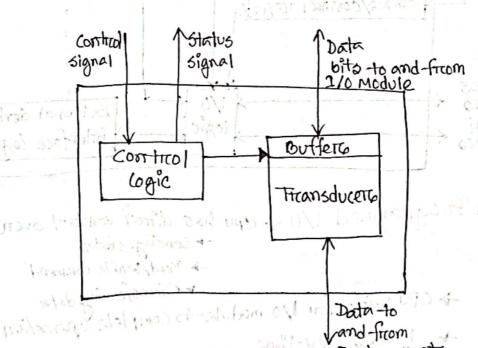
- 1) Interface to the processor and memores
- 2) Interface to one on morre percipheral devices.

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Percipheral - An external device connected to the CPU and memortry through 1/0 Module is called percipheral device.

Classify pherapherral device into 3 categories:

- The computers users. (screen, printers, key board)
- 2 Machine Readable Suitable Forto communicating with equipment. (Monitoring and coor trol)
- 3 Communication switable for communicating with tempte device (Modern, NIC)



Control signal -> determine - the function that the device will personm.

status signal -> indicate the state of the device.

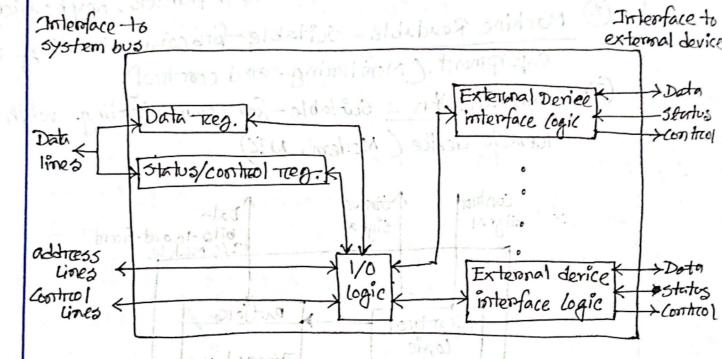
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I/O Module-function:

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- 1- Control and-timing
 - 2 Processor communication
 - 3. Derice communication
 - 4 Data buffering
 - 5 Erosors detection



1 Programmed 1/0 + cpu has direct control over 1/0

- + sensing status
- Read/wrute command
- + CPU waits for 1/0 module to complete operation
- → Wastes CPU+fine

I cpu requests 1/0 operation -> 1/0 module performs operation

- -> 1/0 module sola stolus tolo -> CPU checks stolus bits periodically
- into module does not inform CPU directly -> 1/0 module does not into motor cpu -> CPU may wait on come seck laken.

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- on 1/0 module may treceive when addressed by processor
 - 1) Control Used to activate a peruphetral and tell what to do
 - 2) Test Used to test various status conditions
- 3) Read Causes the Vo module to obtain an item of data from the perupheral
- 4) White Causes the 1/0 module to take an item of data from the data bus

1/0 Mapping stolen with

- 1) Memorey mapped 1/0- Device and memorey share an address space
 - 1/0 Looks just like memores Tread/white
 - No specific command for 1/0
- 2) Isolated 1/0 separcate address space
 - Meed 100 organisme morry select line
 - Specia! commands-for 1/0

I Interrupt Driver 1/0 - Overcomes CPU wait

- No trepeated cou checking of device
 - 1/0 module intermupts when tready
- Derupherial, (PU does other work -> 1/0 module intermupt CPU -> CPU - Trequests data -> module transfers data

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Mich device issued interment Design Issue < XD if multiple intermost occurred, how does the processors decide which one to proce

4 general categories of techniques are in common use:

- @ Multiple interruppt lines between the processors and the 1/0 modules (impregetical)
- 2) Software poll, When the processors detects an interrupt, it branches to an interrupt-service Troutine whose Job it is to poll each 1/0 module to determine which module caused the interrcupt.
- 3 Daisy Chain CPU when senses an interrrupt, it send a intermost acknowledge, ine requesting module tresponds by placing a vector on the data lines, Dector -> address of the CPU-1/0 module on unique identifiers.
- 9 Bus Masters I/O module most finst gain control of the bus, only one module can maise the line of time.

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The taguesting module than places its rectors on the data lines. When motte I objetimental alcham

CS CamScanner

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OPC BUS -

- -> 80x 860 was 1 intermupt line
- → 8086 use .8259 A gotennupt controllers
- > 8259A Nas 8 gartenocupt lines

8250 A accepts intensupts -> determines priority -> raises

INTR line -> CPU acknowledges -> 8250 A put connect

rectors on data bus -> CPU priocess intensupt