ES204 Digital Systems
LAB Assignment - 7

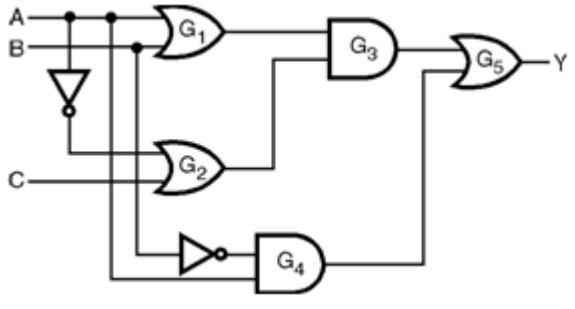
Indian Institute of Technology, Gandhinagar
February 27, 2024

Marks : 30

Submission instructions:

Only one student from the team will submit with the word doc name Rollno1_Rollno2.pdf. The PDF will contain the code, testbench and simulation results.

1. Implement the following circuit in Verilog in such a way that all the hazards can be viewed. Write the testbench such that all the static and dynamic hazards in the following circuit can be shown on the simulator. You can use appropriate delay values.



ES – 204 Digital Systems

Lab Assignment VII

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Static Hazard

Main file:

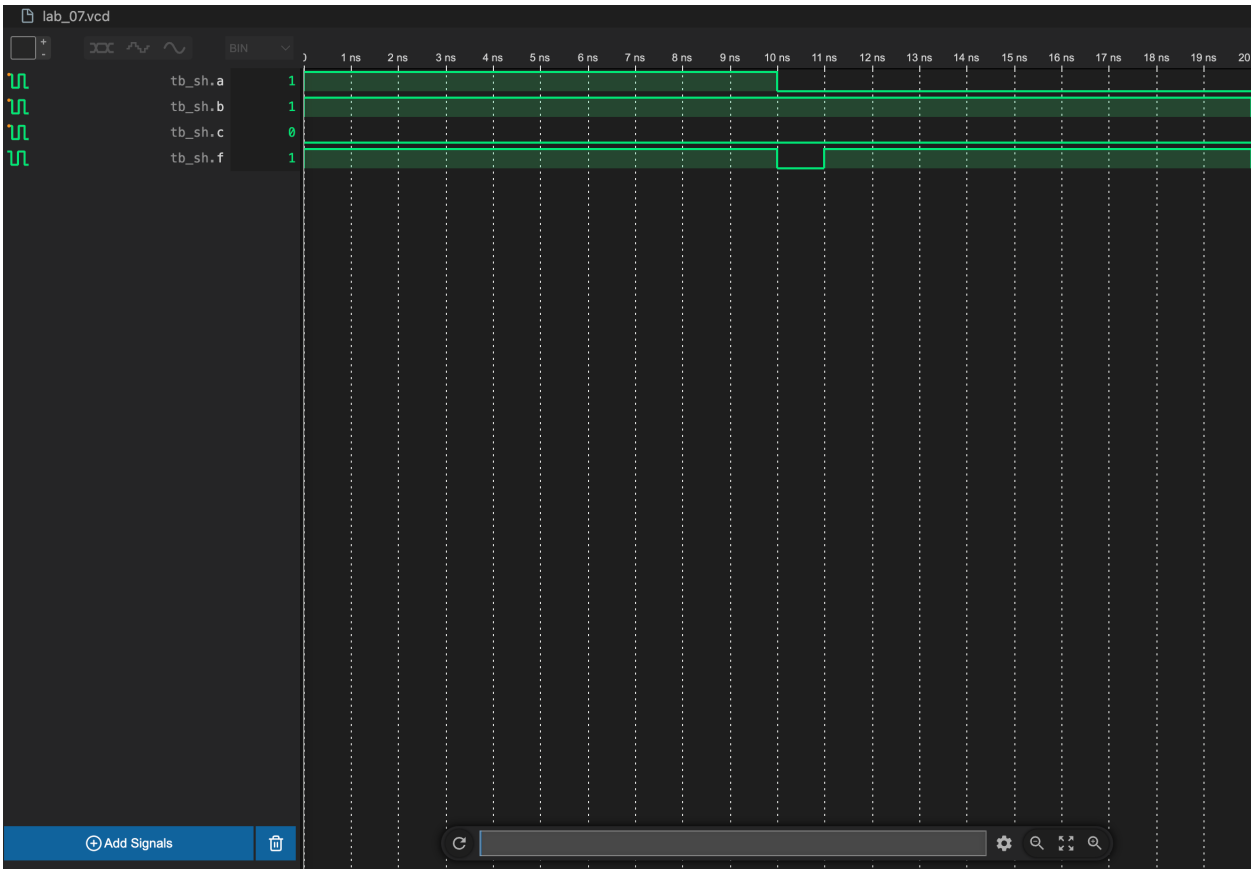
```
module sh(input a, input b, input c, output f);

wire na, nb, o1a, o2a, o3a, a1a, o4a;

not #(1) n1 (na, a);
not #(1) n2 (nb, b);
or #(0) o1 (o1a, a, b);
or #(0) o2 (o2a, na, c);
or #(0) o3 (o3a, a, nb);
and #(0) a1 (a1a, o1a, o2a);
or #(0) o4 (f, o3a, a1a);

endmodule
```

Test bench:

```
`timescale 1ns / 1ps

`include "lab_07.v"
module tb_sh;

reg a, b, c;
wire f;
```

```
sh uut (.a(a), .b(b), .c(c), .f(f));

initial begin

    $dumpfile("lab_07.vcd");
    $dumpvars(0, tb_sh);

    a = 1; b = 1; c = 0; #10;
    a = 0; b = 1; c = 0; #10;

    $finish();
end
endmodule
```

Simulation Results:



Dynamic Hazard

Main file:

```
`timescale 1ns / 1ps

module sh(input a, input b, input c, output f);

wire na, nb, o1a, o2a, o3a, a1a, o4a;

not #(1) n1 (na, a);
not #(6) n2 (nb, b);
or #(3) o1 (o1a, a, b);
or #(6) o2 (o2a, na, c);
and #(7) a1 (a1a, o1a, o2a);
and #(2) a2 (a2a, nb, a);
or #(1) o4 (f, a1a, a2a);

endmodule
```

Test bench:

```
`timescale 1ns / 1ps

`include "sh.v"
module tb_sh;

reg a, b, c;
wire f;

sh uut (.a(a), .b(b), .c(c), .f(f));

initial begin

    $dumpfile("shtb.vcd");
    $dumpvars(0, tb_sh);

    a = 0; b = 0; c = 0;
    #100 a = 1; b = 1; c = 1;
    #100
    $finish();
end
endmodule
```

Simulation Results: