ES204 Digital Systems
LAB Assignment - 3

Indian Institute of Technology, Gandhinagar
January 23, 2024
Time & Venue: Tuesday 8:30-9:50am [7/108]

Submission deadline: Jan 23, 2024 (9:50 am)
Marks : 20

For each of the questions, write a Verilog code. You also need to create a **testbench** and show the simulation results.

[20 Marks]
Implement at 4-bit shift register. Observe the circuit that will result if you use blocking statements versus non-blocking statements. Show the schematic of both of the designs for comparison.