ES204 Digital Systems
Compensation Lab

Indian Institute of Technology, Gandhinagar
February 26, 2024
Time & Venue: Monday 11:30-12:50pm [7/109]

Submission deadline: Feb 26, 2024 (12:50 pm)
Marks : 20/40

Submission instructions: Only one student from the team will submit with the word doc name Rollno1_Rollno2.pdf. The PDF will contain the code, testbench and simulation results, XDC and FPGA snapshots. After synthesis, report power, LUT utilization and timing reports. You can take snapshots or save them as text files and add in the report.

Implement a Synchronous MOD-13 up/down counter with asynchronous reset, and with parallel load. Show the counter values on the LEDs. The inputs for loading the counter needs to be given from the keypad.

Note: Those of you who have missed any of the Labs1-4, need not implement the parallel load feature.

You should use the clock divider module to show the LEDs changing at a slower rate. This is uploaded on the classroom. Also, for the XDC file, please refer to the document uploaded on the classroom.