ES204 Digital Systems
LAB Assignment - 2

Indian Institute of Technology, Gandhinagar
January 16, 2024
Time & Venue: Tuesday 8:30-9:50am [7/108]

Submission deadline: Jan 16, 2024 (9:50 am)
Marks : 20

For each of the questions, write a Verilog code. You also need to create a **testbench** and show the simulation results.

[20 Marks]

1. Implement a 1-bit full adder design using structural code. Write a testbench and show the simulation results for all cases.

2. Use this 1-bit structural code to design 4-bit parallel adder. Write a testbench for random inputs and check for 4 different cases.