ES204 Digital Systems
LAB Assignment – 4

Indian Institute of Technology, Gandhinagar
January 31, 2024
Time & Venue: Tuesday 8:30-9:50am [7/108]

Submission deadline: Jan 31, 2024 (9:50 am)
Marks : 20

For each of the questions, write a Verilog code. You also need to create a **testbench** and show the simulation results.

[20 Marks]

Design a 4-bit Synchronous Down counter with preset using structural code. You need to design a "Toggle FF with preset" module using procedural statement (always @). Use TFFs and other gates to implement the Synchronous counter.

The preset signal initializes the Counter to 1111.

Lab 4 ES 204

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#Structural implementation code of 4-bit Synchronous Down counter with preset

1. Code

```
`timescale 1ns / 1ps
module T_ff(
//T flopflop with always block
    input clk, preset, reset, T,
    output reg Q
    );
    always@(posedge clk, negedge preset)
    begin
    if(!reset)
        Q <= 0;
    else if (!preset)
        Q <= 1;
    else
        Q <= T ^ Q;
    end
endmodule
module Down_counter(
     input clk, reset, preset,
     output [3:0] Q
    );

    wire [3:0] T;
    and(T[0], 1,1);
    and(T[1], ~Q[0], 1);
    and(T[2], ~Q[0], ~Q[1]);
    and(T[3], ~Q[0], ~Q[1], ~Q[2]);
    T_ff inst1(.clk(clk), .preset(preset), .reset(reset), .T(T[0]), .Q(Q[0]));
    T_ff inst2(.clk(clk), .preset(preset), .reset(reset), .T(T[1]), .Q(Q[1]));
    T_ff inst3(.clk(clk), .preset(preset), .reset(reset), .T(T[2]), .Q(Q[2]));
    T_ff inst4(.clk(clk), .preset(preset), .reset(reset), .T(T[3]), .Q(Q[3]));

endmodule
```

2. Test bench

```
`timescale 1ns / 1ps
module down_counter_tb();
    reg clk;
    reg reset;
    reg preset;
    wire [3:0] Q;
    Down_counter uut(.clk(clk), .reset(reset), .preset(preset), .Q(Q));
    initial
    begin
    clk = 1;
    forever #5 clk = ~clk;
    end
    initial
    begin
    reset = 1; preset = 0;
    #10;
    reset = 1; preset = 1;
    #100;
    reset = 1; preset = 0;
    #10;
    reset = 1; preset = 1;
    #200;
    $finish();
    end
Endmodule
```

3. Simulation