ES204 Digital Systems
LAB Assignment – 4

Indian Institute of Technology, Gandhinagar
January 30, 2024
Time & Venue: Tuesday 8:30-9:50am [7/108]

Submission deadline: Jan 30, 2024 (9:50 am)
Marks : 20

For each of the questions, write a Verilog code. You also need to create a **testbench** and show the simulation results.

[20 Marks]

Design a 4-bit Asynchronous counter with reset using structural code. You need to design a Toggle FF module using procedural statement (always @).