ES204 Digital Systems
LAB Assignment - 5

Indian Institute of Technology, Gandhinagar
February 7, 2024
Time & Venue: Tuesday 8:30-9:50am [7/108]

Submission deadline
February 7, 2024 (9:50 am)
Marks : 30

Submit the following: Verilog code, Testbench, Simulation waveforms, FPGA implementation pic and XDC (constraint) file pic.

[20 Marks]
Design a 4-bit comparator that has 2 outputs f, g. The 4-bit comparator has A[3:0] and B[3:0] inputs, and a single output f. A>B, f=1, g=0, and if A<B, g=1, f=0.
Take A and B from the input switches and show f and g on the LEDs.

You have to synthesize and show the implementation on FPGA.

Lab 5 ES 204

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#Behavioural implementation code of 4-bit comparator

1. Code

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 07.02.2024 03:09:25
// Design Name:
// Module Name: comparator_4bit
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module comparator_4bit(
    input [3:0] A,B,
    output reg f, g
    );
    always@(*)
    begin
    if(A > B) begin
    f = 1;
    g = 0;
    end
    else if (A < B) begin
    f = 0;
```

```
    g = 1;
    end
    else
    begin
    f = 0;
    g = 0;
    end
    end
endmodule
```

2. Test Bench

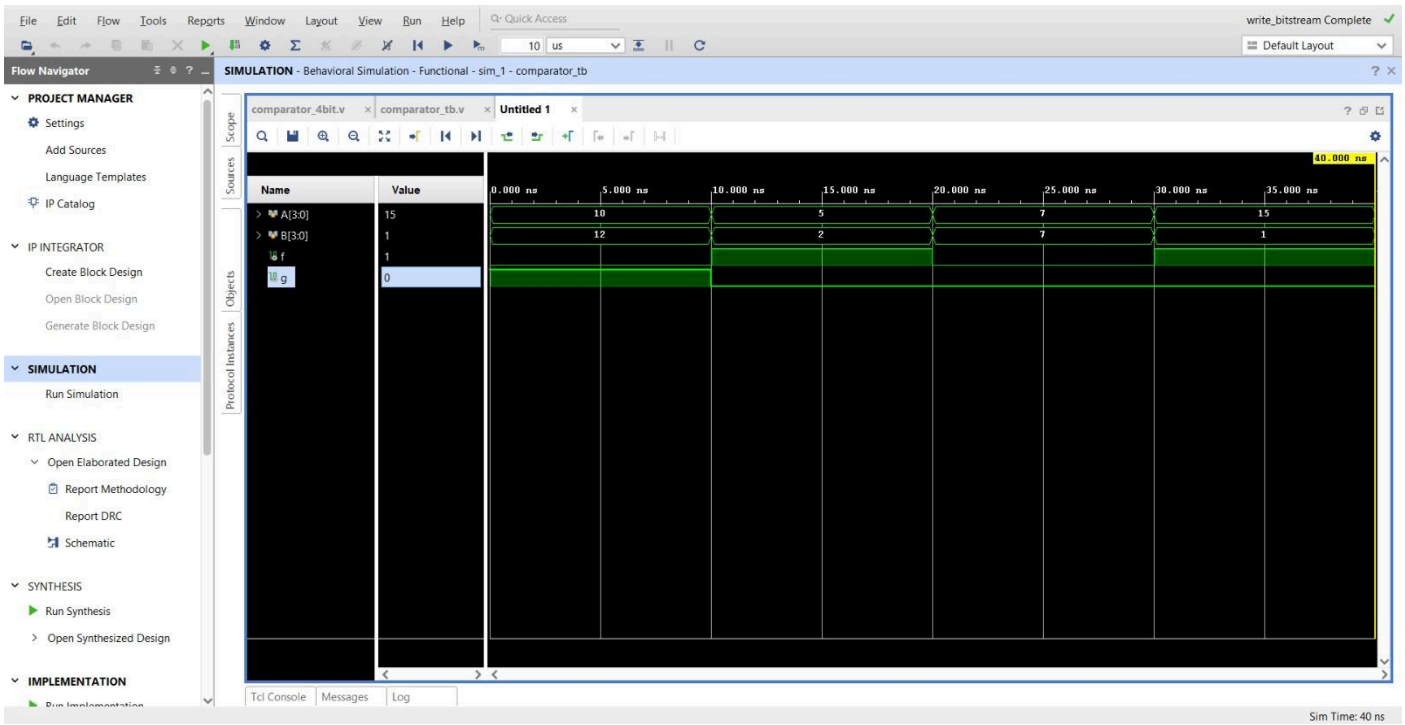
```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 07.02.2024 03:15:19
// Design Name:
// Module Name: comparator_tb
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module comparator_tb();
    reg [3:0] A,B;
    wire f, g;
    comparator_4bit uut (.A(A), .B(B), .f(f), .g(g));
    initial
    begin
    A = 10; B = 12;
```

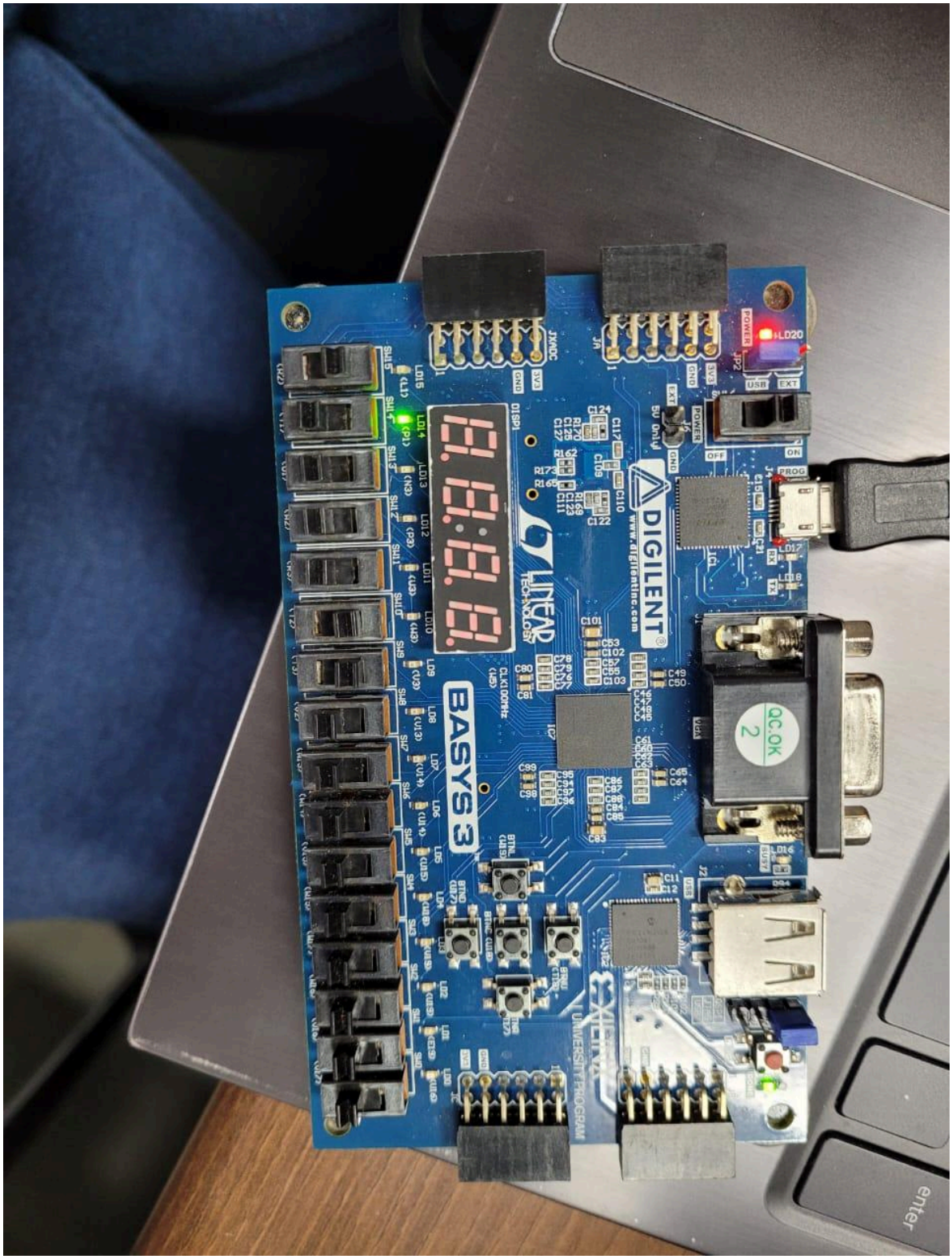
```
    #10;
    A = 5; B = 2;
    #10;
    A = 7; B = 7;
    #10;
    A = 15; B = 17;
    #10;
    $finish();
    end

endmodule
```

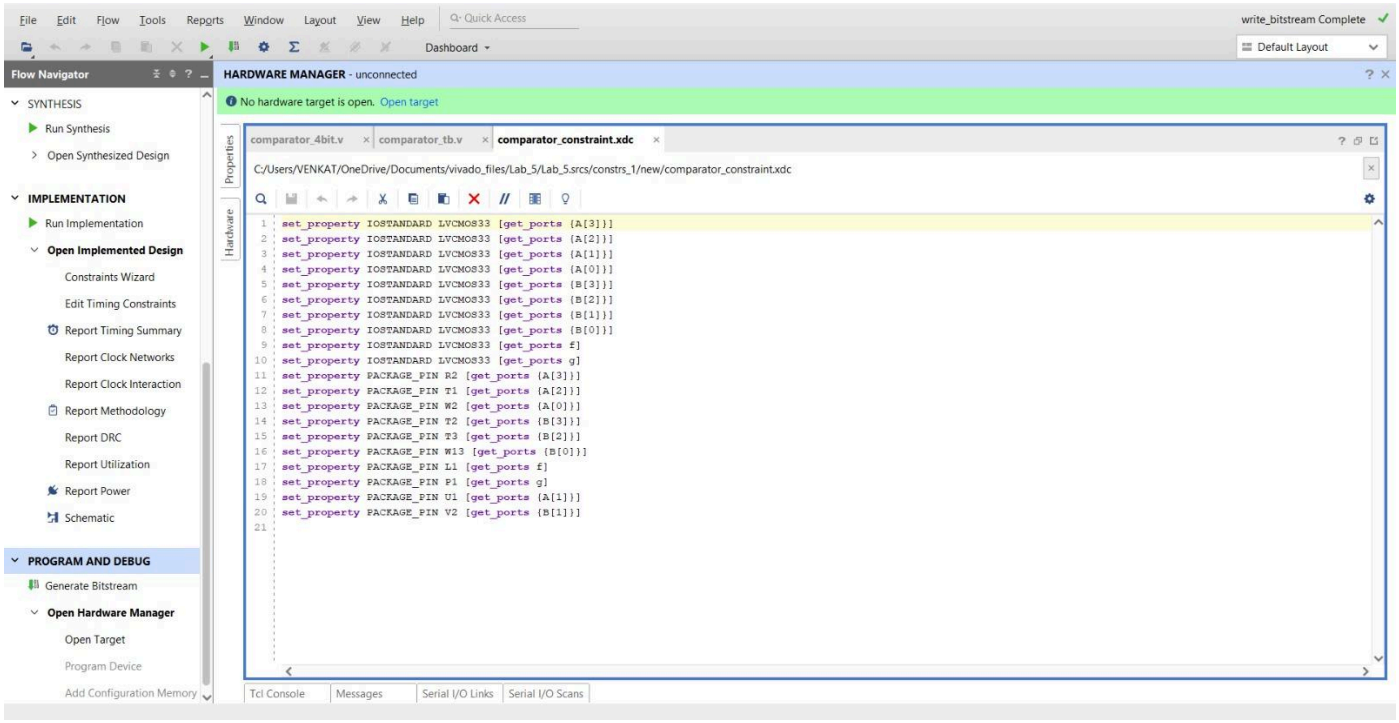
3. Simulation Results



4. Circuit Board



5. XDC File


File Edit Flow Tools Reports Window Layout View Help
Quick Access
write_bitstream Complete
Dashboard
Default Layout
Flow Navigator
HARDWARE MANAGER - unconnected
No hardware target is open. Open target
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Utilization
Report Power
Schematic
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Open Target
Program Device
Add Configuration Memory
comparator_4bit.v
comparator_tb.v
comparator_constraint.xdc
C:/Users/VENKAT/OneDrive/Documents/vivado_files/Lab_5/Lab_5.srcs/constrs_1/new/comparator_constraint.xdc
set_property IOSTANDARD LVCMOS33 [get_ports {A[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {A[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {A[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {A[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {B[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {B[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {B[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {B[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports f]
set_property IOSTANDARD LVCMOS33 [get_ports g]
set_property PACKAGE_PIN R2 [get_ports {A[3]}]
set_property PACKAGE_PIN T1 [get_ports {A[2]}]
set_property PACKAGE_PIN W2 [get_ports {A[0]}]
set_property PACKAGE_PIN T2 [get_ports {B[3]}]
set_property PACKAGE_PIN T3 [get_ports {B[2]}]
set_property PACKAGE_PIN W13 [get_ports {B[0]}]
set_property PACKAGE_PIN L1 [get_ports f]
set_property PACKAGE_PIN P1 [get_ports g]
set_property PACKAGE_PIN U1 [get_ports {A[1]}]
set_property PACKAGE_PIN V2 [get_ports {B[1]}]
Tcl Console
Messages
Serial I/O Links
Serial I/O Scans