# ES204 Digital Systems
# LAB Assignment - 6

Indian Institute of Technology, Gandhinagar
February 13, 2024

**Submission deadline: February 13, 2024**
**Marks : 40**

**Submission instructions:**

**Only one student from the team will submit with the word doc name Rollno1_Rollno2.pdf. The PDF will contain the code, testbench and simulation results, XDC and FPGA snapshots.**
**After synthesis, report power, LUT utilization and timing reports. You can take snapshots or save them as text files and add.**

Design a 4-bit combined BCD/Binary Up/Down counter using behavioral style of coding. Implement it on FPGA and show the counter outputs. (The counter can be assumed to switch between the modes in valid states. For instance, the counter will not switch to BCD if the count is non-BCD).