SONY

IMX273 / IMX287

Support Package

The data except this specification conform to those of IMX273, IMX287.

1. Description

This support package is intended to support product development.

2. Description Items

- ◆Guideline for designing the printed circuit board
- ◆Low voltage serial LVDS output interface
- ◆Communication port (4-wire serial)
- ◆Communication port (I^2C)
- ◆Pattern Generator (PG) function
- ◆How to get sensor information
- ◆Lens design guideline
- ◆FD white spots
- ◆FAQ

Rev. 1.0

Contents

3. Guideline for designing the printed circuit board

In this section we explain the design guideline of the printed circuit board layout and mount.

3.1. Application circuit.

3.1.1. Power supply pins

(1). Please design the suitable filter in power supply line to reduce influence of a power supply noise and to prevent an unnecessary radiation. Especially, the parts to analog power supply pin need to choose the one that is small direct current resistance because that pin is sensitive to the voltage change. The voltage change becomes the factor of horizontal line noise.

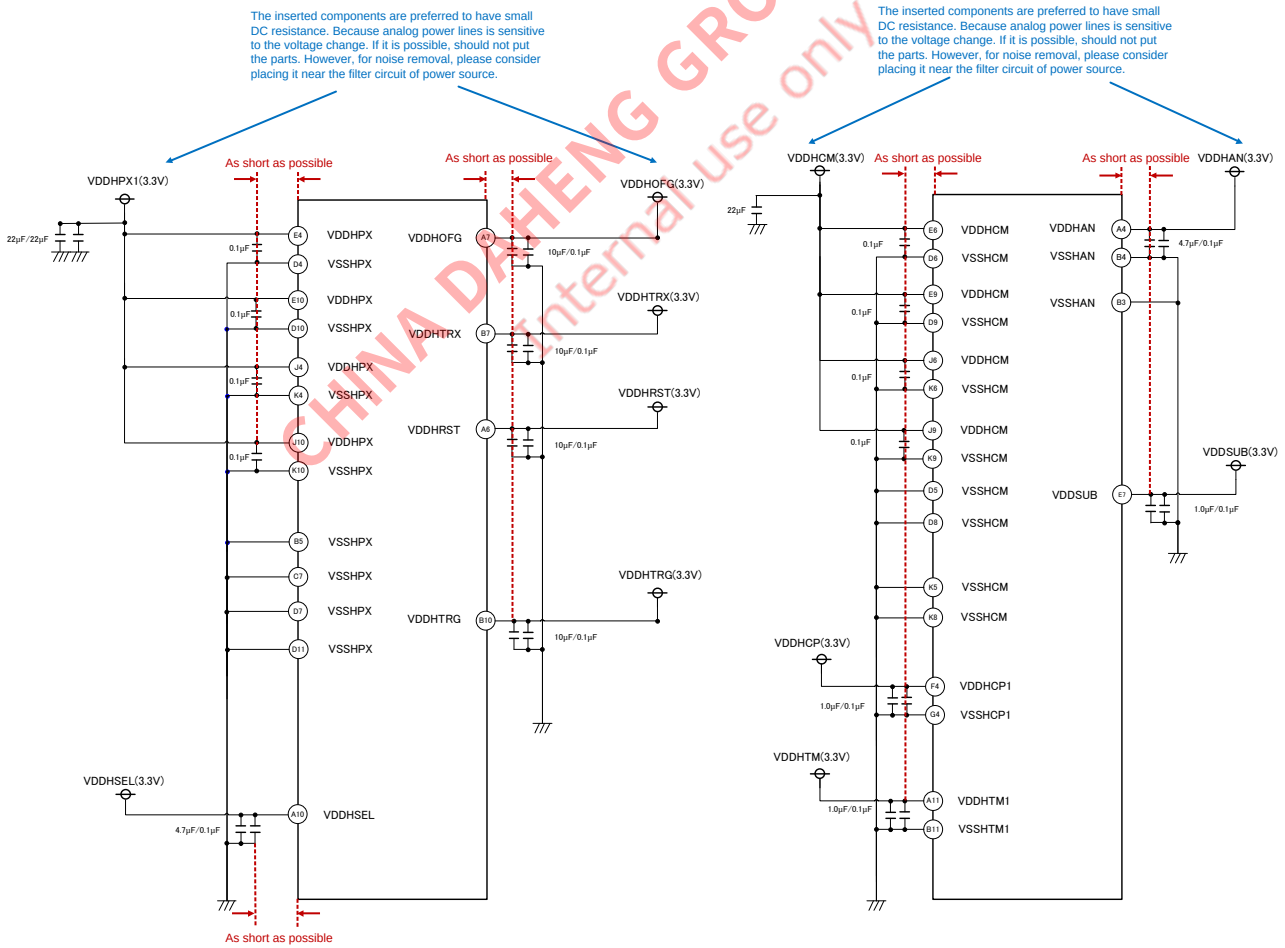
(2). We suggest that the use of reasonable noise filters on the power-line for suppressing the radiation noise from the lines.

(3). E4, E10, J4, J10, A4.Pin (Analog 3.3V) is sensitive signals for noise. So these pins and other power supply should not have the common impedance.

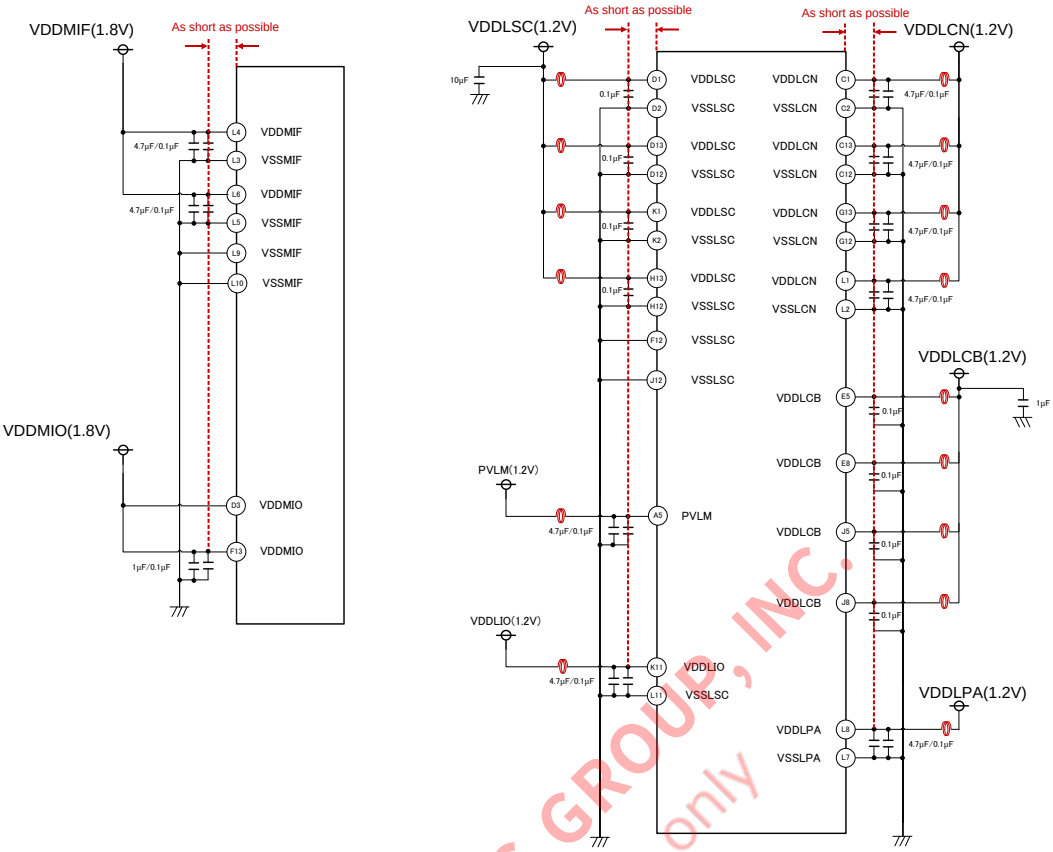
(4). Please mount peripheral parts (capacitor) near the element as much as possible.

(5). Please make patterns of Power supply (3.3V, 1.8V, 1.2V) as wide as possible.

(6). Please put capacitors at each power pin. And avoid putting a capacitor of total capacity value at multiple pins in order to reduce parts.

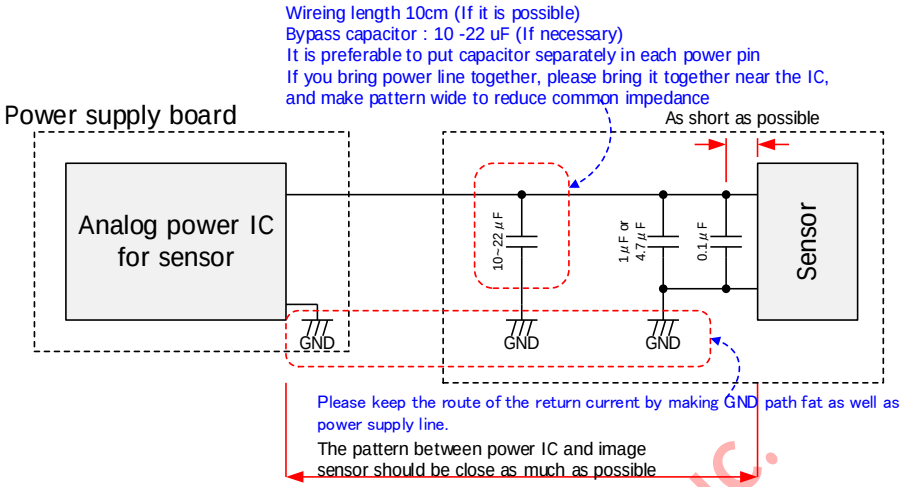


Reference design for analog power supply pins.



Reference design for digital power supply pins.

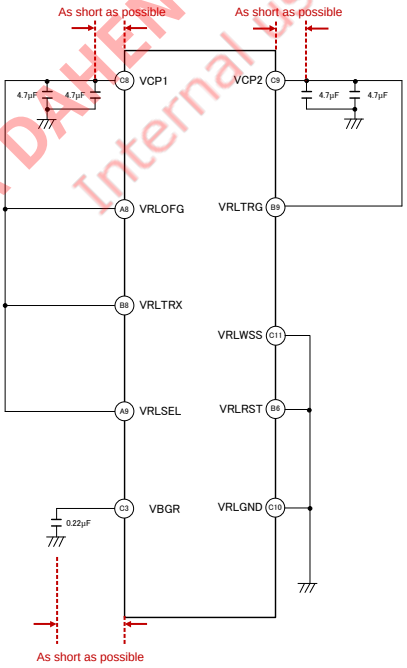
(7). We recommend to implement the power supply IC as close to the sensor as possible. If cannot, use wider power supply pattern of lower DC resistance, implement the large (10uF or more) decoupling capacitor close to the sensor. With regard to pattern, please refer to “3.3. Notes for designing pattern of printed circuit board”.



Layout of power supply IC and decoupling capacitors of large capacity

3.1.2. Other Pins

VCP1, VCP2, VBGR pin is sensitive to noise. Please place the capacitors near the pins. As for the capacity of a capacitor, it is desirable to insert the value according to the example of an application circuit.



Reference design for other pins.

3.2. (Reference) Component

The following describes the components used reference information. When in actual use, please contact the manufacture for each component.

3.2.1. Power supply IC

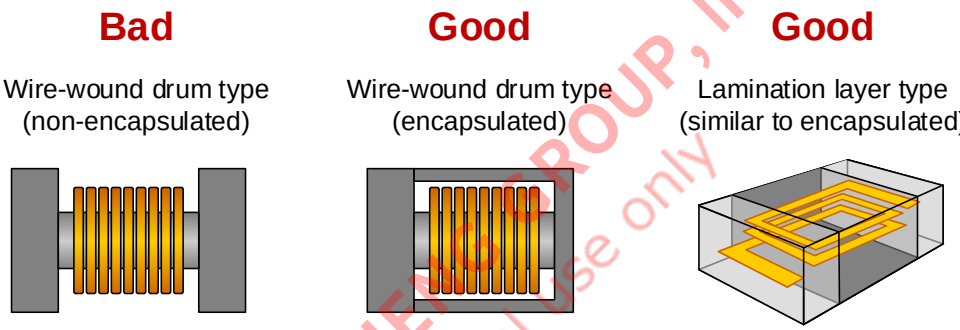
Please select the power supply IC of better PSRR characteristics. Fluctuation of the power supply voltage will cause the horizontal line noise. In that case, we recommend that you use a series regulator.

Please note that when using switching power regulator of the following points.

(1). When using switching power regulator, magnetic field inducted by inductor might cause the noise of the image.

(2). Encapsulated (shield) type inductor is recommended.

(3). Mounting direction of the inductor also affects (increase or decrease) the noise level.



Encapsulated/non-encapsulated type inductor

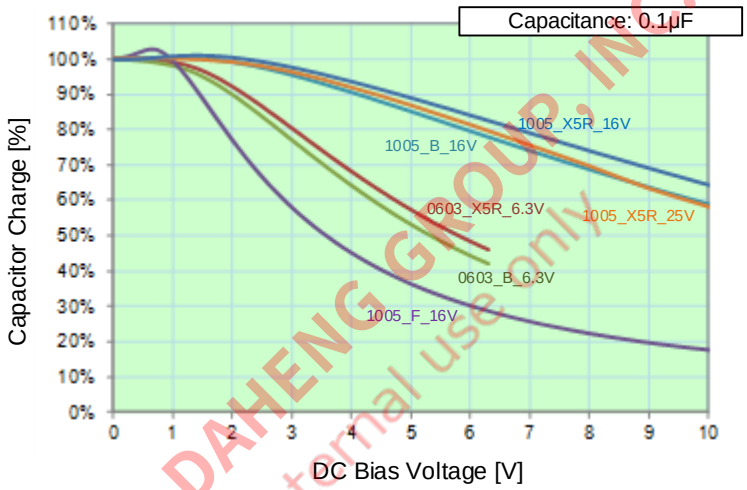
3.2.2. Decoupling capacitors

Please use non-polar capacitors. It is possible to operate the sensor by using typical ceramic capacitors.

(1). All the power supply voltage are smaller than 3.3 V so you can use any 1608M size capacitors of any characteristics in the graph. When you use 1005M size capacitors, you should select characteristics-B device. Characteristics-F device should not be chosen.

(2). Decoupling capacitors for each pin are sensitive to image quality. Please implement sufficient capacity of the decoupling capacitors according to the power supply condition. If you use capacity that is small one and large one, please put the small one near the sensor. Please refer to Application circuit for details.

(3). The capacity of the laminated layer ceramic capacitors will decrease in regard to the impressed DC bias voltage by piezo-electric effect. It will be more obvious when using smaller size and larger capacity, please check the specification sheet of each devices. (Graph below shows the characteristics.)



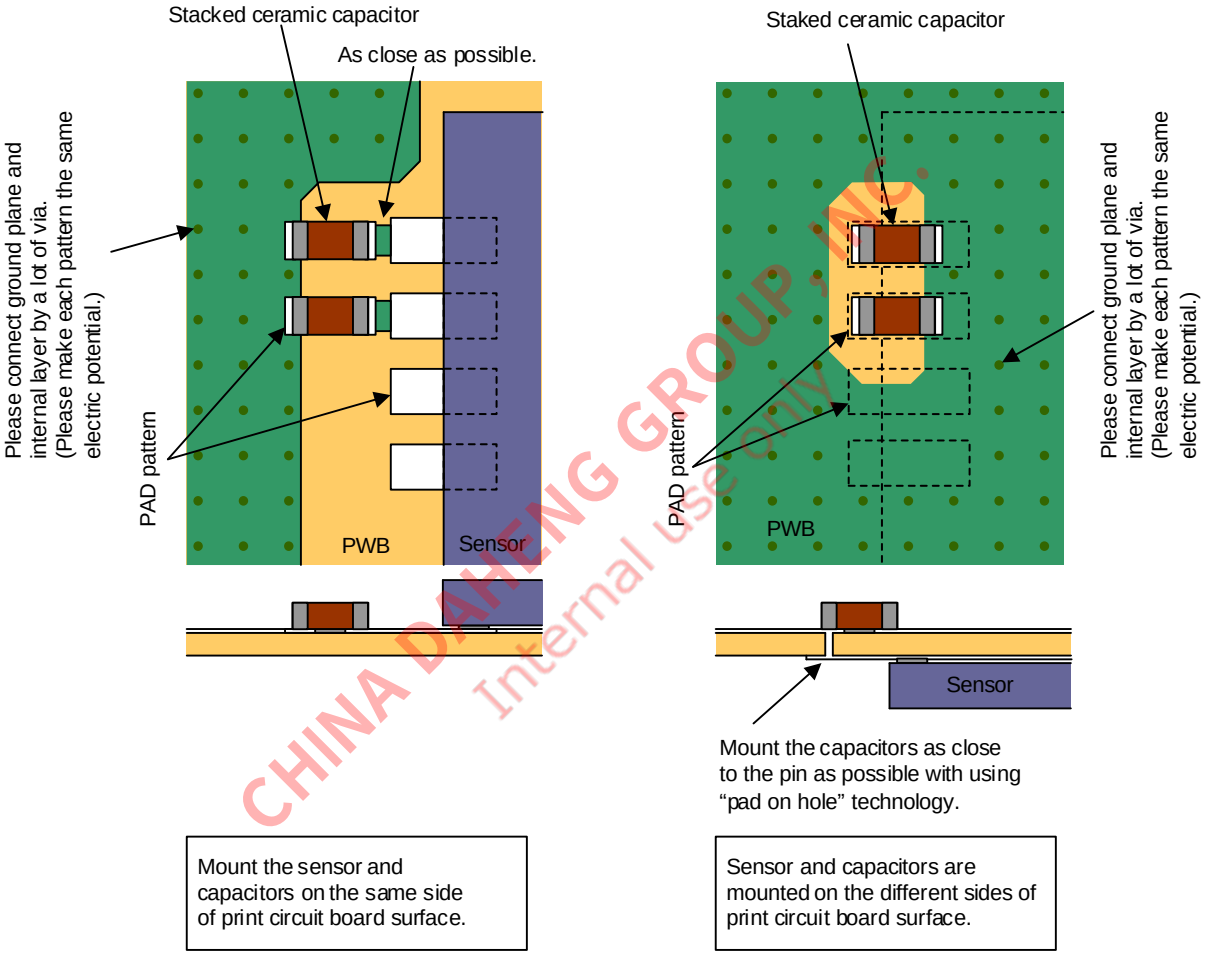
DC bias vs. capacity

3.3. Notes for designing patterns of printed circuit board.

3.3.1. Power supply pins

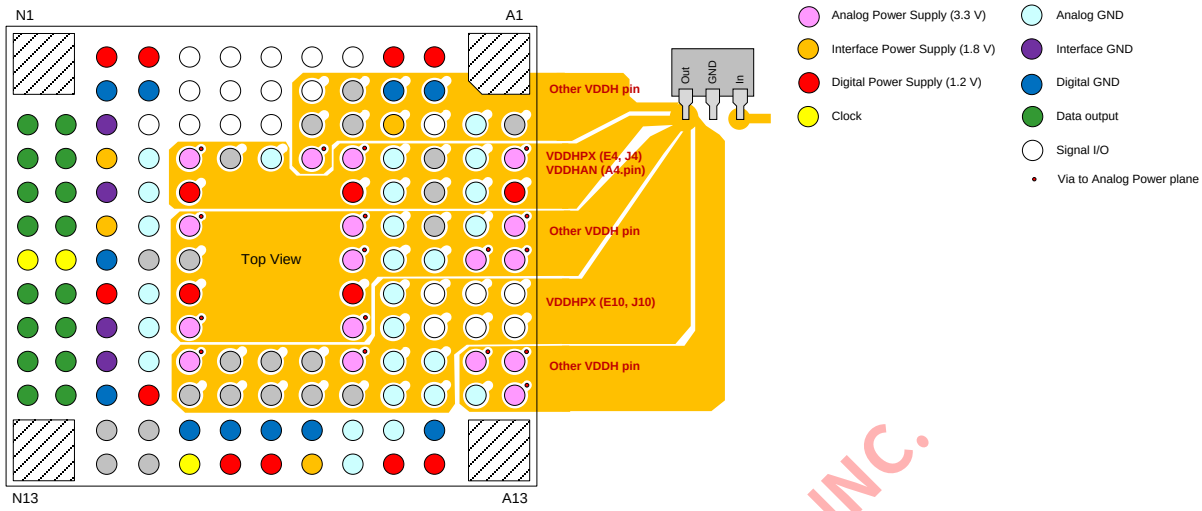
(1). The peripheral devices (capacitors) of the sensor should be mounted as close to the power supply pins as possible. Longer wire length might cause the degradation of the image quality.

(2). Surface power/ground plane and inner layer power/ground plane should be connected with enough number of the vias (Vertical Interconnect Access) . Please make each pattern the same electric potential.



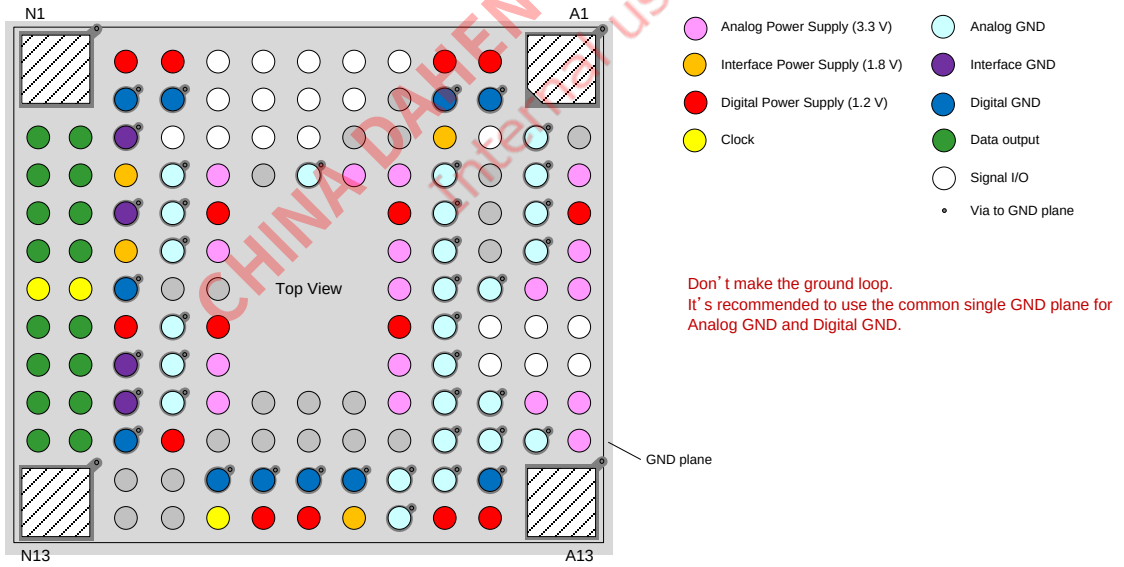
Example of capacitor mounting

(3). The noise on the E4 / E10 / J4 / J10.pin (VDDHPX), and A4.pin (VDDHAN) degrades the image quality. So VDDHPX and VDDHAN should not have the common impedance. Following drawing is the example of the layout of the power supply patterns.



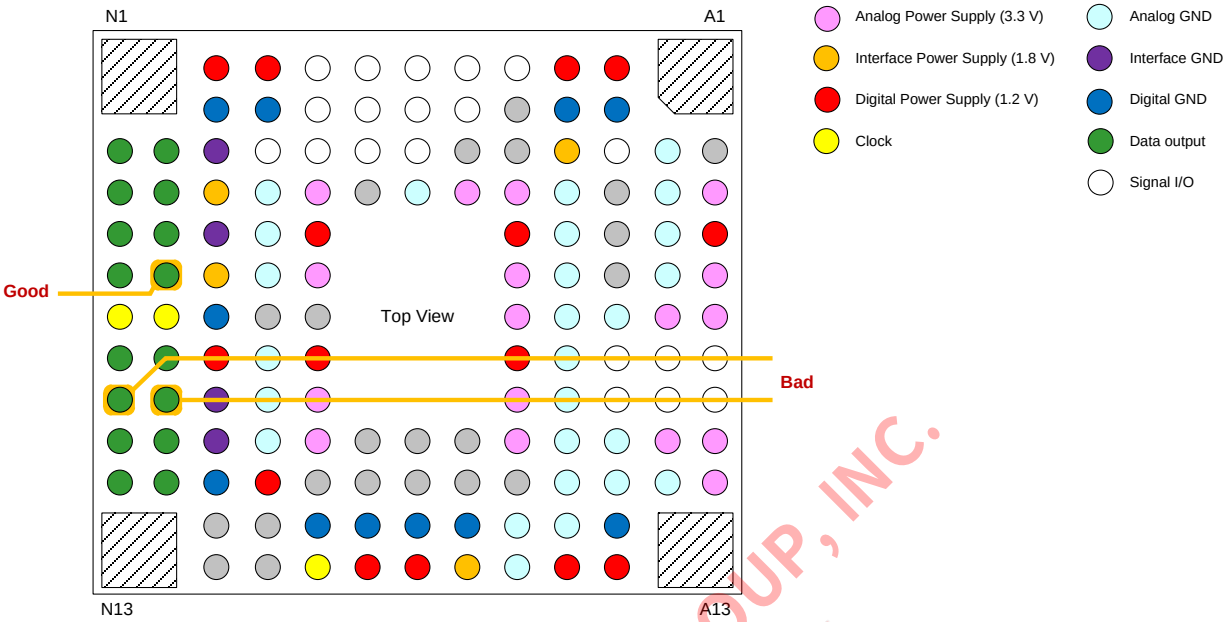
An example of E4 / E10 / J4 / J10 and A4.pin wiring patterns. (With 3-terminal regulator)

(4). Loop of the ground pattern might propagate the noise to the other patterns (ex. Power supply pattern) so the ground pattern recommends Land pattern. Its recommended to use the common single GND plane for Analog GND and Digital GND.



GND pattern

Other notes
Digital signal pattern on the other layer should not be in parallel with the power supply patterns, terminals of VCP1, VCP2, VRLSEL, VRLTRX, VRLOFG, VRLTRG, VRLGND, VRLRST, VBGR and these lines.

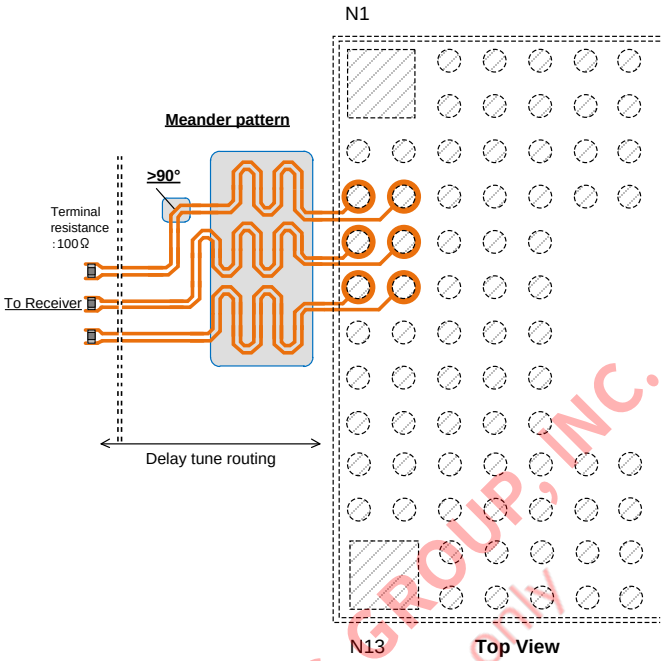


Signal Wire Routing

3.3.2. Wiring patterns for image output signals (Low-voltage LVDS serial output)

(1). When choosing low-voltage LVDS output mode, signal wires (DLOPx1 and DLOMx1, DLCKP1 and DLCKM1) must be paired.

(2). Meander pattern should make pattern as close to the output pins (near the sensor) as possible.

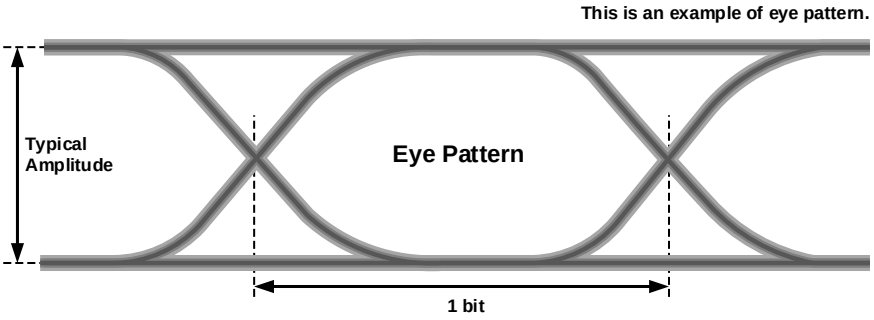


Example of wiring patterns for LVDS serial output signal

(3). We recommend delay tune wiring for image signals, especially delay of each differential pair signal and Data and its Strobe signal should be controlled by using meander wiring. Turning point angle of the wire should be greater or equal to 90 degree. (obtuse angle)

(4). Decoupling capacitors for power supply for image signal output (VDDM) should be mounted close to the power supply pins of the package of the sensor with using small size (1005M or 0603M) laminated layer ceramic capacitor.

<For your reference>
Validity of the image signal can be checked by “eye pattern” of the signals. With the adequate loading and delay tuned condition, you can see clear “eye pattern” with sufficient margin of the threshold and the noise level for the receiver.



Eye pattern of the image signal

4. 4-wire Serial Communication Port

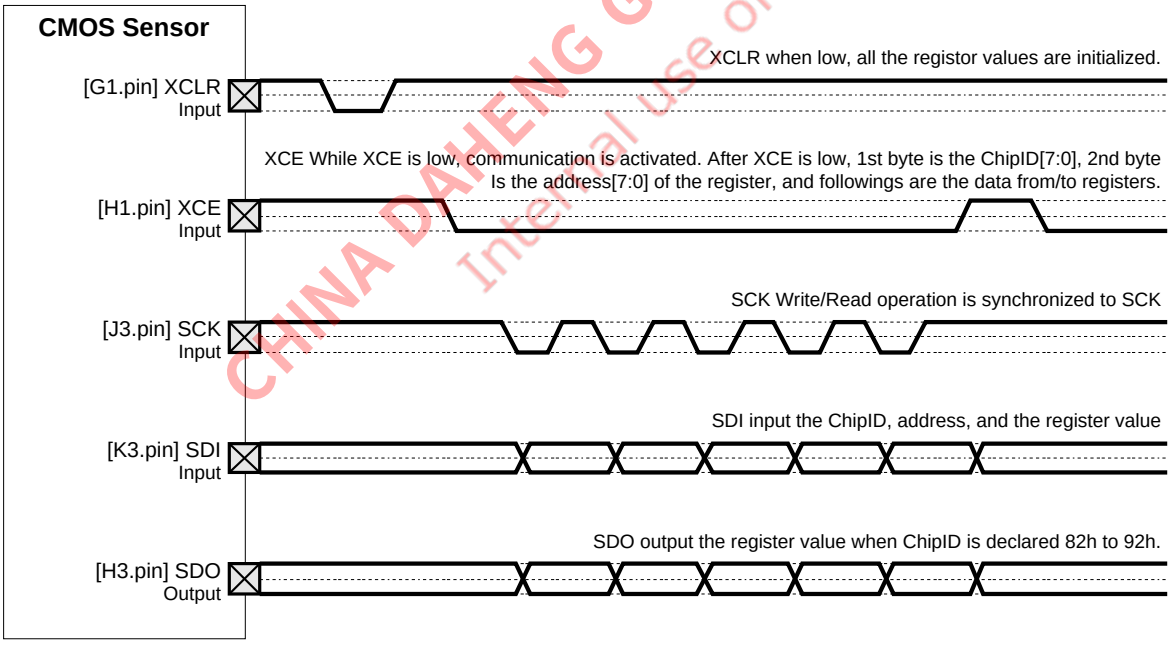
This section describes the operation of 4-wire serial interface.

4.1. Overview

Characteristics of 4-wire serial interface.

(1). 3-wire serial interface consists of serial data input (SDI), serial clock (SCK), and chip enable (XCE). SDO is the data output port for read out the value in the registers.
(2). Data transfer is done in unit of 8bit (1byte). In case of continuous communication, no limitation for the numbers of byte for the communications. (However, limited by communication period.)
(3). LSB first protocol.
Ex.) When sending 8'h28 LSB first transfer is 0001 0100.

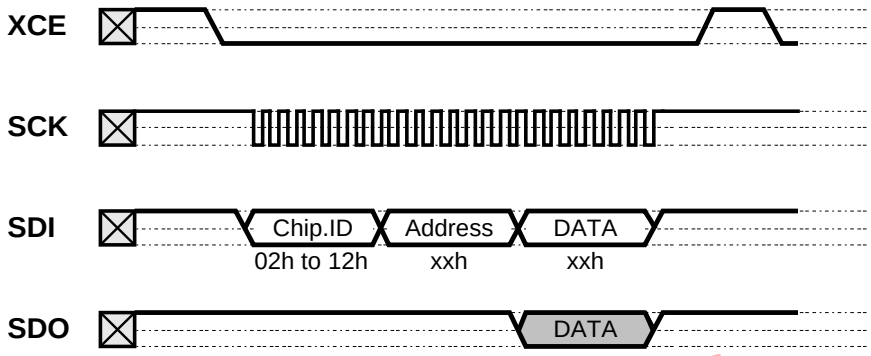
Terminal name	function	description
XCLR	Initialize the system	Initialize the register value.
XCE	Enable the communication	Communication is active for XCE is low.
SCK	Serial clock for communication	Maximum frequency is 13.5 MHz
SDI	Serial data input	Change the value at falling edge of SCK, latch the value by rising edge
SDO	Serial data output	Output the value synchronous to the falling edge of SCK



4-wire Communication Function

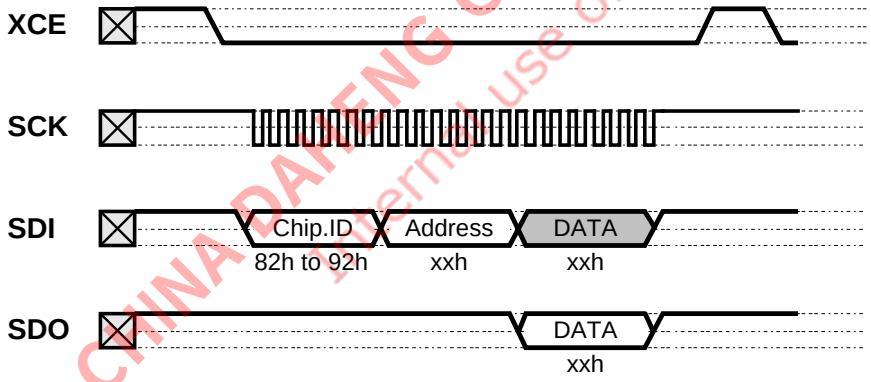
4.2. Register write/read operation

Both of register write and read operation, ChipID, address and register value are declared to SDI. When ChipID is 02h to 12h, value is written to the register designated by the address. When ChipID is 82h to 92h, the value is read out from the register designated by the address. Write and read operation can be done continuously while XCE is low.



Write Operation

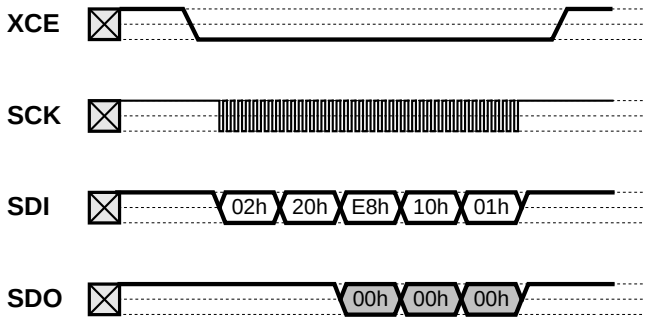
When write operation, the order of the commands to SDI is as follows. 1st byte: ChipID is selected among from 02h to 12h, 2nd byte: address to write, 3rd byte and after: register value. SDO output the current value (Before write) of the register designated by the address.



Read Operation

When read operation, the order of the commands to SDI is as follow. 1st byte: ChipID is selected among from 82h to 92h, 2nd byte: address to read, 3rd byte and after : invalid data SDO output the value of the register designated by the address.

The example of communication timing to writing to continuous address as shown table 1 is shown below.

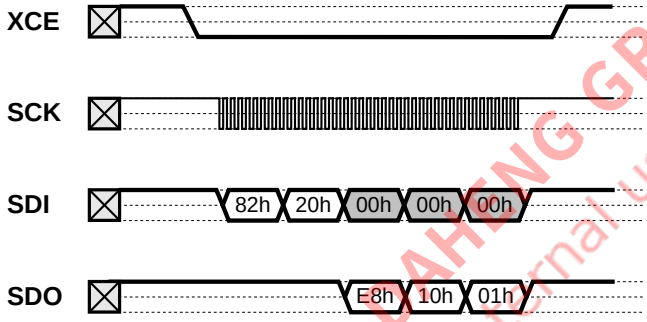


Write operation to continuous address

Table1. The example of writing registers

Address	bit	Default value	Setting value	
			before	After
20h	[7:0]	00h	00h	E8h
21h	[7:0]	00h	00h	10h
22h	[7:0]	00h	00h	01h

Write E8h to address 20h first. And with keeping XCE low, by writing 10h, 01h in succession, these values are set to consecutive addresses (21h and 22h). The example of reading communication timing to writing to continuous address as shown table 1 as shown table 2 is shown below.



Read operation to continuous address

Table2. The example of reading registers

Address	bit	Default value	Setting value	
			before	After
20h	[7:0]	00h	E8h	E8h
21h	[7:0]	00h	10h	10h
22h	[7:0]	00h	01h	01h

In case of reading out the value from the registers, write 82h to 92h as the ChipID then designate the address to read. After that input the dummy data to SDI. In read mode, input data are discarded and no register is updated, current register values are output from SDO continuously.

5. I²C interface communication port

This section describes the operation of I²C interface.

5.1. Overview

I²C Communication mode.

Mode	Data rate	Correspondant
Standard mode	100 kbps	○
Fast mode	400 kbps	○
High speed mode	3.4 Mbps	×

Slave address

Slave address	Slave Address [7:1]	MSB							LSB
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
SLAMODE = 0	36h	0	1	1	0	1	1	0	R/W
SLAMODE = 1	37h	0	1	1	0	1	1	1	R/W
SLAMODE = 0 / 1	1Ah	0	0	1	1	0	1	0	R/W

Characteristics of I²C communication

- I²C consists of 2 wires of serial data and serial clock.
- Unit of the communication is 8 bit (1 byte), bi-directional communication.

And in case of continuous communication, no limitation for the numbers of byte for the communications.(However, limited by communication period.)

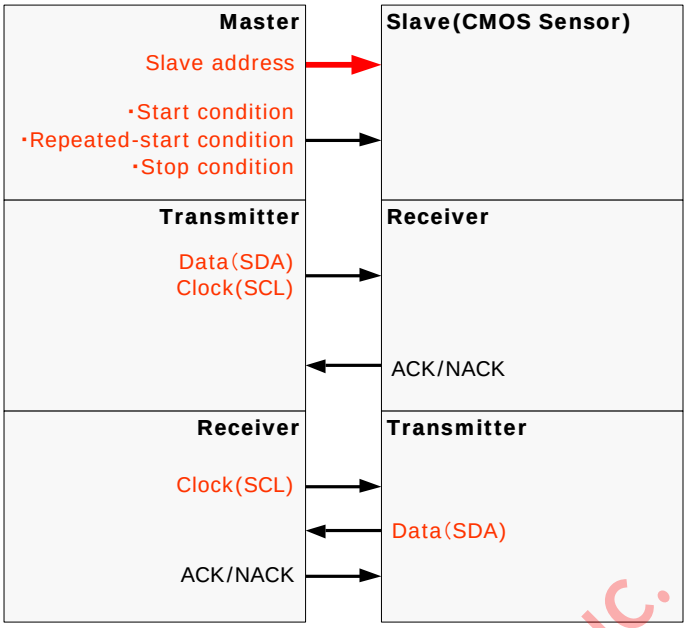
- Acknowledge bit (ACK/NACK) is required at the end of communication.
- MSB first protocol

Ex.) When sending 28h MSB first : 0010 1000.

- I²C is the bi-directional communication and the “master” side controls the communication, the “slave” side is controlled by master.
- IC is the bi-directional communication and the “master” side controls the communication, the “slave” side is controlled by master. The “master” always provides the for the data.

-While communication, the device transferring the data is the transmitter, and the device receiving the data is the receiver. The “slave” provides acknowledge bit.

- The sensor will be the slave.



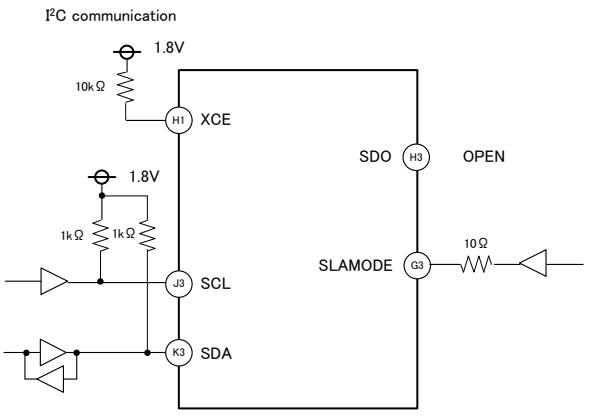
Relation between the sensor and the ISP when I^2C communication.

Master execute the following communication.

- Generate slave address (declare the device to be slave. Sensor is the slave here.)
- Generate “start condition”, “repeated start condition”, and “stop condition”.

While communication, the device transforming the data is the transmitter, and the device receiving the data is the receiver. Master can work as both transmitter and receiver, slave also work as both. Transmitter generates the data (SDA) and the clock (SCL), receiver generates the acknowledge Bit (ACK/NACK) and master always generates the clock (SCL) for acknowledge bit.

Reference design for I^2C serial communication is shown below. Please connect XCE and OV_{DD} when I^2C communication. In addition, SCL, SDA, please pull up to 1 kΩ OV_{DD}.



Reference design for I^2C serial communication

5.2. Overview of the communication protocol

Data is transferred by SDA port. The transition timing of the SDA follows the rule below.

- State control (start, restart, stop of the communication) is done while SCL is “high”.
- When data transfer, SDA toggles while SCL is “low”

5.2.1. State control (start, restart, stop of the communication)

The conditions of start (start condition), restart (repeated start condition), and stop (stop condition) of the communication is shown below. State control is done by master device.

State condition	condition
Start condition	SDA toggles from High to Low while SCL is high
Repeated start condition	start condition while stop condition is of the previous data transfer is not Declared
Stop condition	SDA toggles from Low to High while SCL is High.

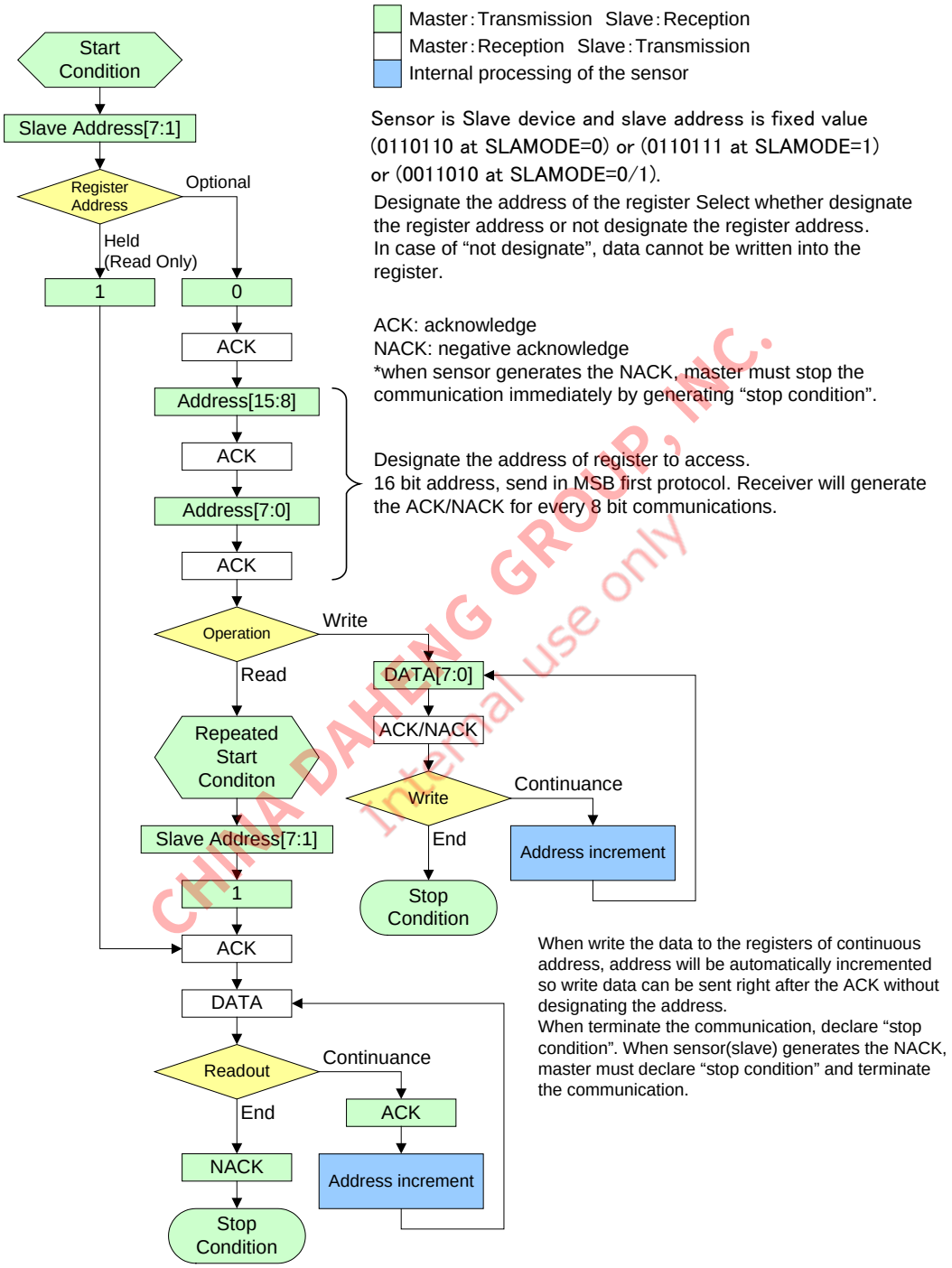
5.2.2. Acknowledge bit

Data transfer is done in unit of 8 bit (1 byte). The acknowledge bit is generated for every 8 bit data transfer and added after the last (8th) bit to indicate that receiver normally received the data. When receiver wants to stop the communication by the internal interrupt or etc. receiver generates the negative acknowledge bit (NACK).

- Master must send the slave address after declaration of the “Start condition” and “Repeated start condition”.
- When slave generators the negative acknowledge bit, master declares the stop condition and stops the communication immediately.

5.3. Write/read operation of the registers

Write/read operation of the registers are executed as shown below.



I^2C Register setting flow chart

6. Note for access to register

When writing the value to registers, we recommend “Read-modify-write” to avoid the trouble caused by inadequate over write of the register. For example “VREVERSE” value is assigned to address of 0Eh [0] , “HREVERSE” value is assigned to address of 0Eh [1]. When update HREVERSE value after writing VREVERSE, VREVERSE value in address of 0Eh [0] should be kept. “Read-modify-write” can prevent the wrong overwrite of the value

Ex.) In case of writhing the value 1d to VREVERSE and HREVERSE

In case of “no Read-modify-write”

1) HREVERSE = 1d ⋯ set value 02h to address: 0Eh

Address: 0Eh

0	0	0	0	0	0	1	0

2) VREVERSE = 1d ⋯ set value 01h to address: 0Eh

01h

Address: 0Eh

0	0	0	0	0	0	0	1

HREVERSE=0d VREVERSE=1d

Writing the VREVERSE value 01h to address 0Eh without considering HREVERSE bit in 0Eh [1], HREVERSE will be changed.

In case of “Read-modify-write”

1) HREVERSE = 1d ⋯ set value 02h to address: 0Eh

Address: 0Eh

0	0	0	0	0	0	1	0

2) Read register value

0	0	0	0	0	0	1	0

Read out the current value and store the value in the memory area of MCU

3) VREVERSE = 1d ⋯ set value 01h to address: 0Eh

01h

Address: 0Eh

0	0	0	0	0	0	1	1

Bit operation “add” with the value stored in step 2)

03h

Address: 0Eh

0	0	0	0	0	0	1	1

HREVERSE=1d VREVERSE=1d

Write value after bit operation (No overwrite of VREVERSE value)

7. Pattern Generator

This chapter explains the pattern generator function.

7.1. Feature

The pattern generator provides the following patterns.

- ◆Multiple Pixels Pattern
- ◆Sequence Pattern 1
- ◆Sequence Pattern 2
- ◆Gradation Pattern
- ◆Horizontal 1 Row Pattern
- ◆Vertical 1 Column Pattern
- ◆Horizontal 1 Row and Vertical 1 Column Pattern
- ◆Stripe Pattern of the Arbitrary Value
- ◆Checks Pattern of the Arbitrary Value
- ◆Color Bar which Changes Horizontally
- ◆Color Bar which Changes Vertically

7.2. Register map for pattern generator function

The Register map for Pattern Generator is shown below.
Please set via sensor standby.
Please refer to the datasheet for registers setup other than those lists.

Chip ID = 02 (Write: Chip ID = 02h, Read: Chip ID = 82h, I²C: 30**h)

Address	bit	Register Name	Description	Default value after reset		Reflection timing
				By register	By address	
22h	[7:0]		Fixed to F0h	01h	01h	S

Chip ID = 04 (Write: Chip ID = 04h, Read: Chip ID = 84h, I²C: 32**h)

Address	bit	Register Name	Description	Default value after reset		Reflection timing
				By register	By address	
38h	0	PGREGEN [0]	PG operation enabled 0h : PG OFF 1h : PG ON	0	06h	S
	1	PGTHRU [0]	Back Ground Transient 0h : Invalid PGMODE=00h / 06h; The background is fixed to "0h". PGMODE=04h / 05h; The background is set to PGDATA2. 1h : Valid	1		S
	2	PGCLKEN [0]	Clock control for PG 0h : Clock stop 1h : Clock operation Set to “1h” when using Pattern Generator	1		S
	3 4 5 6 7	PGMODE [4:0]	PG mode setting 00h: Multiple pixels Pattern 01h: Sequence Pattern 1 02h: Sequence Pattern 2 03h: Gradation Pattern 04h: Horizontal 1 Row Pattern 05h: Vertical 1 Column Pattern 06h: Horizontal 1 Row and Vertical 1 Column Pattern 07h: Stripe Pattern of the arbitrary value 08h: Checks pattern of the arbitrary value 0Ah: Color bar which changes horizontally 0Bh: Color bar which changes vertically Others: Setting prohibited	00h		S

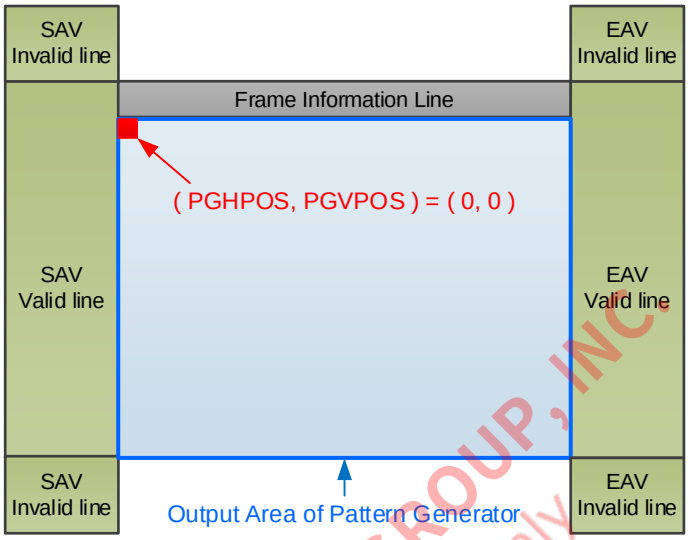
Address	bit	Register Name	Description	Default value after reset		Reflection timing
				By register	By address	
39h	0	PGHPOS [12:0]	LSB	0000h	00h	S
	1					
	2					
	3					
	4					
	5					
	6		Horizontal Start Address 0 or more is valid.			
	7					
3Ah	0				00h	
	1					
	2					
	3					
	4		MSB			
	5		Fixed to 0	0		-
	6		Fixed to 0	0		-
	7		Fixed to 0	0		-
3Ch	0	PGVPOS [11:0]	LSB	000h	00h	S
	1					
	2					
	3					
	4					
	5					
	6		Vertical Start Address 0 or more is valid.			
	7					
3Dh	0				00h	
	1					
	2					
	3		MSB			
	4		Fixed to 0	0		-
	5		Fixed to 0	0		-
	6		Fixed to 0	0		-
	7		Fixed to 0	0		-
3Eh	0	PGHPSTEP [7:0]	Interval of horizontal pixels 00h is prohibited	00h	00h	S
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3Fh	0	PGVPSTEP [7:0]	Interval of vertical pixels 00h is prohibited	00h	00h	S
	1					
	2					
	3					
	4					
	5					
	6					
	7					

Address	bit	Register Name	Description	Default value after reset		Reflection timing
				By register	By address	
40h	0	PGHPNUM [7:0]	Number of horizontal pixels 00h is prohibited	01h	01h	S
	1					
	2					
	3					
	4					
	5					
	6					
	7					
41h	0	PGVPNUM [7:0]	Number of vertical pixels 00h is prohibited	01h	01h	S
	1					
	2					
	3					
	4					
	5					
	6					
	7					
44h	0	PGDATA1 [12:0]	LSB	0000h	00h	S
	1					
	2					
	3					
	4					
	5					
	6		Set PGDATA1			
	7					
45h	0				00h	
	1					
	2					
	3					
	4		MSB			
	5		Fixed to 0	0		-
	6		Fixed to 0	0		-
	7		Fixed to 0	0		-
46h	0	PGDATA2 [12:0]	LSB	0000h	00h	S
	1					
	2					
	3					
	4					
	5					
	6		Set PGDATA2			
	7					
47h	0				00h	
	1					
	2					
	3					
	4		MSB			
	5		Fixed to 0	0		-
	6		Fixed to 0	0		-
	7		Fixed to 0	0		-

Address	bit	Register Name	Description	Default value after reset		Reflection timing
				By register	By address	
48h	[7:0]	COLORWIDTH [7:0]	Color bar width setting 16 pixels unit 00h and 01h are prohibited	0Bh	0Bh	S
49h	0		Fixed to 0	0	0Ah	-
	1		Fixed to 1	1		-
	2		Fixed to 0	0		-
	3		Fixed to 1	1		-
	4		Fixed to 0	0		-
	5		Fixed to 0	0		-
	6	PGHGSTEP [1:0]	The increment of gradation pattern 00b; +1 / 01b: +2 / 10b: +4 / 11b: prohibited	0h		S
	7					
4Ah to 53h	[7:0] to [7:0]		Do not rewrite	-	-	-
54h	0	BLKLEVEL [11:0]	LSB Black level offset value setting Set to “000h” when using Pattern Generator	03Ch	3Ch	S
	1					
	2					
	3					
	4					
	5					
	6					
	7					
55h	0				00h	
	1					
	2					
	3		MSB			
	4		Fixed to 0	0		-
	5		Fixed to 0	0		-
	6		Fixed to 0	0		-
	7		Fixed to 0	0		-

7.3. Common setting item for the PG

The output area of the PG pattern is the effective area of each mode. (The area shown in the blue of the following figure is output area.) In a pattern (0, 4, 5, 6) that specifies the location, the origin of horizontal is the next pixel of SAV4th and the origin of vertical is the next line of frame information line. By the register PGTHRU, the background can be selected to "Fixed 0h (Pattern 0, 6)" and "Setting PGDATA2 (pattern 4, 5)" and "Through" (imaging data). The figure below shows the details.



PG settings

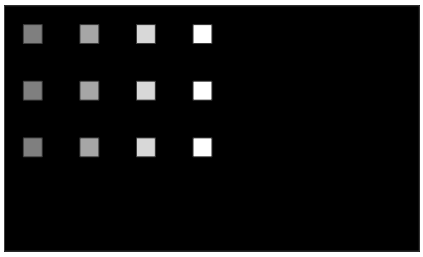
The output range for each output resolution is limited with the value of the following table.

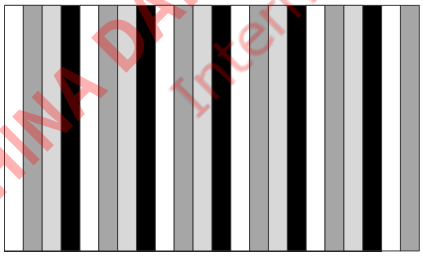
The range of the signal output

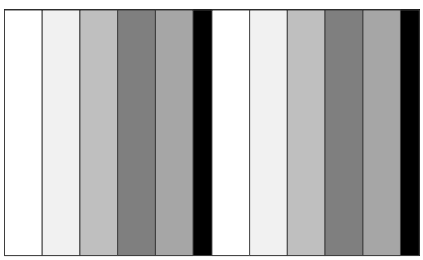
Resolution	Output value	
	Min.	Max.
8bit	01h	FEh
10bit	001h	3FEh
12bit	001h	FFEh

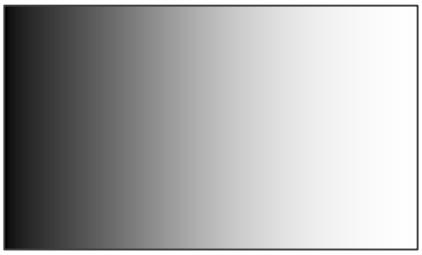
7.4. List of Pattern

The pattern which it outputs by this function is shown below.

0. Multiple pixels Pattern		
Register	Pattern	Notes
PGMODE = 00h PGDATA1 PGDATA2 PGHPOS PGVPOS PGHPSTEP PGVPSTEP PGHPNUM PGVPNUM		Generate multiple pixels pattern. PGDATA1: Data pattern at the location specified by PGVPOS and PGHPOS The output level of the next point to the right is PGDATA1 + PGDATA2. Since (every each vertical line) The output level is increasing at PGDATA1 + PGDATA2 × n (n=2, 3, 4…). It clips with the MAX value and returns to the startup level. PGVPOS: Specify the vertical start address PGHPOS: Specify the horizontal start address PGHPSTEP: Interval of horizontal pixels (0h is prohibited) PGVPSTEP: Interval of vertical pixels (0h is prohibited) PGHPNUM: Number of horizontal pixels (0h is prohibited) PGVPNUM: Number of vertical pixels (0h is prohibited)

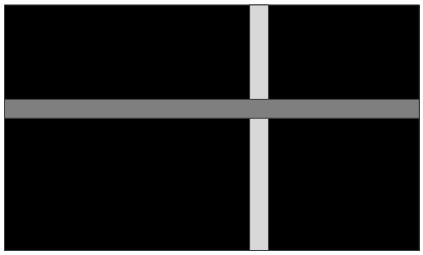
1. Sequence Pattern 1		
Register	Pattern	Notes
PGMODE = 01h		Outputs the sequential pattern of 1 pixel width 12bit: FFEh/555h/AAAh/001h 10bit: 3FEh/155h/2AAh/001h 8bit: FEh/55h/AAh/01h

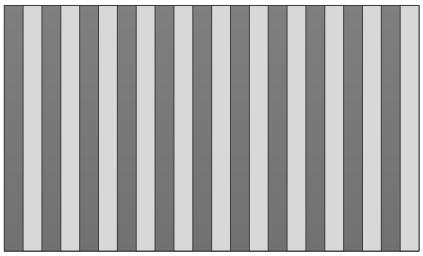
2. Sequence Pattern 2		
Register	Pattern	Notes
PGMODE = 02h		Outputs the following sequential pattern 12bit: FFEh/FFEh/FC0h/FC0h/C3Ch /C3Ch/ 333h/333h/AAAh/AAAh/001h/FFEh 10bit: 3FEh/3FEh/3F0h/3F0h/30Fh/30Fh/ 0CCh/0CCh/2AAh/2AAh/001h/3Feh 8bit: FEh/FEh/FCh/FCh/C3h/C3h/ 33h/33h/AAh/AAh/01h/FEh

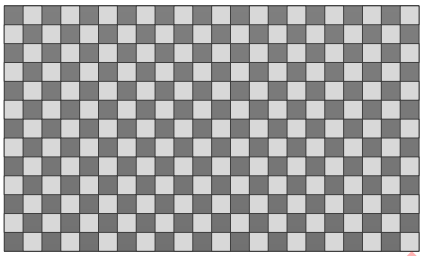
3. Gradation Pattern		
Register	Pattern	Notes
PGMODE = 03h PGHGSTEP		Outputs the following gradation pattern Minimun* to Maximun It reaches the max and increases from 000h* again. * : Output value is set to 001 h. PGHGSTEP : increment 00b; +1 / 01b: +2 / 10b: +4 / 11b: prohibited

4. Horizontal 1 Row Pattern		
Register	Pattern	Notes
PGMODE = 04h PGDATA1 PGVPOS		Outputs 1 row pattern with 1 pixel width at registered address. (Valid in the effective pixel region) PGDATA1: Specify the output value PGVPOS: Specify the vertical address

5. Vertical 1 Column Pattern		
Register	Pattern	Notes
PGMODE = 05h PGDATA1 PGHPOS		Outputs 1 column pattern with 1 pixel width at registered address. (Valid in the effective pixel region) PGDATA1: Specify the output value PGHPOS: Specify the horizontal address

6. Horizontal 1 Row and Vertical 1 Column Pattern		
Register	Pattern	Notes
PGMODE = 06h PGDATA1 PGDATA2 PGHPOS PGVPOS		Outputs 1column/row pattern with 1 pixel width at registered address. (Valid in the effective pixel region) PGDATA1: Specify the output value of the column. PGDATA2: Specify the output value of the row. PGHPOS: Specify the horizontal address for column. PGVPOS: Specify the vertical address for row.

7. Stripe Pattern of the arbitrary value		
Register	Pattern	Notes
PGMODE = 07h PGDATA1 PGDATA2		Outputs the vertical stripe pattern of the arbitrary value by 1-pixel width. PGDATA1: Specify the output value PGDATA2: Specify the output value

8. Checks pattern of the arbitrary value		
Register	Pattern	Notes
PGMODE = 08h PGDATA1 PGDATA2		Outputs the checkered pattern of the one pixel spacing with the arbitrary value. PGDATA1: Specify the output value PGDATA2: Specify the output value

10. Color bar which changes horizontally		
Register	Pattern	Notes
PGMODE = 0Ah COLORWIDTH		Outputs the color bar which changes horizontally. COLORWIDTH: Color bar width setting * 00h and 01h are prohibited COLORWIDTH ×16 pixel unit

11. Color bar which changes vertically		
Register	Pattern	Notes
PGMODE = 0Bh COLORWIDTH		Outputs the color bar which changes vertically. COLORWIDTH: Color bar width setting * 00h and 01h are prohibited COLORWIDTH ×16 pixel unit

8. How to get sensor information

Following sensors can be confirmed the sensor information of Type name and monochrome (LL) / color (LQ) by reading the values of the register as shown below.

8.1. Register map for sensor information

The Register map for sensor information is shown below.
Please refer to the datasheet for registers setup other than those lists.

Chip ID = 03 (Write: Chip ID = 03h, Read: Chip ID = 83h, I²C: 31h)**

Address	bit	Register Name	Description	Reflection timing
48h	6		Type name Information	Read only
	7			
49h	[6:0]			
	7		Monochrome / Color Information	

8.2. The description of reading data

8.2.1. Type name Information

Data	Type name
1 0 0 0 1 0 0 0 1	IMX273
1 0 0 0 1 1 1 1 1	IMX287

8.2.2. Monochrome / Color Information

Data	Monochrome / Color
0	Color (LQ)
1	Monochrome (LL)

9. Lens design guideline

This section describes the information to select the lens.

9.1. Optical system

9.1.1. IMX273 Optical dimension

◆Image size
Diagonal 6.3 mm (type 1/2.9)

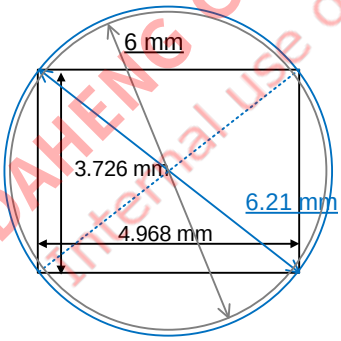
◆Number of recommended recording pixels
All pixel scan : 1440 (H) × 1080 (V) approx. 1.56 M pixels

◆Unit cell size
3.45 µm (H) × 3.45 µm (V)

◆Recommended lens F number
2.8 and larger (close side)

◆Recommended Exit Pupil Distance
- 100mm to -∞ (for B/W)

Image formation on IMX273 with the lens for type 1/3 is shown below.
4 corners are out of the image formation. It might be caused the mechanical vignetting.



All-pixel

Relation between Image Circle and the Pixel Area

9.1.2. IMX287 Optical dimension

◆Image size
Diagonal 6.3 mm (type 1/2.9)

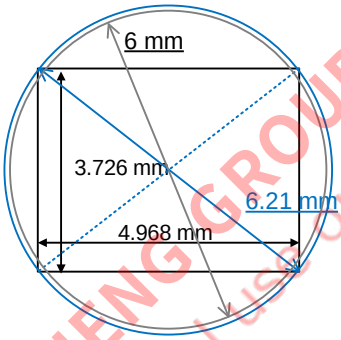
◆Number of recommended recording pixels
All pixel scan : 720 (H) × 540 (V) approx. 0.39 M pixels

◆Unit cell size
6.90 µm (H) × 6.90 µm (V)

◆Recommended lens F number
2.8 and larger (close side)

◆Recommended Exit Pupil Distance
- 100mm to -∞ (for B/W)

Image formation on IMX287 with the lens for type 1/3 is shown below.
4 corners are out of the image formation. It might be caused the mechanical vignetting.



All-pixel

Relation between Image Circle and the Pixel Area

9.1.3. CRA characteristics of recommended lens

The recommended CRA characteristics is 0.0 degrees all over the image height (0 – 100 %), because the target E.P.D. is infinite.
*We assume that the worst case of E.P.D. is -100mm. The CRA characteristics of -100mm E.P.D. are described below. The real CRA should be smaller than the table below.

CRA characteristics of IMX273, IMX287

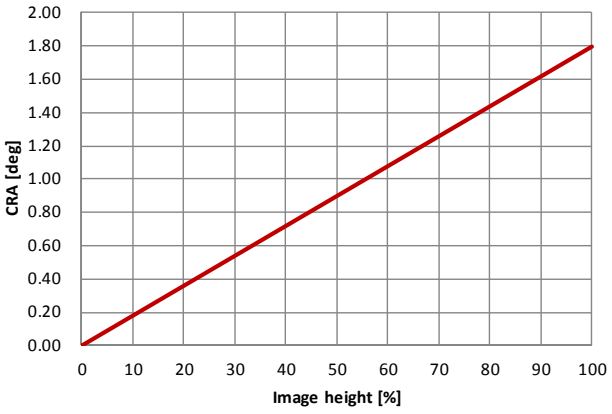
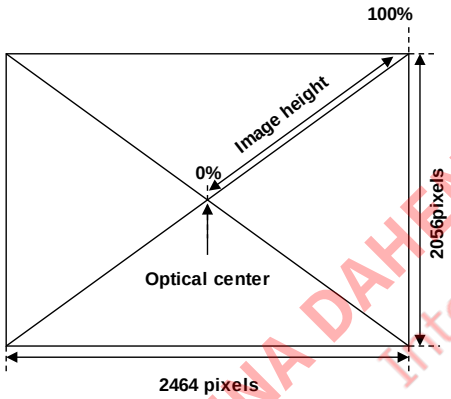


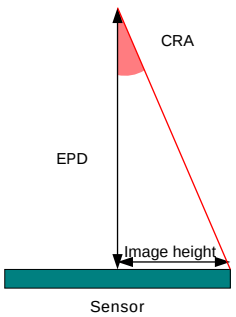
Image height		CRA
(%)	(mm)	(deg)
0	0.00	0.00
5	0.16	0.09
10	0.31	0.18
15	0.47	0.27
20	0.63	0.36
25	0.78	0.45
30	0.94	0.54
35	1.10	0.63
40	1.25	0.72
45	1.41	0.81
50	1.57	0.90
55	1.72	0.99
60	1.88	1.08
65	2.04	1.17
70	2.19	1.26
75	2.35	1.35
80	2.51	1.44
85	2.66	1.53
90	2.82	1.62
95	2.98	1.71
100	3.14	1.80



Example of IMX273

CRA characteristics

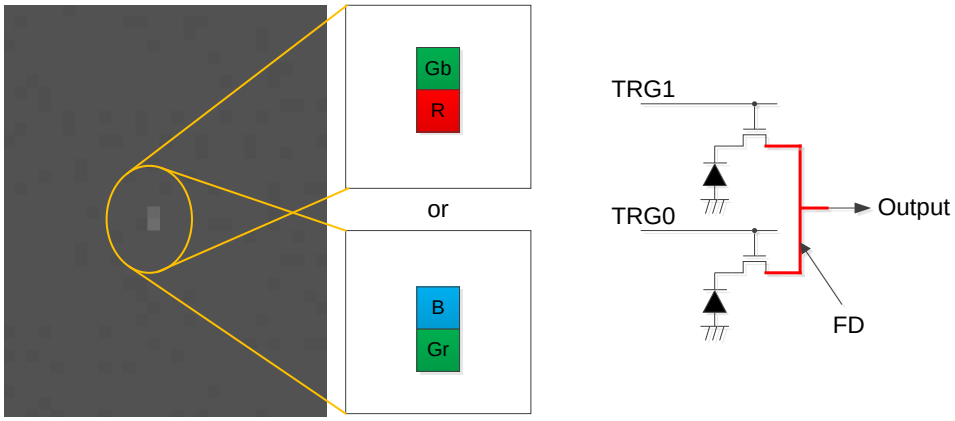
CRA (Chief Ray Angle) indicates the optimum angle of the chief ray for the image height, independent from the aperture size of the lens. This sensor assumes the recommended EPD (Recommended exit pupil distance) is farther than -100mm and the angle of chief ray is theoretically directional light (perpendicular for the imaging plane). CRA characteristics table shown above is calculated with assuming short exit pupil distance case, precisely -100mm.



CRA characteristics

10. FD white spots (IMX287 isn't applicably)

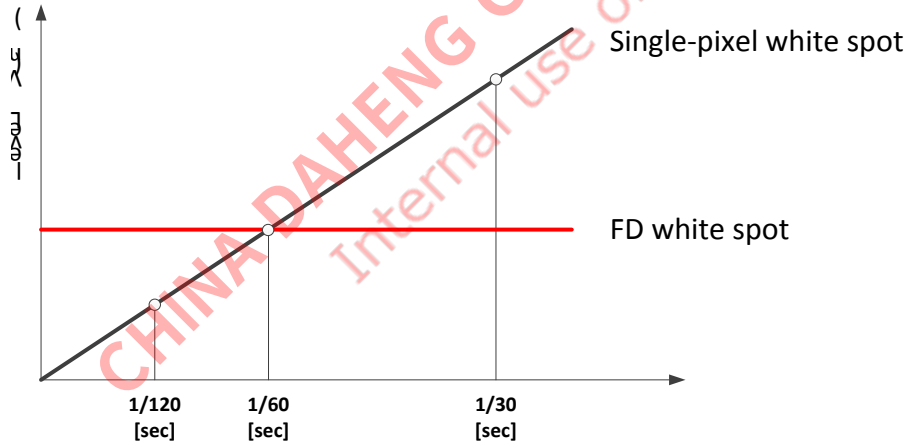
This sensor takes the common floating diffusion transistor (FD) architecture to widen the aperture ratio of the pixel. When FD has the leak current or other defect, white spot consist of 2 pixels (vertical 2 pixels) will appear.



FD White spot

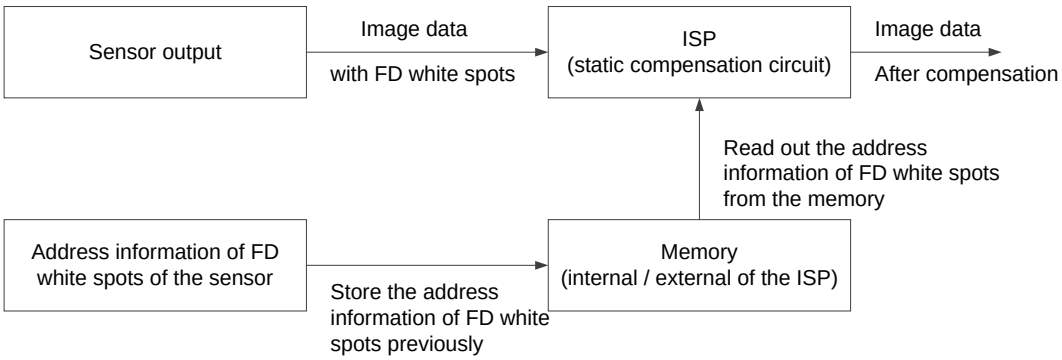
Overview of FD white spot

The signal level of single-pixel white spots (due to the defect of single pixel) increases according to the accumulation time. On the other hand, FD white spot is constant to the accumulation time. There exist the dependency to the temperature, but characteristics are various according to the cause of the spots.



Feature of FD white spot
(Both single-pixel white spots and FD white spots are same level at 60 frame/s)

FD white spot is different from single white pixel, cluster spots, then usual dynamic compensation might not be able to conceal it. Static compensation will be necessary. Please consider to use the static compensation of the ISP.



11. FAQ

11.1. In case the image cannot be displayed with the finished sensor board

Check Item	Description	Remark
Please confirm that the power supply design is according to the specification	- Please confirm that the applied power supply voltage level is within the recommended range (Analog Power 3.3 ±0.15V Interface Power: 1.8 ±0.1V , Digital power: 1.2 ±0.1V.) - Please confirm that the power supply capacity is enough for the total current consumption requirement of the board including the sensor - Please confirm that the direction of the sensor (the foot print of the board and the chip) is correct	Refer to the DC characteristics section of the specification
Please confirm that the register communication is done correctly	- Please confirm that the sensor has come out of the standby mode. Read register of address 00h and confirm that 00h has been written in the register. (See the specification or the register communication description of this document for the register read sequence) - Please double check the communication protocol if the register cannot be written correctly. - In case of 4-wire serial communication, the LSB first protocol should be followed for both register read and write. - In case of 4-wire serial communication, it is necessary to assign the ChipID and Address again after the XCE has been set high. - Please reset the sensor through the XCLR pin right after power-on - After power-on and exit of the standby mode, the default setting is 8ch output in All-pixel 10bit mode. Please make the register settings according to the desired operation mode.	Refer to P.13 of this document

11.2. In case there is noise observed in the output image

Noise Condition	Check Item	Remark
Vertical or horizontal stripes, always present	- Please confirm that the decoupling capacitor of the power supply has sufficient capacitance and is put close to the sensor pin. - Please also confirm that the decoupling capacitor of VCP1, VCP2, VBGR pin has sufficient capacitance as well.	Refer to P. 4 of this document
Horizontal stripes with random timing, not always present	- Please confirm that the register communication timing and the sensor data output timing are not overlapped. Conduct the register communication during the assigned period of the operation mode.	Regarding the communication timing, refer to the Operation mode section of the specification.
Posterization, bit loss	- Please confirm that the bit depth of the captured image data and that of the output image data are matched - It is possible that the data capture timing is critical. Please compare the output waveform of the DO pin against that of the DCK pin to confirm that there is no problem with the data capture timing.	Regarding the timing, refer to the AC characteristics section of the specification.

Revision History

Version	Date	Page	Remarks
Rev.0.1	31-Aug-16	---	First edition
Rev.1.0	10-Mar-17	16, 19	Correction: Each slave addresses of sensor of I^2C.
Rev.1.0	10-Mar-17	21	Delate: TBD of IMX287 supports of the pattern generator.
Rev.1.0	10-Mar-17	22	Correction: The write Chip ID. (Chip ID 04=> Chip ID 02)
Rev.1.0	10-Mar-17	28	Correction: The figure of 3. Gradation Pattern
Rev.1.0	10-Mar-17	30	Update: Description of "How to get sensor information".
Rev.1.0	10-Mar-17	36	Correction: The LVDS ch and the number of bits in table 11.1 of FAQ. (16ch => 8ch, 12bit => 10bit)
Rev.1.0	10-Mar-17	---	First edition (Official version)