SONY

IMX273 / IMX287 Application Note

Driving Low Power Consumption at longtime exposure

The data except this specification conform to those of IMX273 / IMX287.

Description

This document describes how to drive low power consumption at longtime exposure. This setting is effective to reduce the power consumption by stopping internal circuit during V-Blanking period in long exposure time.

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Register Map

The register map for driving low power consumption at longtime exposure is shown below.
Please refer to the product specification for register setup other than those list.

Registers corresponding to Chip ID = 02h in Write mode. (I2C:30**h)

Address	Bit	Register Name	Description	Default value after reset	Reflection timing
24h	0	SST_EN	Low power consumption enable 0: Disable, 1: Enable	0	S
	1		Fixed to “0”	0	-
	2		Fixed to “0”	0	-
	3		Fixed to “0”	0	-
	4		Fixed to “0”	0	-
	5		Fixed to “0”	0	-
	6		Fixed to “0”	0	-
	7		Fixed to “0”	0	-
9Ch	[7:0]		Set to “2Ch”	04h	S

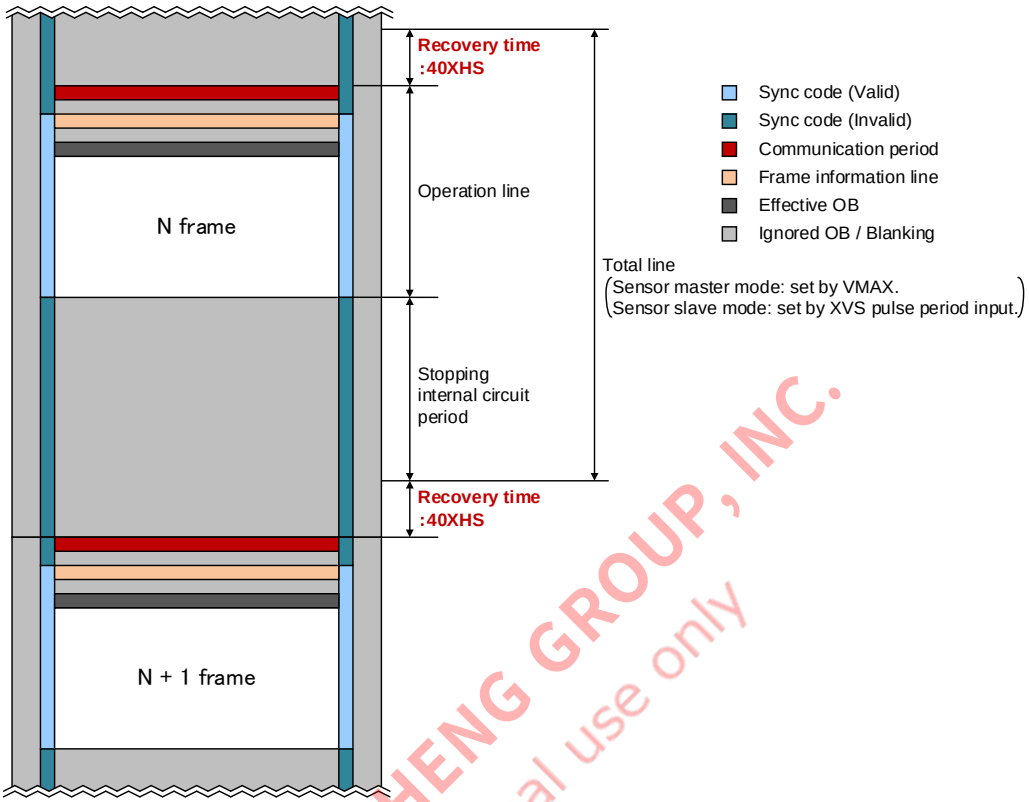
Registers corresponding to Chip ID = 12h in Write mode. (I2C:40**h)

Address	Bit	Register Name	Description	Default value after reset	Reflection timing
C9h	[7:0]	SST_SIESTA1_SET	Set to “FFh”	00h	S
CCh	0	SST_SIESTA1PRE_1U [11:0]	LSB	FFFh	S
	1				
	2				
	3				
	4				
	5				
	6				
	7				
CDh	0		Stopping internal circuit start line designated (Refer to “List of Settings” item.)		
	1				
	2				
	3		MSB		
	4		Fixed to “0”	0	-
	5		Fixed to “0”	0	-
	6		Fixed to “0”	0	-
	7		Fixed to “0”	0	-
CEh	0	SST_ SIESTA1PRE_1D [11:0]	LSB	FFFh	S
	1				
	2				
	3				
	4				
	5				
	6				
	7				
CFh	0		Stopping internal circuit end line designated (Refer to “List of Settings” item.)		
	1				
	2				
	3		MSB		
	4		Fixed to “0”	0	-
	5		Fixed to “0”	0	-
	6		Fixed to “0”	0	-
	7		Fixed to “0”	0	-
D0h	0	SST_SIESTA1PRE_2U [11:0]	LSB	FFFh	S
	1				
	2				
	3				
	4				
	5				
	6				
	7				
D1h	0		Stopping internal circuit start line designated (Refer to “List of Settings” item.)		
	1				
	2				
	3		MSB		
	4		Fixed to “0”	0	-
	5		Fixed to “0”	0	-
	6		Fixed to “0”	0	-
	7		Fixed to “0”	0	-

Address	Bit	Register Name	Description	Default value after reset	Reflection timing
D2h	0	SST_ SIESTA1PRE_2D [11:0]	LSB	FFFh	S
	1				
	2				
	3				
	4				
	5		Stopping internal circuit end line designated (Refer to “List of Settings” item.)		
	6				
	7				
D3h	0				
	1				
	2				
	3		MSB		
	4		Fixed to “0”	0	-
	5		Fixed to “0”	0	-
	6		Fixed to “0”	0	-
	7		Fixed to “0”	0	-

About Low Power Consumption Setting

This setting can be set to only vertical line that sensor is not operated, because this function set by stopping internal circuit. In addition, use this function when performing exposure of longer than certain period of time because 40lines for recovery time is necessary.



Low Power Consumption Setting Diagram

Setting of IMX273

List of Settings

Operation Mode	Operation Line [DEC]	SST_SIESTA1_SET setting [DEC]	SST_SIESTA1PRE_1U SST_SIESTA1PRE_2U setting [DEC]	SST_SIESTA1PRE_1D SST_SIESTA1PRE_2D setting [DEC]
All-Pixels	1130	255	1171	1
ROI	V_{TR} *1	255	V_{TR} + 41	1
ROI Overlap	V_{TR} *1	255	V_{TR} + 41	1
Vertical / Horizontal 1/2 Subsampling	586	255	627	1
Vertical 2-pixel FD Binning*2	586	255	627	1
2 × 2 Vertical FD Binning*2	586	255	627	1

Please set “44d” to register of Chip ID = 02h, Address = 9Ch. (all operation mode)

*1 V_{TR} ; Number of total lines designated in ROI. V_{TR} = ROIWV1 + ROIWV2 + 42.
*2 Vertical 2-pixel FD Binning and 2 × 2 Vertical FD Binning are able to set IMX273LLR only.

Setting of IMX287

List of Settings

Operation Mode	Operation Line [DEC]	SST_SIESTA1_SET setting [DEC]	SST_SIESTA1PRE_1U SST_SIESTA1PRE_2U setting [DEC]	SST_SIESTA1PRE_1D SST_SIESTA1PRE_2D setting [DEC]
All-Pixels	586	255	627	1
ROI	V_{TR} *1	255	V_{TR} + 41	1

Please set “44d” to register of Chip ID = 02h, Address = 9Ch. (all operation mode)

*1 V_{TR} ; Number of total lines designated in ROI. V_{TR} = ROIWV1 + 42.

Revision History

Version	Date	Page	Remarks
Rev.0.1	20 – Jan. – 17	–	First Edition
Rev.1.0	6 – Oct. – 17	–	First Edition (Official Version)