

IMX273 / IMX287 Application Note

Gradation Compression

The data except this specification conform to those of IMX273 / IMX287.

Description

The function of Gradation Compression which makes the output data be 8 bit is described in this document. When this function is used, the data is compressed and reduced.

Features

◆ Support the number of conversion bit

Conversion from 12 bit to 8 bit

Conversion from 10 bit to 8 bit

◆ Position of the compression

The 1 or 2 position can be set by the register.

◆ Compression gain setting

The compression gain can be set by the register.

◆ Supported mode

All-pixel scan mode

Vertical / Horizontal 1 / 2 Subsampling mode (IMX273LLR, IMX273LQR)

Vertical 2-pixel FD Binning mode (IMX273LLR)

2×2 Vertical FD Binning mode (IMX273LLR)

ROI mode

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^{*}This function is used by setting in range which the output of Gradation Compression doesn't saturate.

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Register Map

The register map for Gradation Compression is shown below. Please refer to the product specification for register setup other than those list.

Registers corresponding to Chip ID = 02h in Write mode. (I2C:30**h)

Address	Bit	Register name	Description	Default Value after reset	Reflection timing
16h	[1:0]	ODBIT	Fixed to "2h"	Oh	S
1011	0	CEBIT	Fixed to "1"	1	-
	1		Fixed to "0"	0	_
23h	2	CMPEN	Set Gradation Compression enable 0: Normal mode 1: Gradation Compression mode (according to CCMP1 / 2)	0	S
	3		Fixed to "0"	0	-
	4		Fixed to "0"	0	-
	5		Fixed to "0"	0	-
	6		Fixed to "0"	0	-
	7		Fixed to "0"	0	-
	0		Set the first start point of gradation compression (data position) 0000: Gradation compression off (both of the first and second)		
	1	CCMP1	0001: 000h 0010: 010h 0011: 020h	0h	S
	2	COMPT	0100: 040h 0101: 080h 0110: 100h 0111: 200h	UII	3
	3	OP	1000: 400h 1001: 800h Others: prohibited		
E8h	4	CHIMA	Set the second start point of gradation compression (data position) 0000: The second Gradation compression off 0001: prohibited		
	5	O'	0010: 0010h 0011: 0020h 0100: 0040h		
	6	CCMP2	0101: 0080h 0110: 0100h 0111: 0200h 1000: 0400h	0h	S
	7		1001: 0800h Others: prohibited *In case of setting more than 0010, to set CCMP2 < CCMP1 is prohibited.		

Address	Bit	Register name	Description	Default Value after reset	Reflection timing
	0		Set the gain of the first gradation compression 0000: 1 / 1 0001: 1 / 2		
	1		0010: 1 / 4 0011: 1 / 8 0100: 1 / 16 0101: 1 / 32		_
	2	ACMP1	0110: 1 / 64 0111: 1 / 128 1000: 1 / 256	0h	S
	3		1001: 1 / 512 1010: 1 / 1024 1011: 1 / 2048 Others: prohibited		
E9h	4		Set the gain of the second gradation compression 0000: 1 / 1 0001: 1 / 2		
	5		0010: 1 / 4		
	6	ACMP2	0101: 1 / 32 0110: 1 / 64 0111: 1 / 128 1000: 1 / 256	0h	S
	7		1001: 1 / 512		
		CHIMADA	Triternal		

Readout Drive Mode

IMX273 FREQ (CID = 02h, Address = 1Bh, [1:0]) = 0h

Drive	Frame	Data	**	A/D conversion		per of ng pixels		number xels ^{*2}		Number of INCK in 1H	
mode	rate [frame/s]	rate [Gbps]	Serial LVDS ch ^{*1}	(output gradation)	Н	V	Н	V	INCK: 37.125 MHz	INCK: 74.25 MHz	INCK: 54 MHz
	262.8	4.752	8				2000		125.0	250.0	181.8
	152.8	2.376	4	10 (8)			1720		215.0	430.0	312.7
Allminal	82.1	1.188	2	(0)	1440	1080	1600	1130	400.0	800.0	581.8
All pixel	165.9	4.752	8		1440	1080	3168	1130	198.0	396.0	288.0
	154.2	2.376	4	12 (8)			1704		213.0	426.0	309.8
	81.7	1.188	2	(0)			1608		402.0	804.0	584.7
	506.8	4.752	8				2000		125.0	250.0	181.8
All pixel	506.8	2.376	4	10 (8)			1000		125.0	250.0	181.8
(Vertical /	287.9	1.188	2	(0)	700	540	880	500	400.0	440.0	320.0
Horizontal 1/2	319.9	4.752	8		720	540	3168	586	198.0	396.0	288.0
subsampling)	319.9	2.376	4	12 (8)			1584		198.0	396.0	288.0
	293.3	1.188	2	(0)			864	1.	216.0	432.0	314.2
	506.8	4.752	8				2000		125.0	250.0	181.8
	294.6	2.376	4	10 (8)			1720		215.0	430.0	312.7
Vertical 2-pixel - FD Binning	158.3	1.188	2	(0)	4440	-60	1600	500	400.0	800.0	581.8
(IMX273LLR only)	319.9	4.752	8		1440	540	3168	586	198.0	396.0	288.0
Offig)	297.4	2.376	4	12 (8)			1704		213.0	426.0	309.8
	157.6	1.188	2	(0)) .	1608		402.0	804.0	584.7
	506.8	4.752	8				2000		125.0	250.0	181.8
2×2	506.8	2.376	4	10 (8)	O'	0)	1000		125.0	250.0	181.8
Vertical FD	287.9	1.188	2	(6)	700	2,540	880	500	220.0	440.0	320.0
Binning (IMX273LLR	319.9	4.752	8	70	720	5 40	3168	586	198.0	396.0	288.0
only)	319.9	2.376	4	12 (8)			1584		198.0	396.0	288.0
	293.3	1.188	2	(0)			864		216.0	432.0	314.2
	*4	4.752	8				2000		125.0	250.0	181.8
-	*4	2.376	4	10 (8)			1720		215.0	430.0	312.7
-	*4	1.188	2	(8)	*3	*3	1600	*4	400.0	800.0	581.8
ROI	*4	4.752	8		3	3	3168	,	198.0	396.0	288.0
	*4	2.376	4	12 (8)			1704		213.0	426.0	309.8
	*4	1.188	2	(0)			1608		402.0	804.0	584.7

The data rate of each output channel is value that is obtained by total data rate divided by the number of channels.

Example) In All-pixel 262.8 [frame/s] mode: 4.752 [Gbps] / 8 = 594 [Mbps]

For the setting value to register HMAX / VMAX, see the section of each drive mode settings

^{*3} Designated cropping area (ROI)

^{*4} See the section of "ROI mode"

SONY

IMX273 FREQ (CID = 02h, Address = 1Bh, [1:0]) = 1h

Drive	Frame	Data		A/D conversion	Numb recordin		Total n	umber kels ^{*2}		Number of INCK in 1H	
mode	rate [frame/s]	rate [Gbps]	Serial LVDS ch ^{*1}	(output gradation)	Н	V	Н	V	INCK: 37.125 MHz	INCK: 74.25 MHz	INCK: 54 MHz
	149.3	2.376	8				1760		220.0	440.0	320.0
	80.1	1.188	4	10 (8)			1640		410.0	820.0	596.4
All pivol	42.1	594	2	(0)	1440	1080	1560	1130	780.0	1560.0	1134.6
All pixel	150.0	2.376	8		1440	1000	1752	1130	219.0	438.0	318.6
	80.5	1.188	4	12 (8)			1632		408.0	816.0	593.5
	42.1	594	2	(0)			1560		780.0	1560.0	1134.6
	487.3	2.376	8				1040		130.0	260.0	189.1
All pixel	275.4	1.188	4	10 (8)			920		230.0	460.0	334.6
(Vertical / Horizontal	150.8	594	2	(0)	720	540	840	586	420.0	840.0	610.9
1/2	319.9	2.376	8		720	540	1584	300	198.0	396.0	288.0
subsampling)	285.3	1.188	4	12 (8)			888		222.0	444.0	322.9
	150.8	594	2	(-)			840		420.0	840.0	610.9
	*4	2.376	8				1760		220.0	440.0	320.0
	*4	1.188	4	10 (8)			1640		410.0	820.0	596.4
ROI	*4	594	2	(5)	*3	*3	1560	*4	780.0	1560.0	1134.6
KUI	*4	2.376	8				1752		219.0	438.0	318.6
	*4	1.188	4	12 (8)			1632		408.0	816.0	593.5
	*4	594	2	(5)		Q	1560		780.0	1560.0	1134.6

The data rate of each output channel is value that is obtained by total data rate divided by the number of channels.

ne section Example) In All-pixel 149.3 [frame/s] mode: 2.376 [Gbps] / 8 = 297 [Mbps]

For the setting value to register HMAX / VMAX, see the section of each drive mode settings

Designated cropping area (ROI)

See the section of "ROI mode"

SONY

IMX287 FREQ (CID = 02h, Address = 1Bh, [1:0]) = 0h

Drive	Frame	Data		A/D conversion	Numb recordin	per of ng pixels		number xels ^{*2}		Number of INCK in 1H	
mode	rate [frame/s]	rate [Gbps]	Serial LVDS ch*1	(output gradation)	Н	V	н	V	INCK: 37.125 MHz	INCK: 74.25 MHz	INCK: 54 MHz
	506.8	4.752	8				2000		125.0	250.0	181.8
	506.8	2.376	4	10 (8)			1000		125.0	250.0	181.8
All pixel	287.9	1.188	2	(0)	720	540	880	586	220.0	440.0	320.0
All pixel	319.9	4.752	8		720	540	3168	300	198.0	396.0	288.0
	319.9	2.376	4	12 (8)			1584		198.0	396.0	288.0
	293.3	1.188	2	(0)			864		216.0	432.0	314.2
	*4	4.752	8				2000		125.0	250.0	181.8
	*4	2.376	4	10 (8)			1000		125.0	250.0	181.8
ROI	*4	1.188	2	(0)	*3	*3	880	*4	220.0	440.0	320.0
KUI	*4	4.752	8				3168		198.0	396.0	288.0
	*4	2.376	4	12 (8)			1584		198.0	396.0	288.0
	*4	1.188	2	(3)			864		216.0	432.0	314.2

The data rate of each output channel is value that is obtained by total data rate divided by the number of channels.

Example) In All-pixel 506.8 [frame/s] mode: 4.752 [Gbps] / 8 = 594 [Mbps]

CHIMA DAHERINA IIISE ONIN For the setting value to register HMAX / VMAX, see the section of each drive mode settings

^{*3} Designated cropping area (ROI)

See the section of "ROI mode"

SONY

IMX287 FREQ (CID = 02h, Address = 1Bh, [1:0]) = 1h

Drive	Frame	Data		A/D conversion	Numb recordin	per of ng pixels		number xels ^{*2}		Number of INCK in 1H	
mode	rate [frame/s]	rate [Gbps]	Serial LVDS ch*1	(output gradation)	Н	V	н	V	INCK: 37.125 MHz	INCK: 74.25 MHz	INCK: 54 MHz
	487.3	2.376	8				1040		130.0	260.0	189.1
	275.4	1.188	4	10 (8)			920		230.0	460.0	334.6
All pixel	150.8	594	2	(0)	720	540	840	586	420.0	840.0	610.9
All pixel	319.9	2.376	8		720	540	1584	300	198.0	396.0	288.0
	285.3	1.188	4	12 (8)			888		222.0	444.0	322.9
	150.8	594	2	(0)			840		420.0	840.0	610.9
	*4	2.376	8	1			1040		130.0	260.0	189.1
	*4	1.188	4	10 (8)			920		230.0	460.0	334.6
ROI	*4	594	2	(0)	*3	*3	840	*4	420.0	840.0	610.9
KUI	*4	2.376	8				1584		198.0	396.0	288.0
	*4	1.188	4	12 (8)			888		222.0	444.0	322.9
	*4	594	2	(3)			840		420.0	840.0	610.9

The data rate of each output channel is value that is obtained by total data rate divided by the number of channels.

Example) In All-pixel 487.3 [frame/s] mode: 2.376 [Gbps] / 8 = 297 [Mbps]

CHIMA DAHERINA IIISE ONIN For the setting value to register HMAX / VMAX, see the section of each drive mode settings

^{*3} Designated cropping area (ROI)

See the section of "ROI mode"



Drive Mode Setting

Please refer to the product specification for register setup other than those list.

IMX273 (All pixel)

						Setting	y value			
					AD = 10 bit			AD = 12 bit		Remarks
Address	bit	Register name	Initial Value	8 ch	4 ch	2 ch	8 ch	4 ch	2 ch	
			value	262.8 [frame/s]	152.8 [frame/s]	82.1 [frame/s]	165.9 [frame/s]	154.2 [frame/s]	81.7 [frame/s]	FREQ = 0h
				149.3 [frame/s]	80.1 [frame/s]	42.1 [frame/s]	150.0 [frame/s]	80.5 [frame/s]	42.1 [frame/s]	FREQ = 1h
Chip ID =	02h	•	•		· · ·		. ,			
0Ch	[1:0]	ADBIT	0h	0h 1h						0: 10 bit 1: 12 bit
10h	[7:0]									
11h	[7:0]	VMAX	46Ah			46	Ah			1130 line
12h	[3:0]									
14h	[7:0]	HMAX	122h	7D0h	6E8h	640h	C60h	6A8h	648h	FREQ = 0h
15h	[7:0]	HIVIAX	12211	6E0h	668h	618h	6D8h	660h	618h	FREQ = 1h
16h	[1:0]	ODBIT	0h			2	h		•	2: 8 bit
1Bh	[1:0]	FREQ	0h	0h / 1h						

IMX273 (Vertical / Horizontal 1/2 subsampling)

						Setting	value			
					AD = 10 bit)	AD = 12 bit		Remarks
Address	bit	Register name	Initial Value	8 ch	4 ch	2 ch	8 ch	4 ch	2 ch	
			value	506.8 [frame/s]	506.8 [frame/s]	287.9 [frame/s]	319.9 [frame/s]	319.9 [frame/s]	293.3 [frame/s]	FREQ = 0h
				487.3 [frame/s]	275.4 [frame/s]	150.8 [frame/s]	319.9 [frame/s]	285.3 [frame/s]	150.8 [frame/s]	FREQ = 1h
Chip ID =	02h						,			
0Ch	[1:0]	ADBIT	0h		0h	a		1h		0: 10 bit 1: 12 bit
10h	[7:0]					1)				
11h	[7:0]	VMAX	46Ah			24	Ah			586 line
12h	[3:0]				~ ~	>				
14h	[7:0]	HMAX	122h	7D0h	3E8h	370h	C60h	630h	360h	FREQ = 0h
15h	[7:0]	HIVIAA	12211	410h	398h	348h	630h	378h	348h	FREQ = 1h
16h	[1:0]	ODBIT	0h			2	h			2: 8 bit
1Bh	[1:0]	FREQ	0h		,	0h /	/ 1h			

IMX273 (Vertical 2-pixel FD Binning, IMX273LLR only)

						Setting	g value				
		5	Initial		AD = 10 bit			AD = 12 bit		Remarks	
Address	bit	Register name	Value	8 ch	4 ch	2 ch	8 ch	4 ch	2 ch		
				506.8 [frame/s]	294.6 [frame/s]	158.3 [frame/s]	319.9 [frame/s]	297.4 [frame/s]	157.6 [frame/s]	FREQ = 0h	
Chip ID =	02h										
0Ch	[1:0]	ADBIT	0h	Oh 1h						0: 10 bit 1: 12 bit	
10h	[7:0]										
11h	[7:0]	VMAX	46Ah			24	Ah			586 line	
12h	[3:0]										
14h	[7:0]	HMAX	122h	7D0h	6B8h	640h	C60h	6A8h	C40h	EDEO OF	
15h	[7:0]	HIVIAX	12211	7D0N	00011	64011	Coun	DAOII	648h	FREQ = 0h	
16h	[1:0]	ODBIT	0h			2	th .			2: 8 bit	
1Bh	[1:0]	FREQ	0h		Oh						



IMX273 (2×2 Vertical FD binning, IMX273LLR only)

						Setting	y value				
A .l.d	6.24	D. sister assess	Initial		AD = 10 bit			AD = 12 bit		Remarks	
Address	bit	Register name	Value	8 ch	4 ch	2 ch	8 ch	4 ch	2 ch		
				506.8 [frame/s]	506.8 [frame/s]	287.9 [frame/s]	319.9 [frame/s]	319.9 [frame/s]	293.3 [frame/s]	FREQ = 0h	
Chip ID =	02h										
0Ch	[1:0]	ADBIT	0h	0h 1h						0: 10 bit 1: 12 bit	
10h	[7:0]										
11h	[7:0]	VMAX	46Ah			24	Ah			586 line	
12h	[3:0]										
14h	[7:0]	HMAX	122h	C60h	630h	360h	7D0h	3E8h	370h	FREQ = 0h	
15h	[7:0]	HIVIAA	12211	Coon	63011	36011	70011	35011	37011	FREQ = UII	
16h	[1:0]	ODBIT	0h			2	h			2: 8 bit	
1Bh	[1:0]	FREQ	0h		0h						

IMX273 (ROI)

						Setti	ng value			
Address	bit	Register name	Initial Value		AD = 10 bit			AD = 12 bit		Remarks
				8 ch	4 ch	2 ch	8 ch	4 ch	2 ch	
Chip ID =	02h						12			T
0Ch	[1:0]	ADBIT	0h		0h			1h		0: 10 bit 1: 12 bit
10h	[7:0]					•	N,			
11h	[7:0]	VMAX	46Ah				*			
12h	[3:0]						,			
14h	[7:0]	HMAX	122h	7D0h	6E8h	640h	C60h	6A8h	648h	FREQ = 0h
15h	[7:0]	HIVIAA	12211	6E0h	668h	618h	6D8h	660h	618h	FREQ = 1h
16h	[1:0]	ODBIT	0h				2h			2: 8 bit
1Bh	[1:0]	FREQ	0h			0	h / 1h			
VMAX =	= ROI\	WV1 + ROIV	VV2 + 4	12 AH	terna					
			N							



IMX287 (All pixel)

	bit	Register name	Initial Value	Setting value								
Address				AD = 10 bit			AD = 12 bit			Remarks		
				8 ch	4 ch	2 ch	8 ch	4 ch	2 ch	7		
				506.8 [frame/s]	506.8 [frame/s]	287.9 [frame/s]	319.9 [frame/s]	319.9 [frame/s]	293.3 [frame/s]	FREQ = 0h		
				487.3 [frame/s]	275.4 [frame/s]	150.8 [frame/s]	319.9 [frame/s]	285.3 [frame/s]	150.8 [frame/s]	FREQ = 1h		
Chip ID = 02h												
0Ch	[1:0]	ADBIT	0h	0h			1h			0: 10 bit 1: 12 bit		
10h	[7:0]	VMAX	46Ah									
11h	[7:0]			24Ah						586 line		
12h	[3:0]											
14h	[7:0]	HMAX	LINANY	LINANY	4001-	7D0h	3E8h	370h	C60h	630h	360h	FREQ = 0h
15h	[7:0]		122h	410h	398h	348h	630h	378h	348h	FREQ = 1h		
16h	[1:0]	ODBIT	0h	2h				2: 8 bit				
1Bh	[1:0]	FREQ	0h	0h / 1h								

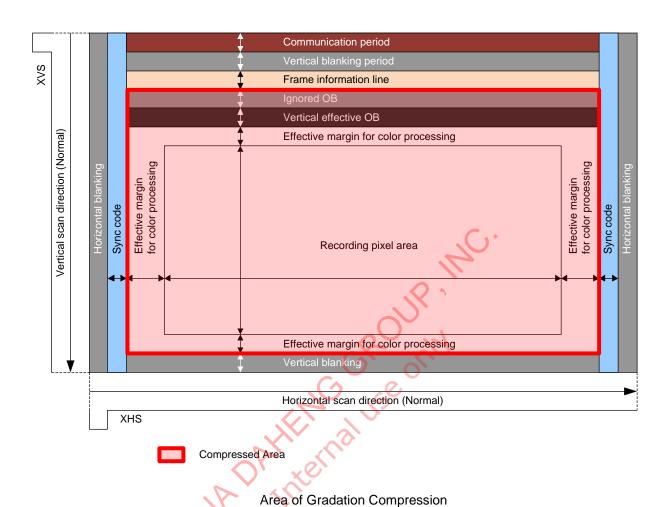
IMX287 (ROI)

	bit	Register name	Initial Value	Setting value						
Address				AD = 10 bit			AD = 12 bit			Remarks
				8 ch	4 ch	2 ch	8 ch	4 ch	2 ch	
Chip ID =	02h									
0Ch	[1:0]	ADBIT	0h	0h 1h			0: 10 bit 1: 12 bit			
10h	[7:0]		46Ah)			
11h	[7:0]	VMAX		20.14						
12h	[3:0]									
14h	[7:0]	LINANY	122h	7D0h	3E8h	370h	C60h	630h	360h	FREQ = 0h
15h	[7:0]	HMAX	12211	410h	398h	348h	630h	378h	348h	FREQ = 1h
16h	[1:0]	ODBIT	0h	2h				2: 8 bit		
1Bh	[1:0]	FREQ	0h		1	0h .	/ 1h			
VMAX = ROIWV1 + 42										
D'Age										
"The state of the										

^{*} VMAX = ROIWV1 + 42

Area of Gradation Compression

The area of Gradation Compression is as below.



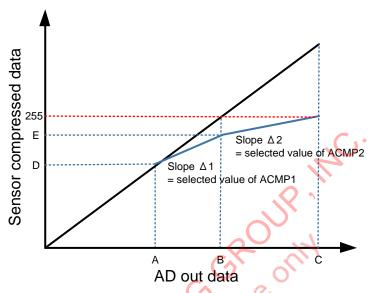
Description of Gradation Compression Function

This is the process which makes the output data be 8 bit.

Gradation Compression compress as below.

The setting which the result of compressed AD data is over 8 bit is prohibited.

In case of LVDS output, 0 and 255 which are compressed data output as 1 and 254. (Refer to section "Output Signal Range" on Datasheet.)



D = A = selected value of CCMP1

B = selected value of CCMP2

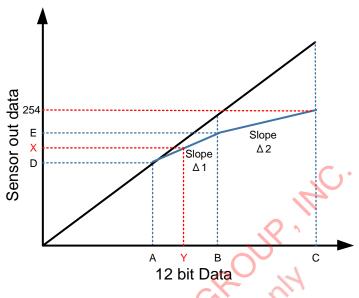
 $E = (B - A) * \Delta 1 + D$

 $255 = (C - B) * \Delta 2 + E$

The image of Gradation Compression

When the sensor outputs image data in Gradation Compression, it may be necessary for the following DSP to decompress the input data to process them properly. An example of inverse formula is shown below. In this case, division operations in the formula can be simply done with shift operations since $\Delta 1$ and $\Delta 2$ are power of 2.

In case of LVDS output, 0 and 255 which are compressed data output as 1 and 254. Because of it, these data can't be decompressed.



$$1 \le X < D$$
 : $Y = X$
 $D \le X < E$: $Y = (X - D) / \Delta 1 + A$
 $E \le X \le 254$: $Y = (X - E) / \Delta 2 + B$

The image of Gradation Decompression

Revision History

Version	Date	Page	Remarks	
Rev.0.1	20-Jan-17	_	First Edition	
		P1	Add: The note in case of saturate	
		P3	Correction: The description of 0001 in CCMP1 prohibited => 000h	
		P6	Correction: Data rate of ROI	
Rev.1.0	1-Sep-17	P14	Correction: The setting over 8bit is prohibited Add: Note of Output Signal Range of LVDS Correction: The figure	
		P15	Delete: About the saturated data Add: Note of Output Signal Range of LVDS Correction: The figure	

Correction: The figure