

IMX273 / IMX287 Application Note

Multi Frame Set Output Mode

The data except this specification conform to those of IMX273 / IMX287.

Description

The function to control the gain and the exposure time according to each frame is described in this document. Multi Frame Set Output is became possible the sequence control by setting the gain and the exposure time of each frame, assuming 2 frames or 4 frames to be one-set.

Features

- ◆ Control the integration time with registers on 2 frame set (Multi Frame Set Output mode 2 frame) and 4 frame set (Multi Frame Set Output mode 4 frame).
- ◆ Support each frame gain adjust function
- THINA DAILLE INTERNATION OF THE PROPERTY OF TH ◆ Sensor outputs the Frame ID (FID) and the Frame set signal in the frame information line.
- ◆ Support readout drive mode All-pixel scan mode

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Register Map

The register map for Multi Frame Set Output mode is shown below. Please refer to the product specification for register setup other than those list.

Registers corresponding to Chip ID = 02h in Write mode. (I2C:30**h)

Address	Bit	Register name	Description	Default Value	Reflection
Addless	Dit	Register flame	·	after reset	timing
	0	WDSEL	WD frame number setting 0d: Normal mode, 1d: Multi Frame Set Output mode 2 frame	0h	V
	1		2d: Setting prohibited 3d: Multi Frame Set Output mode 4 frame		
21h	2		Fixed to "0"	0	-
	3		Fixed to "0"	0	-
	4		Fixed to "0"	0	-
	5		Fixed to "0"	0	-
	6		Fixed to "0"	0	-
	7		Fixed to "0"	0	-
	0		LSB		
	1				
	2		· K		
8Dh	3		GROUN'S ONLY		
ODII	4		2011		
	5				
	6		0,		
	7		Storage time adjustment		
	0		Designated in line unit		
	1	SHS1	K, Y	0000Eh	V
	2		In Multi Frame Set Output mode,	0000211	•
8Eh	3		designated for FID : 1.		
02	4		(2 Frame and 4 Frame commonness)		
	5				
	6	CHIMAD!			
	7				
8Fh	0				
	1				
	2				
	3		MSB	_	
	4		Fixed to "0"	0	-
	5		Fixed to "0"	0	-
	6		Fixed to "0"	0	-
	7		Fixed to "0"	0	-

Address	Bit	Register name	Description	Default Value after reset	Reflection timing
	0		LSB		
	1				
	2				
	3				
90h	4				
	5				
	6				
	7		Storage time adjustment		
	0		Designated in line unit		
	1	CLICO	In Multi France Cat Cutavit made 2 France	000054	.,,
	2	SHS2	In Multi Frame Set Output mode 2 Frame, designated for FID : 0.	0000Eh	V
0.41	3		In Multi Frame Set Output mode 4 Frame,		
91h	4		designated for FID : 2.		
	5				
	6				
	7				
	0		. .		
	1		"12"		
	2				
	3		MSB		
92h	4		Fixed to "0"	0	-
	5		Fixed to "0"	0	-
	6		Fixed to "0"	0	-
	7		Storage time adjustment	0	-
	0		LSB (A)		
	1		20 50		
	2				
0.45	3				
94h	4				
	5	\bigcirc_{I}	VO.		
	6				
	7				
	0		Storage time adjustment		
	1	SHS3	Designated in line unit	000056	V
	2	31133	In Multi Frame Set Output mode 4 Frame,	0000Eh	V
95h	3		designated for FID : 3		
9311	4		g		
	5				
	6				
	7				
	0				
	1				
96h	2				
	3		MSB		
	4		Fixed to "0"	0	-
	5		Fixed to "0"	0	-
	6		Fixed to "0"	0	-
	7		Fixed to "0"	0	-

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Address	Bit	Register name	Description	Default Value after reset	Reflection timing
	0		LSB		
	1				
	2				
	3				
98h	4				
	5				
	6				
	7				
	0		Storage time adjustment		
	1	CHC4	Designated in line unit	000054	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
	2	SHS4	In Multi Frame Set Output mode 4 Frame,	0000Eh	V
004	3		designated for FID : 0		
99h	4		accignated to the		
	5				
	6				
	7				
	0		⊘ .		
	1		16		
	2				
9Ah	3		MSB		
3AII	4		Fixed to "0"	0	-
	5		Fixed to "0"	0	-
	6		Fixed to "0"	0	-
	7		Fixed to "0"	0	-
5 Fixed to "0" 0 - 6 Fixed to "0" 0 - 7 Fixed to "0" 0 -					

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Registers corresponding to Chip ID = 04h in Write mode. (I2C:32**h)

Address	Bit	Register name	Description	Default Value after reset	Reflection timing
	0		Fixed to "1"	1	-
	1		Fixed to "0"	0	-
	2		Fixed to "0"	0	-
	3		Fixed to "0"	0	-
	4		Fixed to "0"	0	-
00h	5		Fixed to "0"	0	-
			Setting of Multi Frame Set Output mode gain		
		WD CAIN MODE	function	0	
	О	6 WD_GAIN_MODE	0 : Normal mode	0	S
			1 : Each frame gain mode		
	7		Fixed to "0"	0	-
	0		LSB		
	1				
	2		Setting of gain adjustment		
0.41	3		Effective at "WD_GAIN_MODE=0"		
04h	4	GAIN	Designated for FID: 0 to 3 identical gain	000h	V
	5		Effective at "WD_GAIN_MODE=1"		
	6		Designated for FID : 0		
	7		Beerghated for Fib. 6		
	0		MSB		
	1		Fixed to "0"	0	-
	2		Fixed to "0"	0	-
0.51	3		Fixed to "0"	0	-
05h	4		Fixed to "0"	0	-
	5		Fixed to "0"	0	-
	6		Fixed to "0"	0	-
	7		Fixed to "0"	0	-
	0		LSB		
	1	O '	ש`		
	2				
0.01	3	- L	Setting of gain adjustment		
08h	4	GAIN1	Effective at "WD_GAIN_MODE=1"	000h	V
	5	CX,	Designated for FID : 1		
	6				
	7				
	0		MSB		
	1		Fixed to "0"	0	-
	2		Fixed to "0"	0	-
001	3		Fixed to "0"	0	-
09h	4		Fixed to "0"	0	-
	5		Fixed to "0"	0	-
	6		Fixed to "0"	0	-
	7		Fixed to "0"	0	-

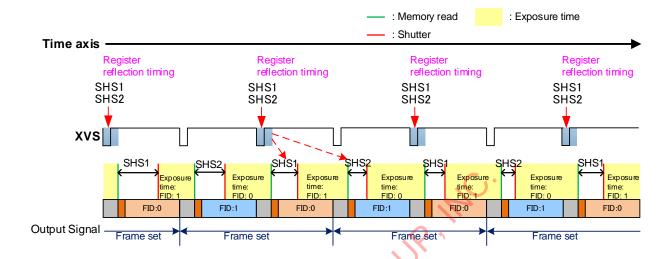
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Address	Bit	Register name	Description	Default Value after reset	Reflection timing
	0		LSB		, J
	1				
	2				
	3		Setting of gain adjustment		
0Ch	4	GAIN2	Effective at "WD_GAIN_MODE=1"	000h	V
	5		Designated for FID : 2		
	6		-		
	7				
	0		MSB		
	1		Fixed to "0"	0	-
	2		Fixed to "0"	0	-
	3		Fixed to "0"	0	-
0Dh	4		Fixed to "0"	0	-
	5		Fixed to "0"	0	-
	6		Fixed to "0"	0	-
	7		Fixed to "0"	0	-
	0		LSB		
	1		112		
	2				
	3		Setting of gain adjustment		
10h	4	GAIN3	Effective at "WD_GAIN_MODE=1"	000h	V
	5		Designated for FID : 3		
	6				
	7		Q, 9/2		
	0		MSB (
11h	1		Fixed to "0"	0	-
	2		Fixed to "0"	0	-
	3		Fixed to "0"	0	-
	4		Fixed to "0"	0	-
	5		Fixed to "0"	0	-
	6		Fixed to "0"	0	-
	7		Fixed to "0"	0	-

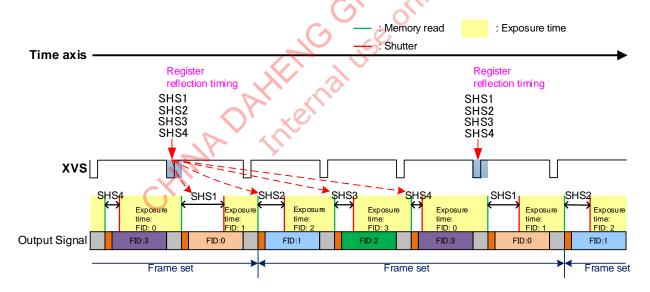
Reflection Timing

In normal mode, the setting of register is reflected in every frame after 4H period from the falling edge of XVS. In Multi Frame Set Output mode, the setting of register is reflected only if the Frame ID is "0d".

- ◆ 2 frame set: SHS1 > SHS2
- ◆ 4 frame set: SHS1 > SHS2 > SHS3 > SHS4



Timing of resister setting for Multi Frame Set Output mode 2 frame



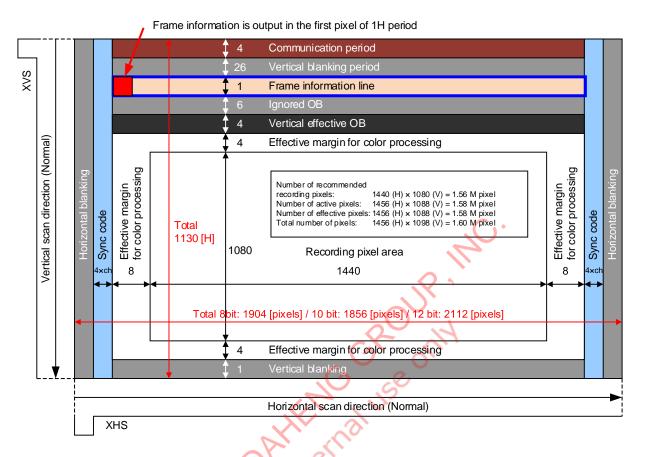
Timing of resister setting for Multi Frame Set Output mode 4 frame

The exposure time of each frames are according to value the following resister.

Frame ID	Multi Frame Set Output mode 2 frame [H]	Multi Frame Set Output mode 4 frame [H]
0	The number of line of 1 frame $-$ (SHS2) + 14.26 [μ s]	The number of line of 1 frame $-$ (SHS4) + 14.26 [μ s]
1	The number of line of 1 frame $-$ (SHS1) + 14.26 [μ s]	The number of line of 1 frame - (SHS1) + 14.26 [µs]
2	_	The number of line of 1 frame - (SHS2) + 14.26 [µs]
3	_	The number of line of 1 frame $-$ (SHS3) + 14.26 [µs]

Frame Information

Frame information line is output followed by V-blanking period. Frame ID is output at the first pixel of the Frame information line. (See the part framed in blue of figure below.) The frame identification signal table is shown below.



Frame information line output timing (In case of IMX273 All-pixel scan mode)

Output	8bit
[7]	1
[6]	Frame set
[5]	Frame ID [1]
[4]	Frame ID [0]
[3]	0
[2]	Frame set
[1]	Frame ID [1]
[0]	Frame ID [0]

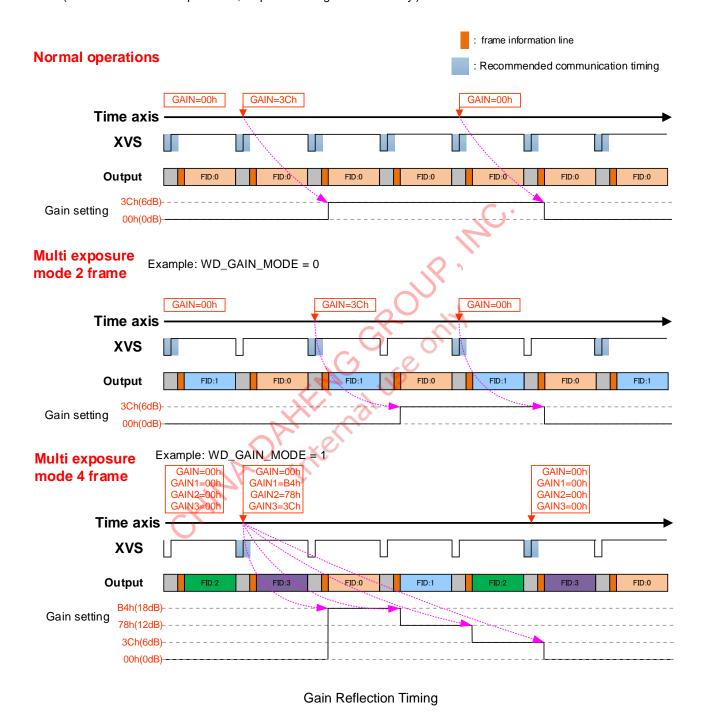
Output	10bit
[9]	1
[8]	Frame set
[7]	Frame ID [1]
[6]	Frame ID [0]
[5]	0
[4]	0
[3]	0
[2]	Frame set
[1]	Frame ID [1]
[0]	Frame ID [0]

Output	12bit
[11]	0
[10]	0
[9]	1
[8]	Frame set
[7]	Frame ID [1]
[6]	Frame ID [0]
[5]	0
[4]	0
[3]	0
[2]	Frame set
[1]	Frame ID [1]
[0]	Frame ID [0]
·	

Gain reflection timing

In Multi Frame Set Output mode, the reflection timing of register GAINx setting is delayed 1 frame. As a result, the gain setting is reflected collectively to the unit of frameset.

The difference between the normal mode and the Multi Frame Set Output mode is shown figure below. (In Multi Frame Set Output mode, a special setting is unnecessary.)



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Mode Transitions

There comes out invalid frames as follows when the mode transit from normal mode to Multi exposure mode.

Here describes only when normal and Multi Frame Set Output mode operate the same frame rate.

Changing the register value of FREQ, HMAX is prohibited.

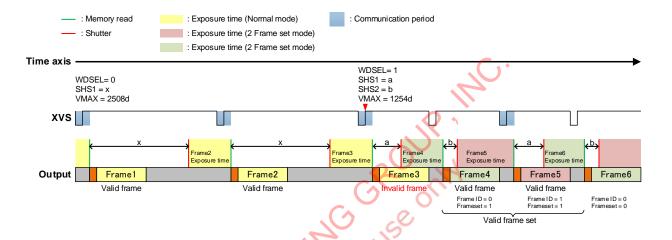
In case of transition between Multi Frame Set Output mode 2 frame and Multi Frame Set Output mode 4 frame, set via sensor standby.

In case of setting the Normal mode and combined frame in Multi Frame Set Output mode to be as the same frame rate

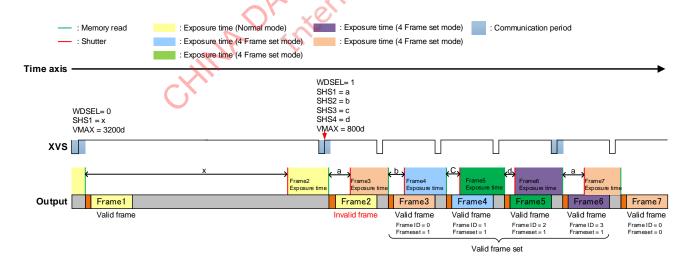
set the 1 frame period of normal mode which to be same as Multi Frame Set Output mode frame period.

◆ Transition from normal to Multi Frame Set Output mode

The transition setting frame become invalid.



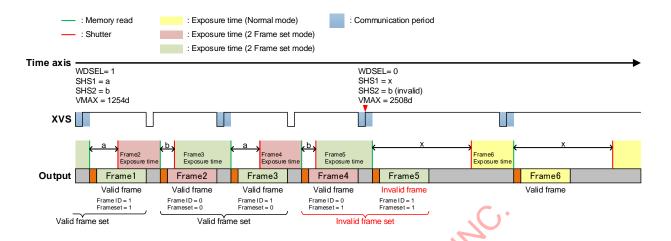
Transition to Multi Frame Set Output mode 2 frame from Normal mode



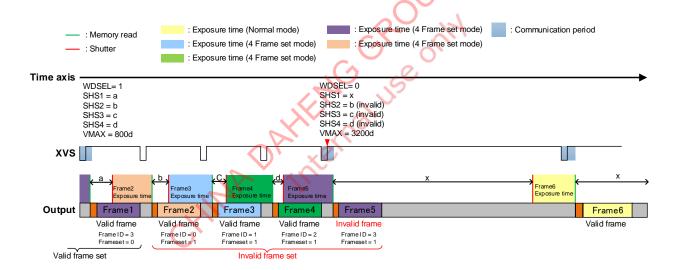
Transition to Multi Frame Set Output mode 4 frame from Normal mode

◆ Transition from Multi Frame Set Output mode to normal mode

The transition setting frame become invalid. Because the transition setting frame is long term exposure signal of Multi Frame Set Output mode frame set, the last signal set become invalid.



Transition to Normal mode from Multi Frame Set Output mode 2 frame



Transition to Normal mode from Multi Frame Set Output mode 4 frame

Revision History

Version	Date	Page	Remarks
Rev.0.1	20 – Jan. – 17	ı	First Edition
Rev.1.0	Rev.1.0 6 – Oct. – 17	8	Update: tOFFSET of the exposure time in the table.
		_	First Edition (Official Version)

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