SONY

IMX273 / IMX287 Application Note

Multi Frame Set Output Mode

The data except this specification conform to those of IMX273 / IMX287.

Description

The function to control the gain and the exposure time according to each frame is described in this document.
Multi Frame Set Output is became possible the sequence control by setting the gain and the exposure time of each frame, assuming 2 frames or 4 frames to be one-set.

Features

- ◆Control the integration time with registers on 2 frame set (Multi Frame Set Output mode 2 frame) and 4 frame set (Multi Frame Set Output mode 4 frame).
- ◆Support each frame gain adjust function
- ◆Sensor outputs the Frame ID (FID) and the Frame set signal in the frame information line.
- ◆Support readout drive mode
  All-pixel scan mode

Contents

Register Map

The register map for Multi Frame Set Output mode is shown below.
Please refer to the product specification for register setup other than those list.

Registers corresponding to Chip ID = 02h in Write mode. (I2C:30**h)

Address	Bit	Register name	Description	Default Value after reset	Reflection timing
21h	0 1	WDSEL	WD frame number setting 0d: Normal mode, 1d: Multi Frame Set Output mode 2 frame 2d: Setting prohibited 3d: Multi Frame Set Output mode 4 frame	0h	V
	2		Fixed to “0”	0	-
	3		Fixed to “0”	0	-
	4		Fixed to “0”	0	-
	5		Fixed to “0”	0	-
	6		Fixed to “0”	0	-
	7		Fixed to “0”	0	-
8Dh	0	SHS1	LSB	0000Eh	V
	1				
	2				
	3				
	4				
	5				
	6				
	7				
8Eh	0		Storage time adjustment Designated in line unit In Multi Frame Set Output mode, designated for FID : 1. (2 Frame and 4 Frame commonness)		
	1				
	2				
	3				
	4				
	5				
	6				
	7				
8Fh	0				
	1				
	2				
	3		MSB		
	4		Fixed to “0”	0	-
	5		Fixed to “0”	0	-
	6		Fixed to “0”	0	-
	7		Fixed to “0”	0	-

Address	Bit	Register name	Description	Default Value after reset	Reflection timing
90h	0	SHS2	LSB	0000Eh	V
	1				
	2				
	3				
	4				
	5				
	6				
	7		Storage time adjustment Designated in line unit		
91h	0				
	1				
	2		In Multi Frame Set Output mode 2 Frame, designated for FID : 0. In Multi Frame Set Output mode 4 Frame, designated for FID : 2.		
	3				
	4				
	5				
	6				
	7				
92h	0				
	1				
	2				
	3		MSB		
	4		Fixed to “0”	0	-
	5		Fixed to “0”	0	-
	6		Fixed to “0”	0	-
	7		Fixed to “0”	0	-
94h	0	SHS3	LSB	0000Eh	V
	1				
	2				
	3				
	4				
	5				
	6				
	7				
95h	0		Storage time adjustment Designated in line unit		
	1				
	2				
	3		In Multi Frame Set Output mode 4 Frame, designated for FID : 3		
	4				
	5				
	6				
	7				
96h	0				
	1				
	2				
	3		MSB		
	4		Fixed to “0”	0	-
	5		Fixed to “0”	0	-
	6		Fixed to “0”	0	-
	7		Fixed to “0”	0	-

Address	Bit	Register name	Description	Default Value after reset	Reflection timing
98h	0	SHS4	LSB	0000Eh	V
	1				
	2				
	3				
	4				
	5				
	6				
	7				
99h	0		Storage time adjustment Designated in line unit In Multi Frame Set Output mode 4 Frame, designated for FID : 0		
	1				
	2				
	3				
	4				
	5				
	6				
	7				
9Ah	0				
	1				
	2				
	3		MSB		
	4		Fixed to “0”	0	-
	5		Fixed to “0”	0	-
	6		Fixed to “0”	0	-
	7		Fixed to “0”	0	-

Registers corresponding to Chip ID = 04h in Write mode. (I2C:32**h)

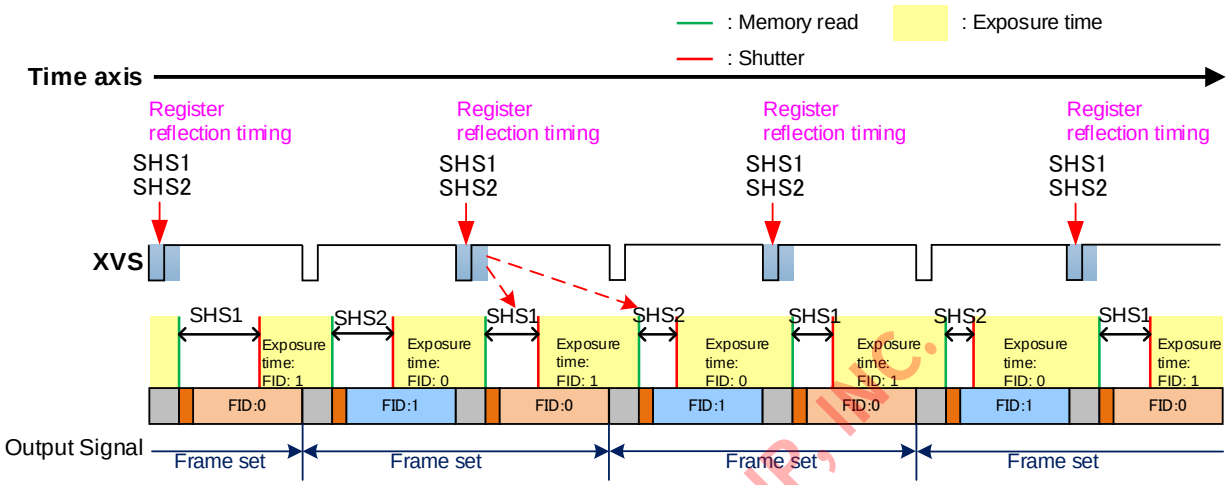
Address	Bit	Register name	Description	Default Value after reset	Reflection timing
00h	0		Fixed to “1”	1	-
	1		Fixed to “0”	0	-
	2		Fixed to “0”	0	-
	3		Fixed to “0”	0	-
	4		Fixed to “0”	0	-
	5		Fixed to “0”	0	-
	6	WD_GAIN_MODE	Setting of Multi Frame Set Output mode gain function 0 : Normal mode 1 : Each frame gain mode	0	S
	7		Fixed to “0”	0	-
04h	0	GAIN	LSB Setting of gain adjustment Effective at ”WD_GAIN_MODE=0” Designated for FID : 0 to 3 identical gain Effective at ”WD_GAIN_MODE=1” Designated for FID : 0	000h	V
	1				
	2				
	3				
	4				
	5				
	6				
	7				
05h	0		MSB		
	1		Fixed to “0”	0	-
	2		Fixed to “0”	0	-
	3		Fixed to “0”	0	-
	4		Fixed to “0”	0	-
	5		Fixed to “0”	0	-
	6		Fixed to “0”	0	-
	7		Fixed to “0”	0	-
08h	0	GAIN1	LSB Setting of gain adjustment Effective at ”WD_GAIN_MODE=1” Designated for FID : 1	000h	V
	1				
	2				
	3				
	4				
	5				
	6				
	7				
09h	0		MSB		
	1		Fixed to “0”	0	-
	2		Fixed to “0”	0	-
	3		Fixed to “0”	0	-
	4		Fixed to “0”	0	-
	5		Fixed to “0”	0	-
	6		Fixed to “0”	0	-
	7		Fixed to “0”	0	-

Address	Bit	Register name	Description	Default Value after reset	Reflection timing
0Ch	0	GAIN2	LSB Setting of gain adjustment Effective at ”WD_GAIN_MODE=1” Designated for FID : 2	000h	V
	1				
	2				
	3				
	4				
	5				
	6				
	7				
0Dh	0		MSB		
	1		Fixed to “0”	0	-
	2		Fixed to “0”	0	-
	3		Fixed to “0”	0	-
	4		Fixed to “0”	0	-
	5		Fixed to “0”	0	-
	6		Fixed to “0”	0	-
	7		Fixed to “0”	0	-
10h	0	GAIN3	LSB Setting of gain adjustment Effective at ”WD_GAIN_MODE=1” Designated for FID : 3	000h	V
	1				
	2				
	3				
	4				
	5				
	6				
	7				
11h	0		MSB		
	1		Fixed to “0”	0	-
	2		Fixed to “0”	0	-
	3		Fixed to “0”	0	-
	4		Fixed to “0”	0	-
	5		Fixed to “0”	0	-
	6		Fixed to “0”	0	-
	7		Fixed to “0”	0	-

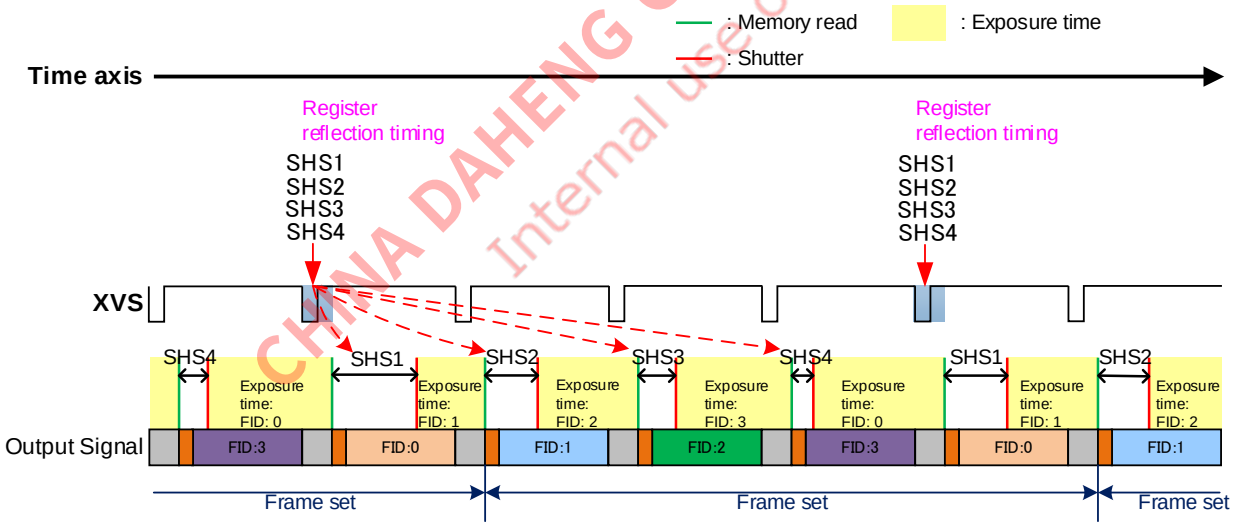
Reflection Timing

In normal mode, the setting of register is reflected in every frame after 4H period from the falling edge of XVS.
In Multi Frame Set Output mode, the setting of register is reflected only if the Frame ID is “0d”.

- 2 frame set: SHS1 > SHS2
- 4 frame set: SHS1 > SHS2 > SHS3 > SHS4



Timing of resister setting for Multi Frame Set Output mode 2 frame



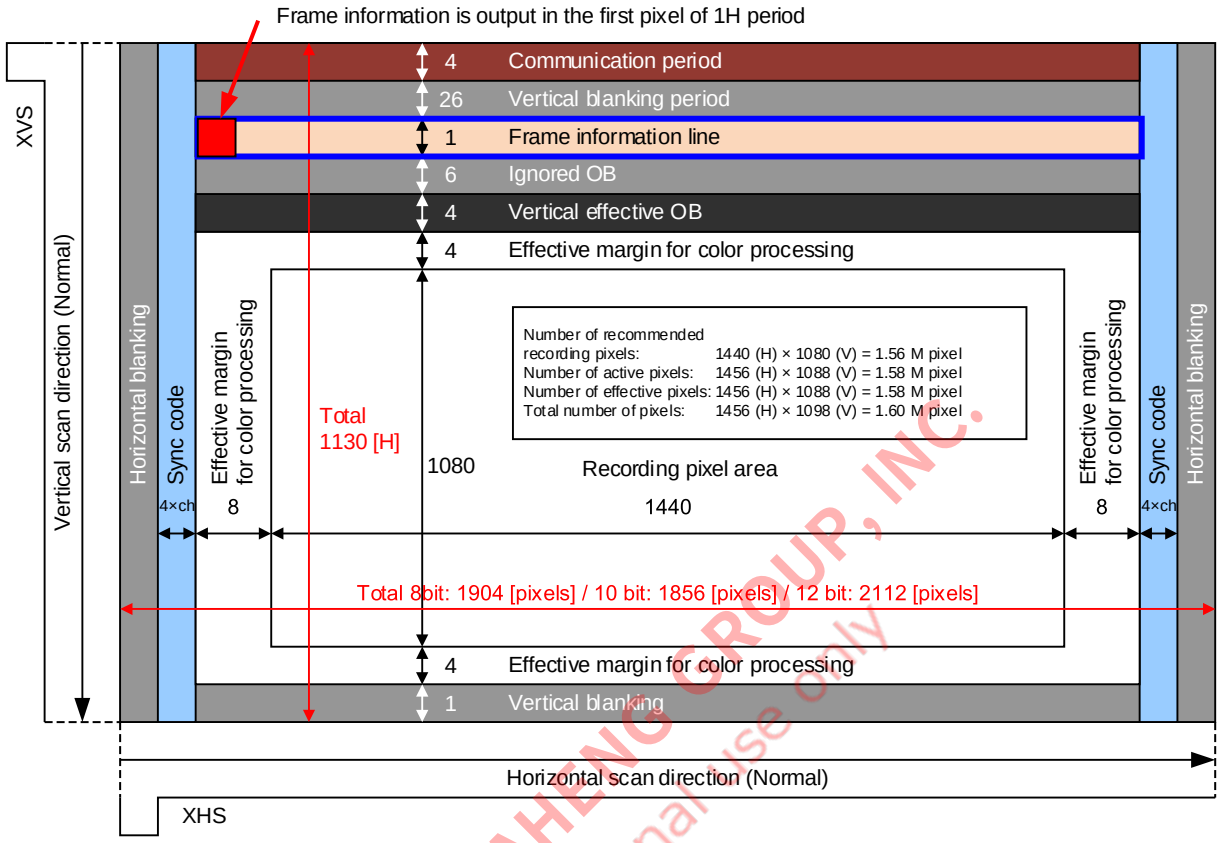
Timing of resister setting for Multi Frame Set Output mode 4 frame

The exposure time of each frames are according to value the following resister.

Frame ID	Multi Frame Set Output mode 2 frame [H]	Multi Frame Set Output mode 4 frame [H]
0	The number of line of 1 frame － (SHS2) + 14.26 [µs]	The number of line of 1 frame － (SHS4) + 14.26 [µs]
1	The number of line of 1 frame － (SHS1) + 14.26 [µs]	The number of line of 1 frame － (SHS1) + 14.26 [µs]
2	－	The number of line of 1 frame － (SHS2) + 14.26 [µs]
3	－	The number of line of 1 frame － (SHS3) + 14.26 [µs]

Frame Information

Frame information line is output followed by V-blanking period. Frame ID is output at the first pixel of the Frame information line. (See the part framed in blue of figure below.) The frame identification signal table is shown below.



Frame information line output timing (In case of IMX273 All-pixel scan mode)

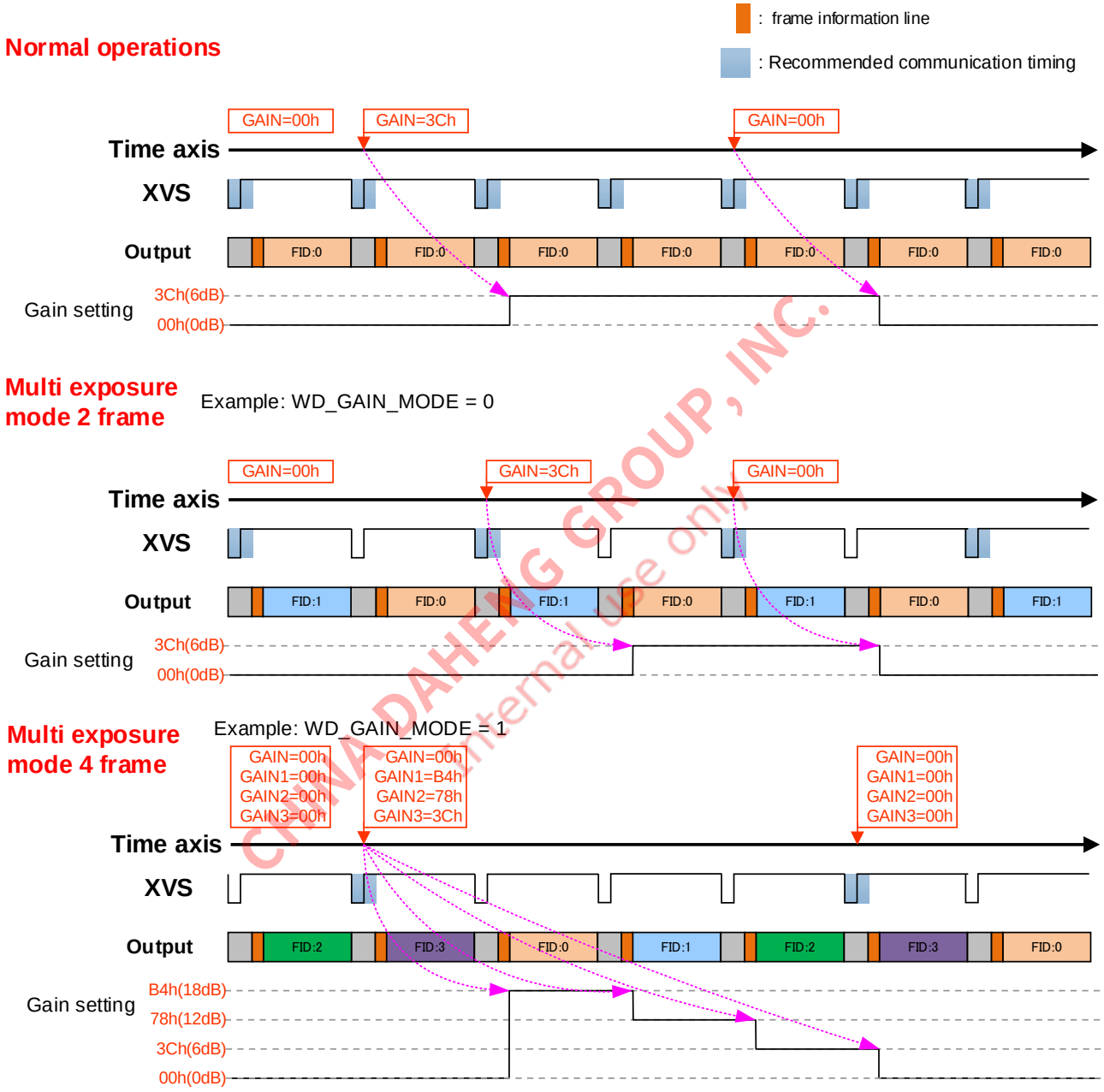
Output	8bit
[7]	1
[6]	Frame set
[5]	Frame ID [1]
[4]	Frame ID [0]
[3]	0
[2]	Frame set
[1]	Frame ID [1]
[0]	Frame ID [0]

Output	10bit
[9]	1
[8]	Frame set
[7]	Frame ID [1]
[6]	Frame ID [0]
[5]	0
[4]	0
[3]	0
[2]	Frame set
[1]	Frame ID [1]
[0]	Frame ID [0]

Output	12bit
[11]	0
[10]	0
[9]	1
[8]	Frame set
[7]	Frame ID [1]
[6]	Frame ID [0]
[5]	0
[4]	0
[3]	0
[2]	Frame set
[1]	Frame ID [1]
[0]	Frame ID [0]

Gain reflection timing

In Multi Frame Set Output mode, the reflection timing of register GAINx setting is delayed 1 frame. As a result, the gain setting is reflected collectively to the unit of frameset.
The difference between the normal mode and the Multi Frame Set Output mode is shown figure below.
(In Multi Frame Set Output mode, a special setting is unnecessary.)



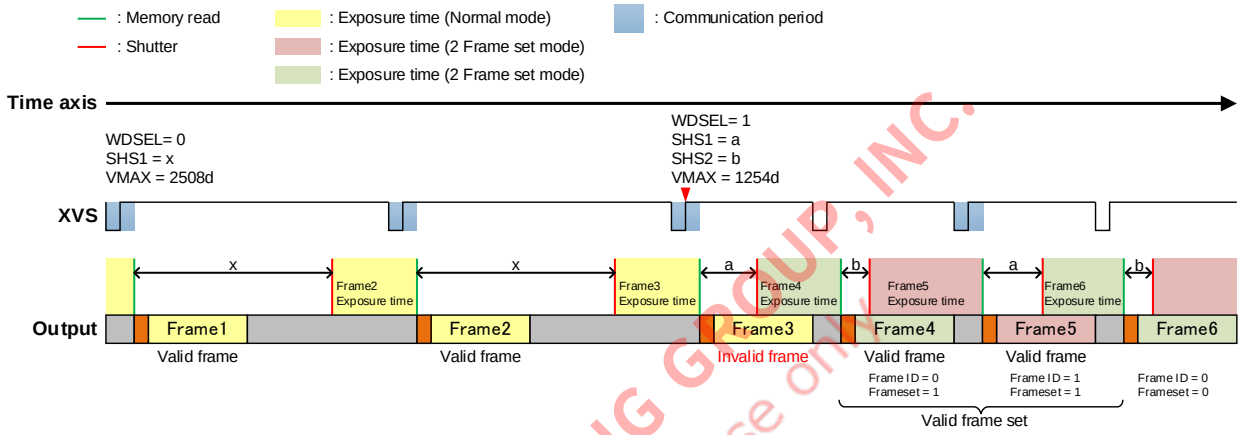
Gain Reflection Timing

Mode Transitions

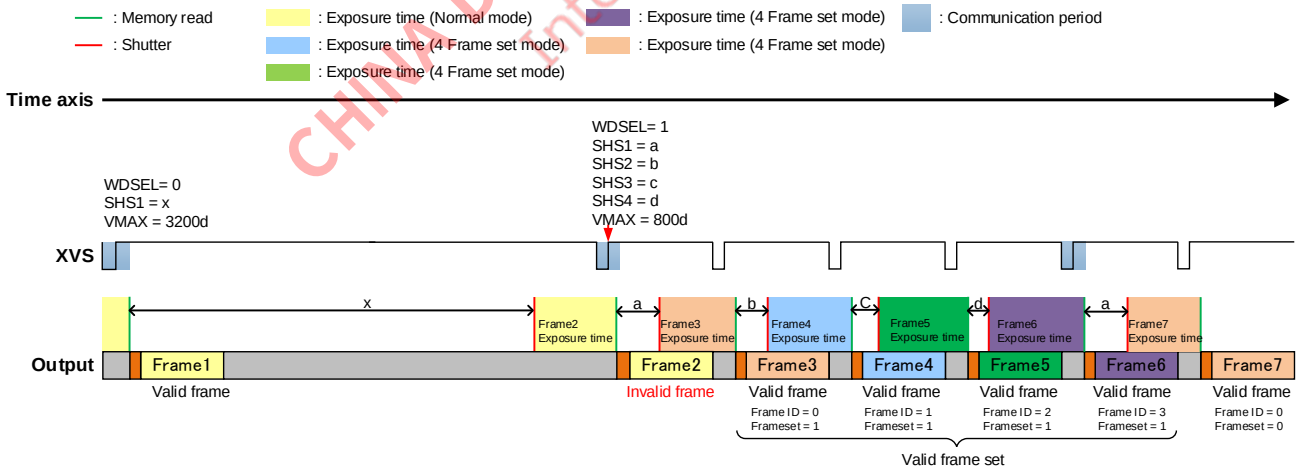
There comes out invalid frames as follows when the mode transit from normal mode to Multi exposure mode.
Here describes only when normal and Multi Frame Set Output mode operate the same frame rate.
Changing the register value of FREQ, HMAX is prohibited.
In case of transition between Multi Frame Set Output mode 2 frame and Multi Frame Set Output mode 4 frame, set via sensor standby.
In case of setting the Normal mode and combined frame in Multi Frame Set Output mode to be as the same frame rate,
set the 1 frame period of normal mode which to be same as Multi Frame Set Output mode frame period.

◆ Transition from normal to Multi Frame Set Output mode

The transition setting frame become invalid.



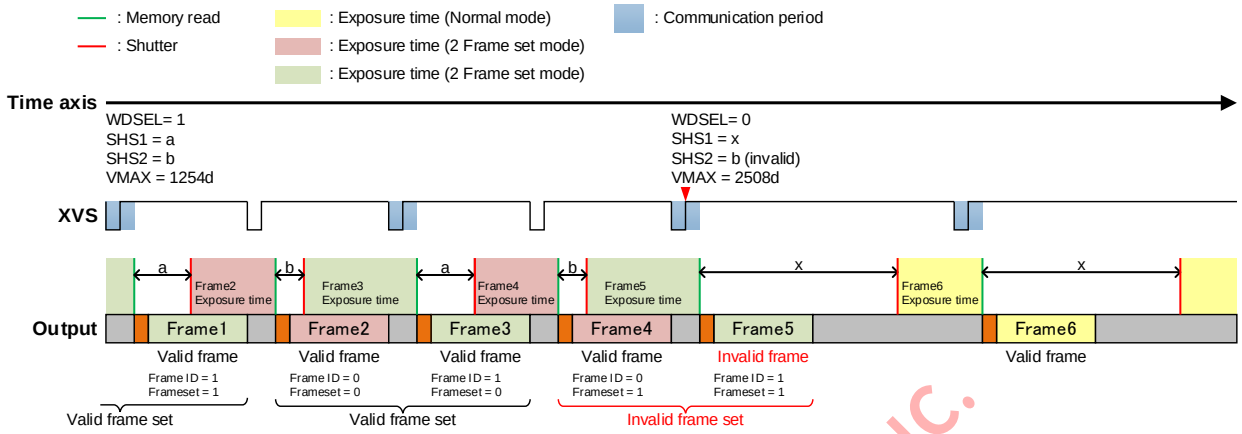
Transition to Multi Frame Set Output mode 2 frame from Normal mode



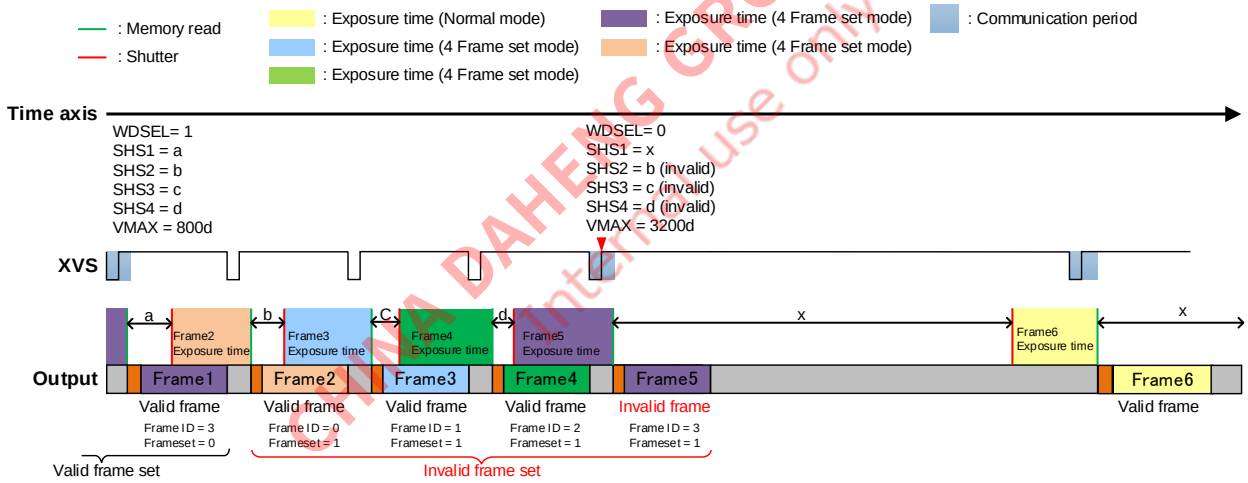
Transition to Multi Frame Set Output mode 4 frame from Normal mode

◆Transition from Multi Frame Set Output mode to normal mode

The transition setting frame become invalid. Because the transition setting frame is long term exposure signal of Multi Frame Set Output mode frame set, the last signal set become invalid.



Transition to Normal mode from Multi Frame Set Output mode 2 frame



Transition to Normal mode from Multi Frame Set Output mode 4 frame

Revision History

Version	Date	Page	Remarks
Rev.0.1	20 – Jan. – 17	–	First Edition
Rev.1.0	6 – Oct. – 17	8	Update: tOFFSET of the exposure time in the table.
		–	First Edition (Official Version)