SONY

IMX273 / IMX287 Application Note

Multi Frame ROI Mode

The data except this specification conform to those of IMX273 / IMX287

Description

The Multi Frame function on the ROI (Region Of Interest) mode is described in this document.
This function is became possible the sequence control by setting the gain and the exposure time of each frame, assuming Multi Frame ROI 2 frames or Multi Frame ROI 4 frames to be one-set.
Cropping position can set maximum 4 areas that specified by horizontal 2 points and vertical 2 points in IMX273, and can set maximum 1 area that specified by horizontal 1 point and vertical 1 point in IMX287, regarding effective pixel start position as origin (0, 0) in all pixel scan mode.

Features

- Cropping position can set maximum 4 areas that specified by horizontal 2 points and vertical 2 points in IMX273, and can set maximum 1 area that specified by horizontal 1 point and vertical 1 point in IMX287.
- Multi Frame ROI Mode is able to set the cropping position on each frames.
- Control the integration time with registers on 2 frames set (Multi Frame ROI 2 frames) and 4 frames set (Multi Frame ROI 4 frames).
- Support each frame gain adjust function
- Sensor outputs the Frame ID (FID) and the Frame set signal in the frame information line.
- Support readout drive mode
  All-pixel scan mode

Note) This function doesn't support Overlap ROI mode.

Contents

Register Map

Refer to the product specification for register setup other than those list.

Registers corresponding to Chip ID = 02h in Write mode. (I2C:30**h)

Address	Bit	Register name	Description	Default Value after reset	Reflection timing
00h	0	STANDBY [0]	Standby mode 0: Normal operation, 1: Standby	1d	I
	1		Fixed to “0”	0	—
	2		Fixed to “0”	0	—
	3		Fixed to “0”	0	—
	4		Fixed to “0”	0	—
	5		Fixed to “0”	0	—
	6		Fixed to “0”	0	—
	7		Fixed to “0”	0	—
21h	0	WDSEL	Multi frame number setting 0d: Normal mode, 1d: Multi Frame ROI mode 2 frames 2d: Setting prohibited 3d: Multi Frame ROI mode 4 frames	0d	V
	1				
	2		Fixed to “0”	0	—
	3		Fixed to “0”	0	—
	4		Fixed to “0”	0	—
	5		Fixed to “0”	0	—
	6		Fixed to “0”	0	—
	7		Fixed to “0”	0	—
8Dh	0	SHS1	LSB	0000Eh	V
	1				
	2				
	3				
	4				
	5				
	6				
	7				
8Eh	0		Storage time adjustment Designated in line unit In Multi Frame ROI mode, designated for FID : 1. (2 Frame and 4 Frame commonness)		
	1				
	2				
	3				
	4				
	5				
	6				
	7				
8Fh	0				
	1				
	2				
	3		MSB		
	4		Fixed to “0”	0	—
	5		Fixed to “0”	0	—
	6		Fixed to “0”	0	—
	7		Fixed to “0”	0	—

Address	Bit	Register name	Description	Default Value after reset	Reflection timing
90h	0	SHS2	LSB	0000Eh	V
	1				
	2				
	3				
	4				
	5				
	6				
	7		Storage time adjustment Designated in line unit		
91h	0				
	1				
	2		In Multi Frame ROI mode 2 frame, designated for FID : 0. In Multi Frame ROI mode 4 frame, designated for FID : 2.		
	3				
	4				
	5				
	6				
	7				
92h	0				
	1				
	2				
	3		MSB		
	4		Fixed to “0”	0	—
	5		Fixed to “0”	0	—
	6		Fixed to “0”	0	—
	7		Fixed to “0”	0	—
94h	0	SHS3	LSB	0000Eh	V
	1				
	2				
	3				
	4				
	5				
	6				
	7				
95h	0		Storage time adjustment Designated in line unit		
	1				
	2				
	3		In Multi Frame ROI mode 4 frame, designated for FID : 3		
	4				
	5				
	6				
	7				
96h	0				
	1				
	2				
	3		MSB		
	4		Fixed to “0”	0	—
	5		Fixed to “0”	0	—
	6		Fixed to “0”	0	—
	7		Fixed to “0”	0	—

Address	Bit	Register name	Description	Default Value after reset	Reflection timing
98h	0	SHS4	LSB	0000Eh	V
	1				
	2				
	3				
	4				
	5				
	6				
	7				
99h	0		Storage time adjustment Designated in line unit In Multi Frame ROI mode 4 frame, designated for FID : 0		
	1				
	2				
	3				
	4				
	5				
	6				
	7				
9Ah	0				
	1				
	2				
	3		MSB		
	4		Fixed to “0”	0	—
	5		Fixed to “0”	0	—
	6		Fixed to “0”	0	—
	7		Fixed to “0”	0	—
B0h	0	MFROI_EN	Enable control of Multi Frame ROI 0: Disable 1: Enable	0	S
	1		Fixed to “0”	0	—
	2		Fixed to “0”	0	—
	3		Fixed to “0”	0	—
	4		Fixed to “0”	0	—
	5		Fixed to “0”	0	—
	6		Fixed to “0”	0	—
	7		Fixed to “0”	0	—

Registers corresponding to Chip ID = 04h in Write mode. (I2C:32**h)

Address	Bit	Register name	Description	Default Value after reset	Reflection timing
00h	0		Fixed to “1”	1	—
	1		Fixed to “0”	0	—
	2		Fixed to “0”	0	—
	3		Fixed to “0”	0	—
	4		Fixed to “0”	0	—
	5		Fixed to “0”	0	—
	6	WD_GAIN_MODE	Setting of Multi Frame ROI gain function 0 : Normal mode 1 : Each frame gain mode	0	S
	7		Fixed to “0”	0	—
04h	0	GAIN	LSB Setting of gain adjustment Effective at ”WD_GAIN_MODE=0” Designated for FID : 0 to 3 identical gain Effective at ”WD_GAIN_MODE=1” Designated for FID : 0	000h	V
	1				
	2				
	3				
	4				
	5				
	6				
	7				
05h	0		MSB		
	1		Fixed to “0”	0	—
	2		Fixed to “0”	0	—
	3		Fixed to “0”	0	—
	4		Fixed to “0”	0	—
	5		Fixed to “0”	0	—
	6		Fixed to “0”	0	—
	7		Fixed to “0”	0	—
08h	0	GAIN1	LSB Setting of gain adjustment Effective at ”WD_GAIN_MODE=1” Designated for FID : 1	000h	V
	1				
	2				
	3				
	4				
	5				
	6				
	7				
09h	0		MSB		
	1		Fixed to “0”	0	—
	2		Fixed to “0”	0	—
	3		Fixed to “0”	0	—
	4		Fixed to “0”	0	—
	5		Fixed to “0”	0	—
	6		Fixed to “0”	0	—
	7		Fixed to “0”	0	—

Address	Bit	Register name	Description	Default Value after reset	Reflection timing
0Ch	0	GAIN2	LSB Setting of gain adjustment Effective at ”WD_GAIN_MODE=1” Designated for FID : 2	000h	V
	1				
	2				
	3				
	4				
	5				
	6				
	7				
0Dh	0		MSB		
	1		Fixed to “0”	0	—
	2		Fixed to “0”	0	—
	3		Fixed to “0”	0	—
	4		Fixed to “0”	0	—
	5		Fixed to “0”	0	—
	6		Fixed to “0”	0	—
	7		Fixed to “0”	0	—
10h	0	GAIN3	LSB Setting of gain adjustment Effective at ”WD_GAIN_MODE=1” Designated for FID : 3	000h	V
	1				
	2				
	3				
	4				
	5				
	6				
	7				
11h	0		MSB		
	1		Fixed to “0”	0	—
	2		Fixed to “0”	0	—
	3		Fixed to “0”	0	—
	4		Fixed to “0”	0	—
	5		Fixed to “0”	0	—
	6		Fixed to “0”	0	—
	7		Fixed to “0”	0	—

Registers corresponding to Chip ID = 05h in Write mode. (I2C:33**h)

The Chip ID = 05h registers of IMX287 doesn't support registers other than ROI area (1, 1).
Registers other than ROI area (1,1) are 00h[2:3], 02h[2:3], 18h to 1Fh and 58h to 5Fh.

Address	Bit	Register name	Description	Default Value after reset	Reflection timing
00h	0	FID0_ROIH1ON [0]	The horizontal setting of FID0 ROI area (1, y) (y = 1 to 2) 0: Disable 1: Enable	0	V
	1	FID0_ROIV1ON [0]	The vertical setting of FID0 ROI area (x, 1) (x = 1 to 2) 0: Disable 1: Enable	0	I
	2	FID0_ROIH2ON [0]	The horizontal setting of FID0 ROI area (2, y) (y = 1 to 2) 0: Disable 1: Enable	0	V
	3	FID0_ROIV2ON [0]	The vertical setting of FID0 ROI area (x, 2) (x = 1 to 2) 0: Disable 1: Enable	0	I
02h	0	FID1_ROIH1ON [0]	The horizontal setting of FID1 ROI area (1, y) (y = 1 to 2) 0: Disable 1: Enable	0	V
	1	FID1_ROIV1ON [0]	The vertical setting of FID1 ROI area (x, 1) (x = 1 to 2) 0: Disable 1: Enable	0	I
	2	FID1_ROIH2ON [0]	The horizontal setting of FID1 ROI area (2, y) (y = 1 to 2) 0: Disable 1: Enable	0	V
	3	FID1_ROIV2ON [0]	The vertical setting of FID1 ROI area (x, 2) (x = 1 to 2) 0: Disable 1: Enable	0	I
10h	[7:0]	FID0_ROIPH1 [12:0]	Designation of horizontal cropping position for FID0 on area (1, y) (y = 1 to 2) *Set the value of multiple of 4	0000h	V
11h	[4:0]				
	[7:5]		Fixed to "0"	0	—
12h	[7:0]	FID0_ROIPV1 [11:0]	Designation of vertical cropping position for FID0 on area (x, 1) (x = 1 to 2) *Set the value of multiple of 4	000h	I
13h	[3:0]				
	[7:4]		Fixed to "0"	0	—
14h	[7:0]	FID0_ROIWH1 [12:0]	Designation of horizontal cropping size for FID0 on area (1, y) (y = 1 to 2) *Set the value of multiple of 4	0000h	V
15h	[4:0]				
	[7:5]		Fixed to "0"	0	—
16h	[7:0]	FID0_ROIWV1 [11:0]	Designation of vertical cropping size for FID0 on area (x, 1) (x = 1 to 2) *Set the value of multiple of 4	000h	I
17h	[3:0]				
	[7:4]		Fixed to "0"	0	—
18h	[7:0]	FID0_ROIPH2 [12:0]	Designation of horizontal cropping position for FID0 on area (2, y) (y = 1 to 2) *Set the value of multiple of 4	0000h	V
19h	[4:0]				
	[7:5]		Fixed to "0"	0	—
1Ah	[7:0]	FID0_ROIPV2 [11:0]	Designation of vertical cropping position for FID0 on area (x, 2) (x = 1 to 2) *Set the value of multiple of 4	000h	I
1Bh	[3:0]				
	[7:4]		Fixed to "0"	0	—
1Ch	[7:0]	FID0_ROIWH2 [12:0]	Designation of horizontal cropping size for FID0 on area (2, y) (y = 1 to 2) *Set the value of multiple of 4	0000h	V
1Dh	[4:0]				
	[7:5]		Fixed to "0"	0	—
1Eh	[7:0]	FID0_ROIWV2 [11:0]	Designation of vertical cropping size for FID0 on area (x, 2) (x = 1 to 2) *Set the value of multiple of 4	000h	I
1Fh	[3:0]				
	[7:4]		Fixed to "0"	0	—

Address	Bit	Register name	Description	Default Value after reset	Reflection timing
50h	[7:0]	FID1_ROIPH1 [12:0]	Designation of horizontal cropping position for FID1 on area (1, y) (y = 1 to 2) *Set the value of multiple of 4	0000h	V
51h	[4:0]				
	[7:5]		Fixed to “0”	0	—
52h	[7:0]	FID1_ROIPV1 [11:0]	Designation of vertical cropping position for FID1 on area (x, 1) (x = 1 to 2) *Set the value of multiple of 4	000h	I
53h	[3:0]				
	[7:4]		Fixed to “0”	0	—
54h	[7:0]	FID1_ROIWH1 [12:0]	Designation of horizontal cropping size for FID1 on area (1, y) (y = 1 to 2) *Set the value of multiple of 4	0000h	V
55h	[4:0]				
	[7:5]		Fixed to “0”	0	—
56h	[7:0]	FID1_ROIWV1 [11:0]	Designation of vertical cropping size for FID1 on area (x, 1) (x = 1 to 2) *Set the value of multiple of 4	000h	I
57h	[3:0]				
	[7:4]		Fixed to “0”	0	—
58h	[7:0]	FID1_ROIPH2 [12:0]	Designation of horizontal cropping position for FID1 on area (2, y) (y = 1 to 2) *Set the value of multiple of 4	0000h	V
59h	[4:0]				
	[7:5]		Fixed to “0”	0	—
5Ah	[7:0]	FID1_ROIPV2 [11:0]	Designation of vertical cropping position for FID1 on area (x, 2) (x = 1 to 2) *Set the value of multiple of 4	000h	I
5Bh	[3:0]				
	[7:4]		Fixed to “0”	0	—
5Ch	[7:0]	FID1_ROIWH2 [12:0]	Designation of horizontal cropping size for FID1 on area (2, y) (y = 1 to 2) *Set the value of multiple of 4	0000h	V
5Dh	[4:0]				
	[7:5]		Fixed to “0”	0	—
5Eh	[7:0]	FID1_ROIWV2 [11:0]	Designation of vertical cropping size for FID1 on area (x, 2) (x = 1 to 2) *Set the value of multiple of 4	000h	I
5Fh	[3:0]				
	[7:4]		Fixed to “0”	0	—

Registers corresponding to Chip ID = 06h in Write mode. (I2C:34**h)

The Chip ID = 06h registers of IMX287 doesn't support registers other than ROI area (1, 1).
Registers other than ROI area (1,1) are 00h[2:3], 02h[2:3], 18h to 1Fh and 58h to 5Fh.

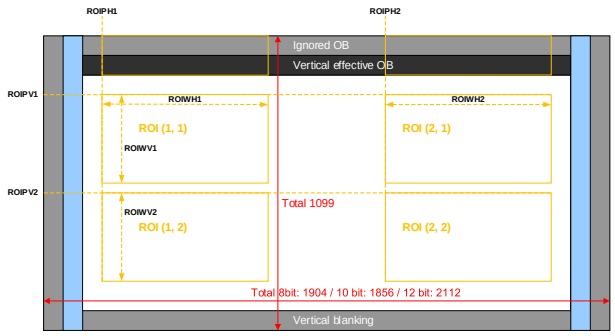
Address	Bit	Register name	Description	Default Value after reset	Reflection timing
00h	0	FID2_ROIH1ON [0]	The horizontal setting of FID2 ROI area (1, y) (y = 1 to 2) 0: Disable 1: Enable	0	V
	1	FID2_ROIV1ON [0]	The vertical setting of FID2 ROI area (x, 1) (x = 1 to 2) 0: Disable 1: Enable	0	I
	2	FID2_ROIH2ON [0]	The horizontal setting of FID2 ROI area (2, y) (y = 1 to 2) 0: Disable 1: Enable	0	V
	3	FID2_ROIV2ON [0]	The vertical setting of FID2 ROI area (x, 2) (x = 1 to 2) 0: Disable 1: Enable	0	I
02h	0	FID3_ROIH1ON [0]	The horizontal setting of FID3 ROI area (1, y) (y = 1 to 2) 0: Disable 1: Enable	0	V
	1	FID3_ROIV1ON [0]	The vertical setting of FID3 ROI area (x, 1) (x = 1 to 2) 0: Disable 1: Enable	0	I
	2	FID3_ROIH2ON [0]	The horizontal setting of FID3 ROI area (2, y) (y = 1 to 2) 0: Disable 1: Enable	0	V
	3	FID3_ROIV2ON [0]	The vertical setting of FID3 ROI area (x, 2) (x = 1 to 2) 0: Disable 1: Enable	0	I
10h	[7:0]	FID2_ROIPH1 [12:0]	Designation of horizontal cropping position for FID2 on area (1, y) (y = 1 to 2) *Set the value of multiple of 4	0000h	V
11h	[4:0]				
	[7:5]		Fixed to “0”	0	—
12h	[7:0]	FID2_ROIPV1 [11:0]	Designation of vertical cropping position for FID2 on area (x, 1) (x = 1 to 2) *Set the value of multiple of 4	000h	I
13h	[3:0]				
	[7:4]		Fixed to “0”	0	—
14h	[7:0]	FID2_ROIWH1 [12:0]	Designation of horizontal cropping size for FID2 on area (1, y) (y = 1 to 2) *Set the value of multiple of 4	0000h	V
15h	[4:0]				
	[7:5]		Fixed to “0”	0	—
16h	[7:0]	FID2_ROIWV1 [11:0]	Designation of vertical cropping size for FID2 on area (x, 1) (x = 1 to 2) *Set the value of multiple of 4	000h	I
17h	[3:0]				
	[7:4]		Fixed to “0”	0	—
18h	[7:0]	FID2_ROIPH2 [12:0]	Designation of horizontal cropping position for FID2 on area (2, y) (y = 1 to 2) *Set the value of multiple of 4	0000h	V
19h	[4:0]				
	[7:5]		Fixed to “0”	0	—
1Ah	[7:0]	FID2_ROIPV2 [11:0]	Designation of vertical cropping position for FID2 on area (x, 2) (x = 1 to 2) *Set the value of multiple of 4	000h	I
1Bh	[3:0]				
	[7:4]		Fixed to “0”	0	—
1Ch	[7:0]	FID2_ROIWH2 [12:0]	Designation of horizontal cropping size for FID2 on area (2, y) (y = 1 to 2) *Set the value of multiple of 4	0000h	V
1Dh	[4:0]				
	[7:5]		Fixed to “0”	0	—
1Eh	[7:0]	FID2_ROIWV2 [11:0]	Designation of vertical cropping size for FID2 on area (x, 2) (x = 1 to 2) *Set the value of multiple of 4	000h	I
1Fh	[3:0]				
	[7:4]		Fixed to “0”	0	—

Address	Bit	Register name	Description	Default Value after reset	Reflection timing
50h	[7:0]	FID3_ROIPH1 [12:0]	Designation of horizontal cropping position for FID3 on area (1, y) (y = 1 to 2) *Set the value of multiple of 4	0000h	V
51h	[4:0]				
	[7:5]		Fixed to “0”	0	—
52h	[7:0]	FID3_ROIPV1 [11:0]	Designation of vertical cropping position for FID3 on area (x, 1) (x = 1 to 2) *Set the value of multiple of 4	000h	I
53h	[3:0]				
	[7:4]		Fixed to “0”	0	—
54h	[7:0]	FID3_ROIWH1 [12:0]	Designation of horizontal cropping size for FID3 on area (1, y) (y = 1 to 2) *Set the value of multiple of 4	0000h	V
55h	[4:0]				
	[7:5]		Fixed to “0”	0	—
56h	[7:0]	FID3_ROIWV1 [11:0]	Designation of vertical cropping size for FID3 on area (x, 1) (x = 1 to 2) *Set the value of multiple of 4	000h	I
57h	[3:0]				
	[7:4]		Fixed to “0”	0	—
58h	[7:0]	FID3_ROIPH2 [12:0]	Designation of horizontal cropping position for FID3 on area (2, y) (y = 1 to 2) *Set the value of multiple of 4	0000h	V
59h	[4:0]				
	[7:5]		Fixed to “0”	0	—
5Ah	[7:0]	FID3_ROIPV2 [11:0]	Designation of vertical cropping position for FID3 on area (x, 2) (x = 1 to 2) *Set the value of multiple of 4	000h	I
5Bh	[3:0]				
	[7:4]		Fixed to “0”	0	—
5Ch	[7:0]	FID3_ROIWH2 [12:0]	Designation of horizontal cropping size for FID3 on area (2, y) (y = 1 to 2) *Set the value of multiple of 4	0000h	V
5Dh	[4:0]				
	[7:5]		Fixed to “0”	0	—
5Eh	[7:0]	FID3_ROIWV2 [11:0]	Designation of vertical cropping size for FID3 on area (x, 2) (x = 1 to 2) *Set the value of multiple of 4	000h	I
5Fh	[3:0]				
	[7:4]		Fixed to “0”	0	—

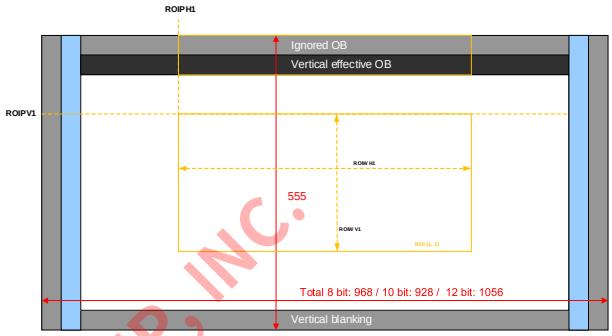
Setting concerning Multi Frame ROI

The setting of ROI is basically similar to the datasheet. Refer to the datasheet for details.
The setting of Multi Frame concerns is basically similar to the application note. Refer to the application note of Multi Frame Set Output mode.
However, Multi Frame ROI have the following restrictions.

◆ Cropping position can set maximum 4 areas that specified by horizontal 2 points and vertical 2 points in IMX273, and can set maximum 1 area that specified by horizontal 1 point and vertical 1 point in IMX287, regarding effective pixel start position as origin (0, 0) in all pixel scan mode.

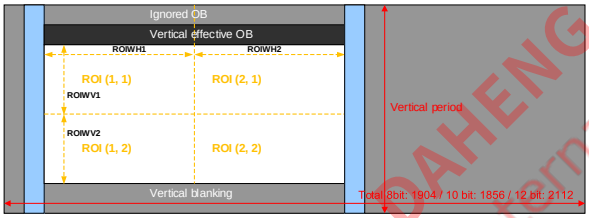


IMX273LLR FREQ = 0, 8 ch LVDS

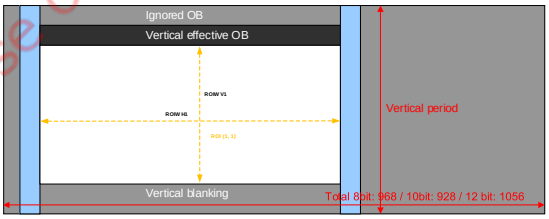


IMX287LLR FREQ = 0, 4 ch LVDS

Image Drawing of Designated Areas in ROI Mode



IMX273LLR FREQ = 0, 8 ch LVDS



IMX287LLR FREQ = 0, 4 ch LVDS

Details of Image Drawing

◆ Multi Frame ROI is able to set cropping address of each frame. But set the same values of ROI cropping size of each frame.

Set the same values to the following registers.

Multi Frame ROI 2 frames [*1] :
Designation of horizontal cropping size : FID0_ROIWH1 = FID1_ROIWH1, FID0_ROIWH2 = FID1_ROIWH2
Designation of vertical cropping size : FID0_ROIWV1 = FID1_ROIWV1, FID0_ROIWV2 = FID1_ROIWV2

Multi Frame ROI 4 frames [*1] :
Designation of horizontal cropping size : FID0_ROIWH1 = FID1_ROIWH1 = FID2_ROIWH1 = FID3_ROIWH1
FID0_ROIWH2 = FID1_ROIWH2 = FID2_ROIWH2 = FID3_ROIWH2

Designation of vertical cropping size : FID0_ROIWV1 = FID1_ROIWV1 = FID2_ROIWV1 = FID3_ROIWV1
FID0_ROIWV2 = FID1_ROIWV2 = FID2_ROIWV2 = FID3_ROIWV2

[*1] : IMX287 doesn't support each registers of FIDx_ROIWH2 and FIDx_ROIWV2. (x=0 to 3)

The register settings should satisfy following conditions:

* Do not designate area like be overlap.
・IMX273
ROIPH1 + ROIWH1 < ROIPH2
ROIPH2 + ROIWH2 ≤ The horizontal width at All-pixel scan. (1456d)

ROIPV1 + ROIWV1 < ROIPV2
ROIPV2 + ROIWV2 ≤ The vertical width at All-pixel scan. (1088d)

・IMX287
ROIPH1 + ROIWH1 ≤ 728d

ROIPV1 + ROIWV1 ≤ 574d

* Set the horizontal and vertical setting in multiple of 4

* Minimum width of the window is as below.
10 / 12 bit mode
ROIWH1 + ROIWH2 ≧ 260d (IMX273 / IMX287)

8 bit mode
ROIWH1 + ROIWH2 ≧ 516d (IMX273 / IMX287)

・8 / 10 / 12 bit mode
ROIWV1 + ROIWV2 ≧ 4d (IMX273 / IMX287)

Reflection timing of FID is same as Multi Frame Set Output Mode.

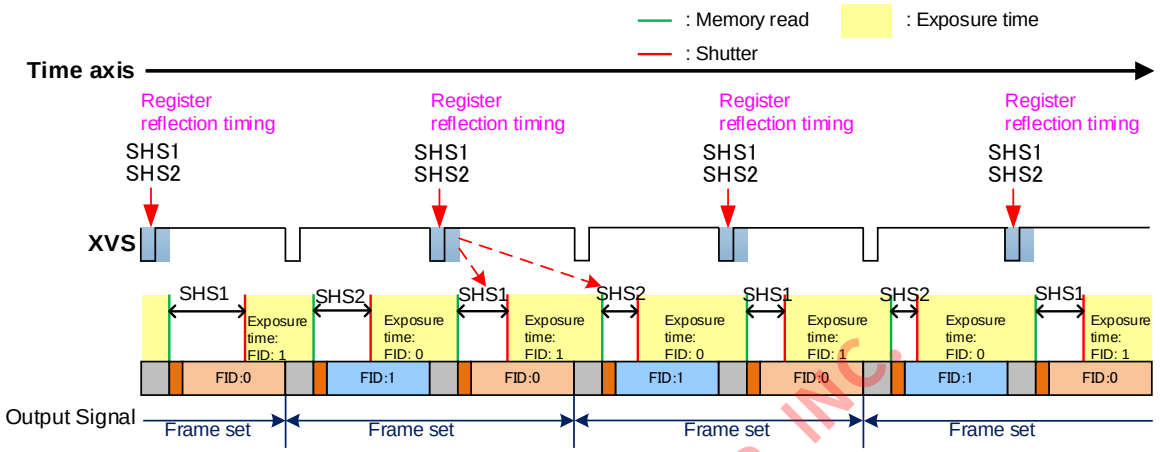
◆ Restrictions of register change and mode transition
It is recommended that the register change of ROI is done via sensor standby.
In case without sensor standby, a frame set becomes invalid.

The following mode transition must be done via sensor standby.
・In case of transition between Normal mode and Multi Frame ROI.
・In case of transition between Multi Frame ROI 2 frames and Multi Frame ROI 4 frames .

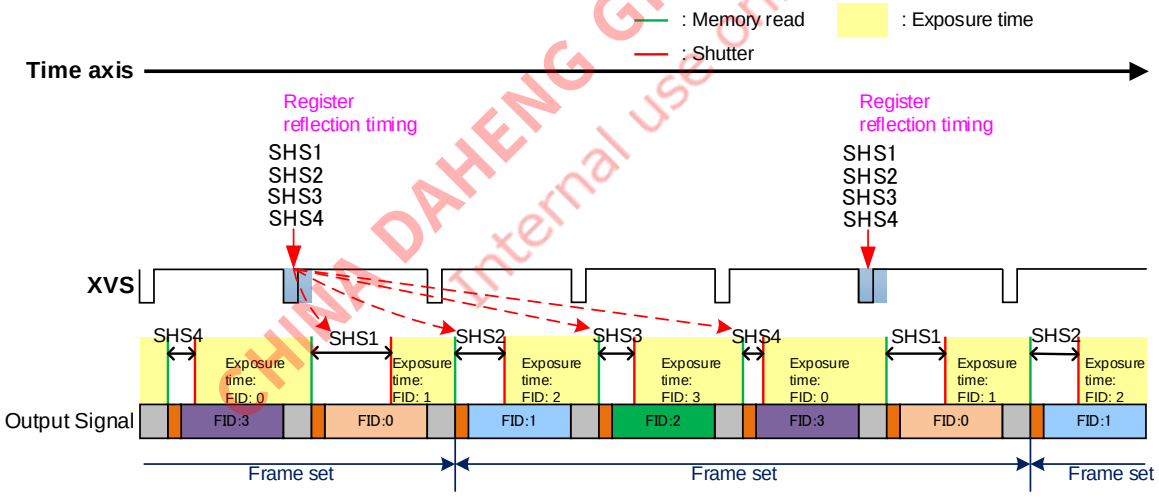
SHS Reflection Timing

In normal mode, the setting of register is reflected in every frame after 4H period from the falling edge of XVS.
In Multi Frame ROI, the setting of register is reflected only if the Frame ID is “0”.

- 2 frame set: SHS1 > SHS2
- 4 frame set: SHS1 > SHS2 > SHS3 > SHS4



Timing of resister setting for Multi Frame ROI 2 frames



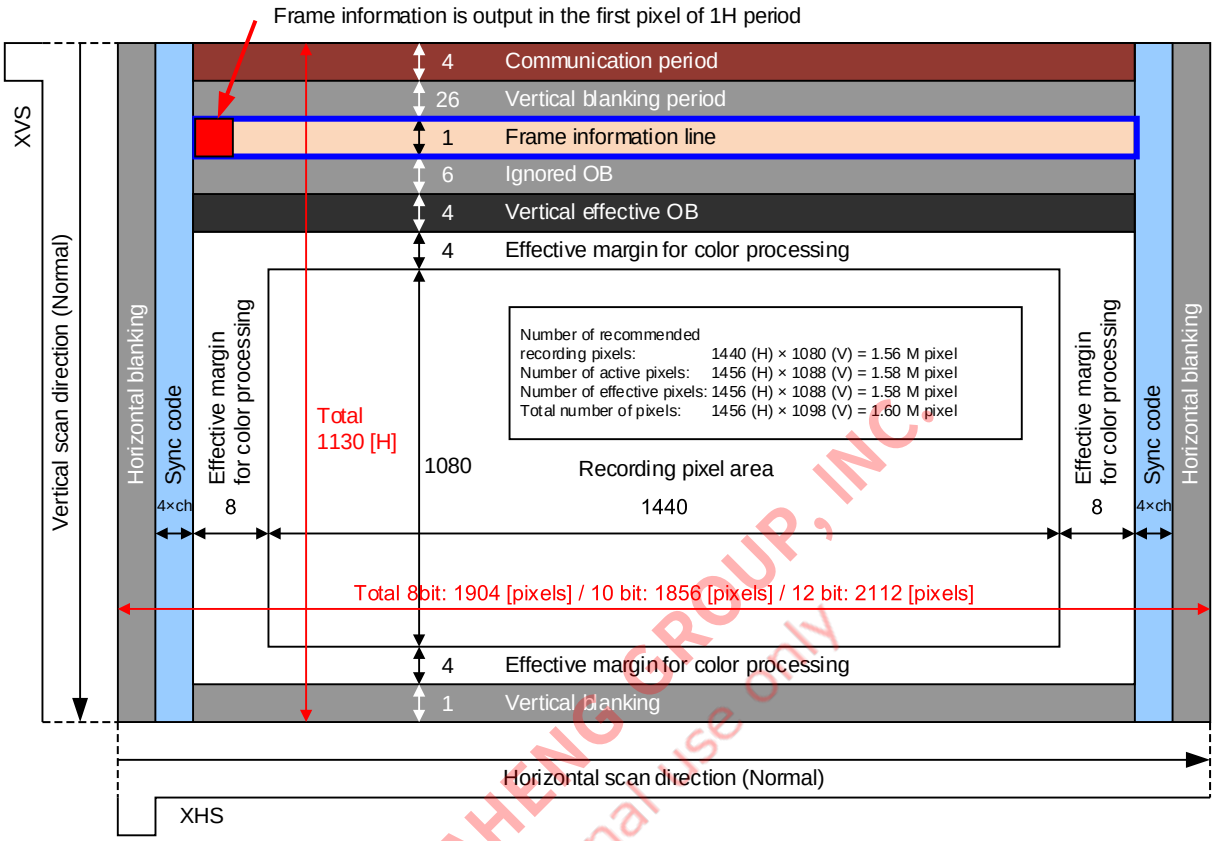
Timing of resister setting for Multi Frame ROI 4 frames

The exposure time of each frames are according to value the following resister.

Frame ID	Multi Frame ROI 2 frames [H]	Multi Frame ROI 4 frames [H]
0	The number of line of 1 frame – (SHS2) + 14.26 [µs]	The number of line of 1 frame – (SHS4) + 14.26 [µs]
1	The number of line of 1 frame – (SHS1) + 14.26 [µs]	The number of line of 1 frame – (SHS1) + 14.26 [µs]
2	–	The number of line of 1 frame – (SHS2) + 14.26 [µs]
3	–	The number of line of 1 frame – (SHS3) + 14.26 [µs]

Frame Information

Frame information line is output followed by V-blanking period. Frame ID is output at the first pixel of the Frame information line. (See the part framed in blue of figure below.) The frame identification signal table is shown below.



Frame information line output timing (In case of IMX273 All-pixel scan mode)

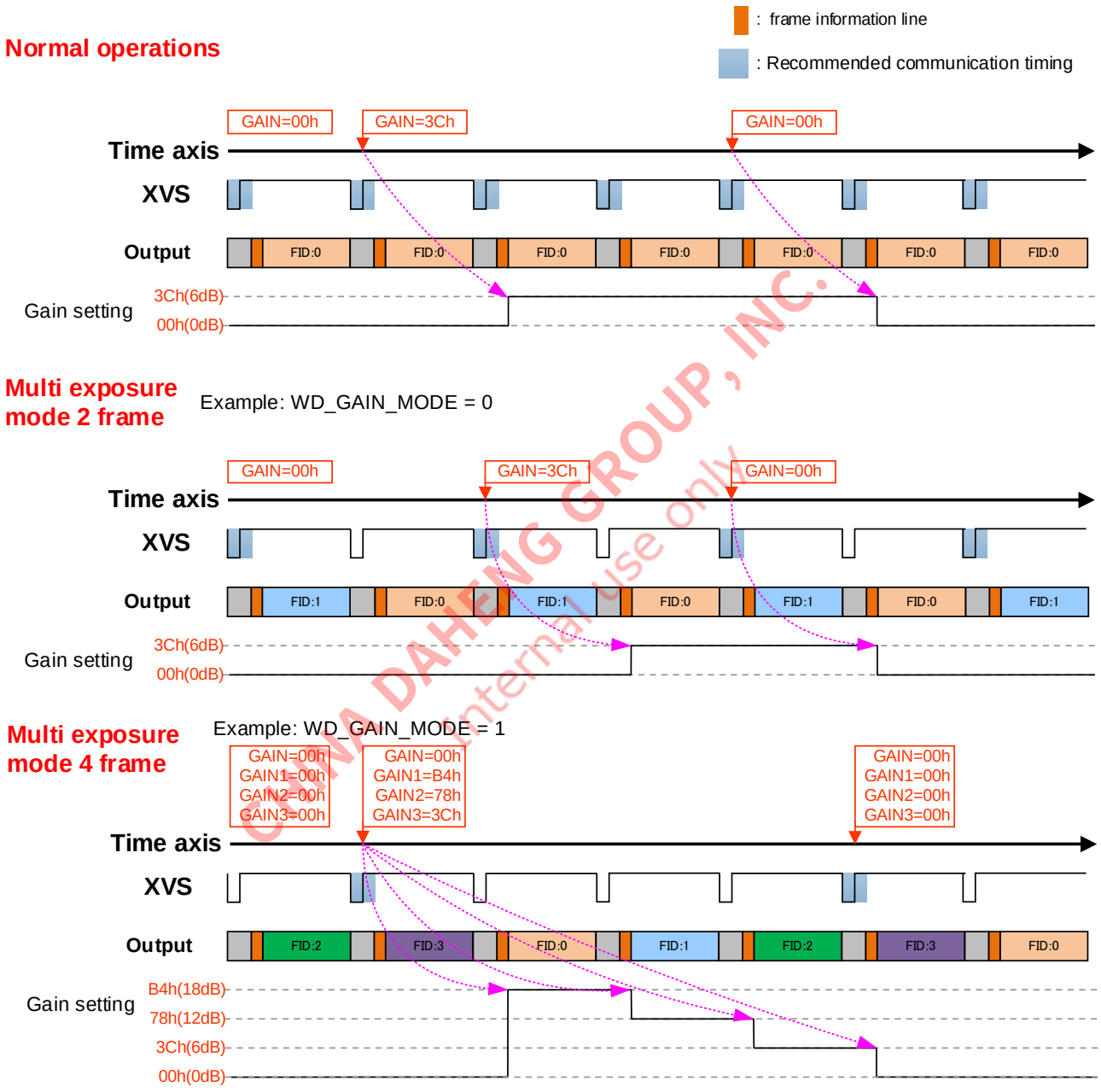
Output	8bit
[7]	1
[6]	Frame set
[5]	Frame ID [1]
[4]	Frame ID [0]
[3]	0
[2]	Frame set
[1]	Frame ID [1]
[0]	Frame ID [0]

Output	10bit
[9]	1
[8]	Frame set
[7]	Frame ID [1]
[6]	Frame ID [0]
[5]	0
[4]	0
[3]	0
[2]	Frame set
[1]	Frame ID [1]
[0]	Frame ID [0]

Output	12bit
[11]	0
[10]	0
[9]	1
[8]	Frame set
[7]	Frame ID [1]
[6]	Frame ID [0]
[5]	0
[4]	0
[3]	0
[2]	Frame set
[1]	Frame ID [1]
[0]	Frame ID [0]

Gain reflection timing

In Multi Frame ROI, the reflection timing of register GAINx setting is delayed 1 frame. As a result, the gain setting is reflected collectively to the unit of frameset.
The gain setting is able to set each frame by “WD_GAIN_MODE = 1”.
The difference between the normal mode and the Multi Frame ROI is shown figure below.
(In Multi Frame ROI, a special setting is unnecessary.)



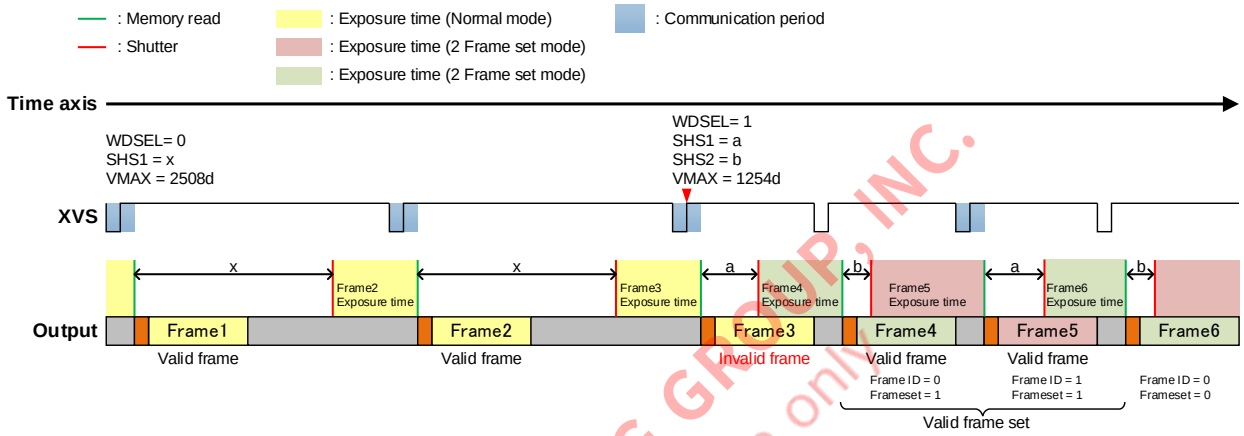
Gain Reflection Timing

Mode Transitions

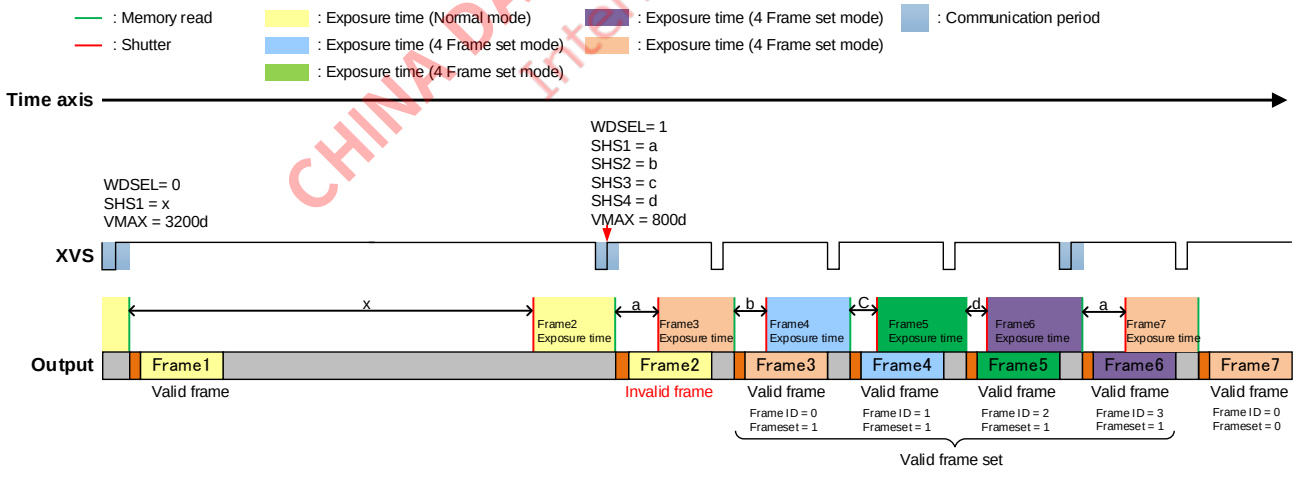
There comes out invalid frames as follows when the mode transit from normal mode to Multi exposure mode.
Here describes only when normal and Multi Frame ROI mode operate the same frame rate.
Changing the register value of FREQ, HMAX is prohibited.
In case of transition between Multi Frame ROI mode 2 frame and Multi Frame ROI mode 4 frame, set via sensor standby.
In case of setting the Normal mode and combined frame in Multi Frame ROI mode to be as the same frame rate, set the 1 frame period of normal mode which to be same as Multi Frame ROI mode frame period.

◆ Transition from normal to Multi Frame ROI mode

The transition setting frame become invalid.



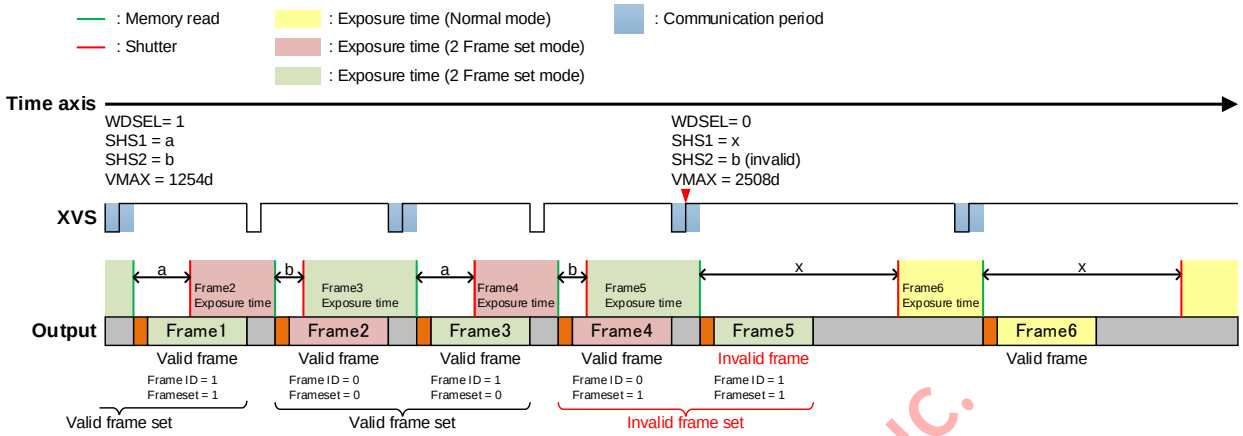
Transition to Multi Frame ROI mode 2 frame from Normal mode



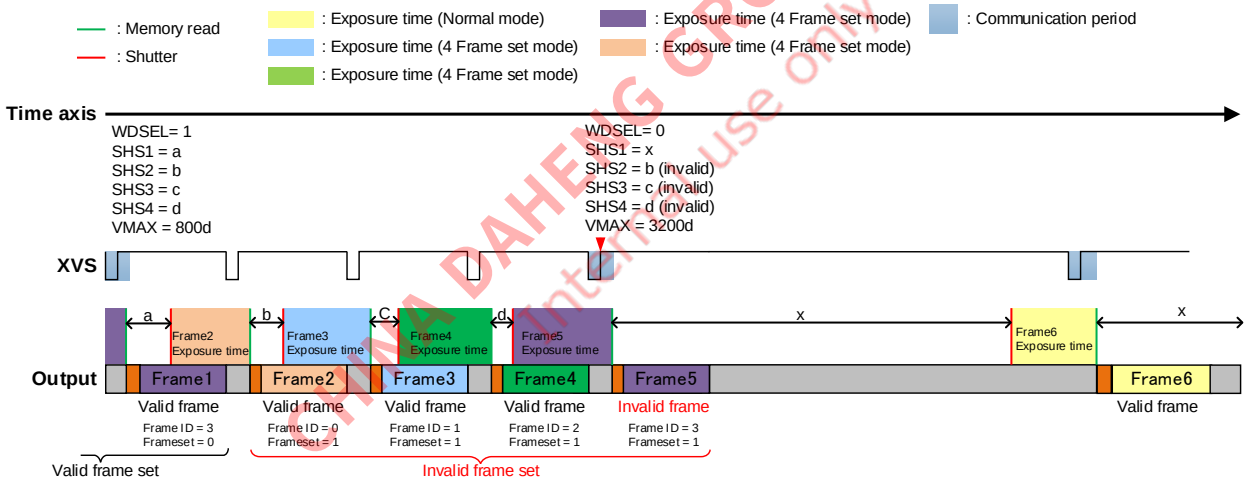
Transition to Multi Frame ROI mode 4 frame from Normal mode

◆Transition from Multi Frame ROI mode to normal mode

The transition setting frame become invalid. Because the transition setting frame is long term exposure signal of Multi Frame ROI mode frame set, the last signal set become invalid.



Transition to Normal mode from Multi Frame ROI mode 2 frame



Transition to Normal mode from Multi Frame ROI mode 4 frame

Revision History

Version	Date	Page	Remarks
Rev.0.1	27 – Jan. – 17	–	First Edition
Rev.1.0	6 – Oct. – 17	14	Update: tOFFSET of the exposure time in the table.
		–	First Edition (Official Version)