24-Bit, 96-kHz/192-kHz, 6-In/8-Out Audio Codec with Differential Input/Output

FEATURES

- **24-BIT ΔΣ ADC AND DAC**
- **SIX-CHANNEL ADC:**
  - **High Performance: Differential and Single-Ended, f_S = 48 kHz**
  - **THD+N: –93 dB (Differential), –93 dB (Single-Ended)**
  - **SNR: 107 dB (Differential), 104 dB (Single-Ended)**
  - **Dynamic Range: 107 dB (Differential), 104 dB (Single-Ended)**
  - **Sampling Rate: 8 kHz to 96 kHz**
  - **System Clock: 256 f_S, 384 f_S, 512 f_S, 768 f_S**
  - **Differential Voltage Input: 2 V_{RMS}**
  - **Single-Ended Voltage Input: 1 V_{RMS}**
  - **Decimation Filter:**
    - **Passband Ripple: ±0.035 dB**
    - **Stop Band Attenuation: –75 dB**
  - **On-Chip, High-Pass Filter: 0.96 Hz at f_S = 48 kHz**
  - **Overflow Flag**
- **EIGHT-CHANNEL DAC:**
  - **High Performance: Differential, f_S = 48 kHz**
  - **THD+N: –94 dB**
  - **SNR: 112 dB**
  - **Dynamic Range: 112 dB**
  - **Sampling Rate: 8 kHz to 192 kHz**
  - **System Clock: 128 f_S, 192 f_S, 256 f_S, 384 f_S, 512 f_S, 768 f_S**
  - **Differential Voltage Output: 8 V_{PP}**
  - **Analog Low-Pass Filter Included**
  - **4x/8x Oversampling Digital Filter:**
    - **Passband Ripple: ±0.0018 dB**
    - **Stop Band Attenuation: –75 dB**
  - **Zero Flag**

- **FLEXIBLE MODE CONTROL:**
  - **Four-Wire SPI™, Two-Wire I²C™ Compatible Serial Control Interface or Hardware Control**
- **MULTIPLE FUNCTIONS VIA SPI OR I²C I/F:**
  - **Audio I/F Mode/Format Select for ADC and DAC**
  - **Digital Attenuation and Soft Mute for ADC and DAC**
  - **Digital De-Emphasis: 32 kHz, 44.1 kHz, 48 kHz for DAC**
  - **Data Polarity Control for ADC and DAC**
  - **Power Down ADC/DAC Independently**
- **MULTI FUNCTIONS VIA H/W CONTROL:**
  - **Audio I/F Mode/Format Select**
  - **Digital De-Emphasis Filter: 44.1 kHz for DAC**
- **EXTERNAL RESET PIN:**
  - **ADC/DAC Simultaneous**
- **AUDIO INTERFACE MODE:**
  - **ADC/DAC Independent Master/Slave**
- **AUDIO DATA FORMAT:**
  - **ADC/DAC Independent I²S™, Left-Justified, Right-Justified, DSP, TDM**
- **POWER SUPPLIES: 5 V for Analog and 3.3 V for Digital**
- **PACKAGE: HTQFP-64**
- **OPERATING TEMPERATURE RANGE:**
  - **Consumer Grade: –40°C to +85°C**
  - **Automotive Audio Grade: –40°C to +105°C**

APPLICATIONS
- **CAR AUDIO EXTERNAL AMPLIFIERS**
- **CAR AUDIO AVN APPLICATIONS**
- **HOME THEATERS**
- **AV RECEIVERS**

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DESCRIPTION

The PCM3168A and PCM3168A-Q1 are high-performance, single-chip, 24-bit, 6-in/8-out, audio coders/decoders (codecs) with single-ended and differential selectable analog inputs and differential outputs. The six-channel, 24-bit analog-to-digital converter (ADC) employs a delta-sigma (ΔΣ) modulator and supports 8-kHz to 96-kHz sampling rates and a 16-bit/24-bit width digital audio output word on the audio interface. The eight-channel, 24-bit digital-to-analog converter (DAC) employs a ΔΣ modulator and supports 8-kHz to 192-kHz sampling rates and a 16-bit/24-bit width digital audio input word on the audio interface. Each audio interface supports I^{2}S, left-justified, right-justified, and DSP formats with 16-bit/24-bit word width. In addition, the PCM3168A and PCM3168A-Q1 support the time-division-multiplexed (TDM) format.

The PCM3168A and PCM3168A-Q1 can be controlled through a four-wire, SPI-compatible interface, or two-wire, I^{2}C-compatible serial interface in software, which provides access to all functions including digital attenuation, soft mute, de-emphasis, and so forth. Also, hardware control mode provides a subset of user-programmable functions through four control pins. The PCM3168A and PCM3168A-Q1 are available in a 12-mm × 12-mm (10-mm × 10-mm body) HTQFP-64 PowerPAD™ package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

Product Folder Link(s): *PCM3168A PCM3168A-Q1*

ABSOLUTE MAXIMUM RATINGS[1]

Over operating free-air temperature range (unless otherwise noted).

	PCM3168A, PCM3168A-Q1	UNIT
Supply voltage: VCCAD1, VCCAD2, VCCDA1, VCCDA2	−0.3 to +6.5	V
Supply voltage: VDD1, VDD2	−0.3 to +4.0	V
Ground voltage differences: AGNDAD1, AGNDAD2, AGNDDA1, AGNDDA2, DGND1, DGND2	±0.1	V
Supply voltage differences: VCCAD1, VCCAD2, VCCDA1, VCCDA2	±0.1	V
Supply voltage differences: VDD1, VDD2	±0.1	V
Digital input voltage: RST, MS, MC, MDI, SCK	−0.3 to +6.5	V
Digital input voltage: BCKAD/DA, LRCKAD/DA, DIN1/2/3/4, DOUT1/2/3, MODE, OVF, ZERO, MDO	−0.3 to (VDD + 0.3) < +4.0	V
Analog input voltage: VIN1-6±, VCOMAD/DA, VOUT1-8±, VREFAD1/2	−0.3 to (VCC + 0.3) < +6.5	V
Input current (all pins except supplies)	±10	mA
Ambient temperature range (under bias)	−40 to +125	°C
Storage temperature	−55 to +150	°C
Junction temperature	+150	°C
Lead temperature (soldering, 5s)	+260	°C
Package temperature (IR reflow, peak)	+260	°C

(1)   Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		PCM3168A, PCM3168A-Q1			UNIT
		MIN	TYP	MAX	
Analog supply voltage, VCC		4.5	5.0	5.5	V
Digital supply voltage, VDD		3.0	3.3	3.6	V
Digital Interface		LVTTL compatible			
Digital input clock frequency	Sampling frequency, LRCKAD/LRCKDA[1]	8		96/192[1]	kHz
	System clock frequency, SCKI	2.048		36.864	MHz
Analog input level	Single-ended		1		V$_{RMS}$
	Differential		2		V$_{RMS}$
Analog output voltage	Differential		8		V$_{PP}$
Analog output load resistance	To ac-coupled GND	5			kΩ
	To dc-coupled GND	15			kΩ
Analog output load capacitance				50	pF
Digital output load capacitance				20	pF
Operating free-air temperature	PCM3168A Consumer grade	−40	+25	+85	°C
	PCM3168A-Q1 Automotive audio grade	−40	+25	+105	°C

(1)   192 kHz is supported only for DAC.

PCM3168A
PCM3168A-Q1

ELECTRICAL CHARACTERISTICS: Digital Input/Output

All specifications at T_A = +25°C, VCCAD1 = VCCAD2 = VCCDA1 = VCCDA2 = 5 V, VDD1 = VDD2 = 3.3 V, f_S = 48 kHz, SCKI = 512 f_S, 24-bit data, Sampling Mode = Auto for ADC and DAC, and Interface Mode = Slave for ADC and DAC, unless otherwise noted.

PARAMETER		TEST CONDITIONS	PCM3168A, PCM3168A-Q1			UNIT
			MIN	TYP	MAX	
DATA FORMAT						
Audio data interface format			I^{2}S, LJ, RJ, DSP, TDM			
Audio data word length				16, 24		Bits
Audio data format			MSB first, twos complement			
Sampling frequency, ADC	f_S		8	48	96	kHz
Sampling frequency, DAC			8	48	192	kHz
System clock frequency		128 f_S, 192 f_S, 256 f_S, 384 f_S, 512 f_S, 768 f_S	2.048		36.864	MHz
INPUT LOGIC						
Input logic level	V_{IH}[1][2]		2.0		VDD	VDC
	V_{IL}[1][2]				0.8	VDC
Input logic level	V_{IH}[3][4]		2.0		5.5	VDC
	V_{IL}[3][4]				0.8	VDC
Input logic level	I_{IH}[2][3]	V_{IN} = VDD			±10	µA
	I_{IL}[2][3]	V_{IN} = 0 V			±10	µA
Input logic level	I_{IH}[1][4]	V_{IN} = VDD		+65	+100	µA
	I_{IL}[1][4]	V_{IN} = 0 V			±10	µA
OUTPUT LOGIC						
Output logic level	V_{OH}[5]	I_{OUT} = −4 mA	2.4			VDC
	V_{OL}[5][6]	I_{OUT} = +4 mA			0.4	VDC
REFERENCE INPUT/OUTPUT						
VREFAD1 output voltage				VCCAD1		V
VREFAD2 output voltage				AGNDAD1		V
VCOMAD output voltage				0.5 × VCCAD1		V
VCOMAD output impedance				10		kΩ
Allowable VCOMAD output source/sink current					1	µA
VCOMDA output voltage				0.5 × VCCDA1		V
VCOMDA output impedance				7.5		kΩ
Allowable VCOMDA output source/sink current					1	µA

(1) BCKAD, BCKDA, LRCKAD, and LRCKDA (in slave mode, Schmitt trigger input with 50-kΩ typical internal pull-down resistor).
(2) DIN1/2/3/4 and MDO/ADR1/MD1. (Except SPI mode, Schmitt trigger input).
(3) SCKI, MDI/SDA/DEMP, and MC/SCL/FMT (Schmitt trigger input, 5-V tolerant).
(4) RST and MS/ADR0/MD0 (Schmitt trigger input with 50-kΩ typical internal pull-down resistor, 5-V tolerant).
(5) BCKAD, BCKDA, LRCKAD, and LRCKDA (in master mode), DOUT1/2/3, ZERO, OVF, and MDO/ADR1/MD1 (in SPI mode).
(6) SDA (in I^{2}C mode, open-drain low output).

Product Folder Link(s): PCM3168A PCM3168A-Q1

ELECTRICAL CHARACTERISTICS: ADC Characteristics

All specifications at T_A = +25°C, VCCAD1 = VCCAD2 = VCCDA1 = VCCDA2 = 5 V, VDD1 = VDD2 = 3.3 V, f_S = 48 kHz, SCKI = 512 f_S, 24-bit data, Sampling Mode = Auto for ADC and DAC, and Interface Mode = Slave for ADC and DAC, unless otherwise noted.

PARAMETER	TEST CONDITIONS	PCM3168A, PCM3168A-Q1			UNIT
		MIN	TYP	MAX	
ADC CHARACTERISTICS					
Resolution		16	24		Bits
Full-scale input voltage	V_{IN} = 0 dB, Single-ended		0.2 × VCCAD1		V_{RMS}
	V_{IN} = 0 dB, Differential		0.4 × VCCAD1		V_{RMS}
Center voltage			0.5 × VCCAD1		V
Input impedance			45		kΩ
Common-mode rejection ratio			80		dB
DC ACCURACY					
Gain mismatch channel-to-channel	Full-scale input, V_{IN}		±2.0	±6	% of FSR
Gain error	Full-scale input, V_{IN}		±2.0	±6	% of FSR
Bipolar zero error	High-pass filter bypass, V_{IN}		±1.0		% of FSR
DYNAMIC PERFORMANCE[1][2]					
THD+N, V_{IN} = −1 dB	f_S = 48 kHz, Differential		−93	−87	dB
	f_S = 96 kHz, Differential		−93		dB
	f_S = 48 kHz, Single-ended		−93		dB
	f_S = 96 kHz, Single-ended		−93		dB
Dynamic range	f_S = 48 kHz, A-weighted, differential	100	107		dB
	f_S = 96 kHz, A-weighted, differential		107		dB
	f_S = 48 kHz, A-weighted, single-ended		104		dB
	f_S = 96 kHz, A-weighted, single-ended		104		dB
S/N ratio	f_S = 48 kHz, A-weighted, differential	100	107		dB
	f_S = 96 kHz, A-weighted, differential		107		dB
	f_S = 48 kHz, A-weighted, single-ended		104		dB
	f_S = 96 kHz, A-weighted, single-ended		104		dB
Channel separation (between one channel and others)	f_S = 48 kHz, Differential	98	104		dB
	f_S = 96 kHz, Differential		104		dB
	f_S = 48 kHz, Single-ended		101		dB
	f_S = 96 kHz, Single-ended		101		dB

(1) In differential mode at VINx± pin, f_{IN} = 1 kHz, using Audio Precision System II, RMS mode with 20-kHz low-pass filter and 400-Hz high-pass filter.
(2) f_S = 48 kHz : SCKI = 512 f_S (single), f_S = 96 kHz : SCKI = 256 f_S (dual), f_S = 192 kHz : SCKI = 128 f_S (quad).

ELECTRICAL CHARACTERISTICS: ADC Characteristics (continued)

All specifications at T_A = +25°C, VCCAD1 = VCCAD2 = VCCDA1 = VCCDA2 = 5 V, VDD1 = VDD2 = 3.3 V, f_S = 48 kHz, SCKI = 512 f_S, 24-bit data, Sampling Mode = Auto for ADC and DAC, and Interface Mode = Slave for ADC and DAC, unless otherwise noted.

PARAMETER	TEST CONDITIONS	PCM3168A, PCM3168A-Q1			UNIT
		MIN	TYP	MAX	
DIGITAL FILTER PERFORMANCE					
Passband (single)				$0.454 \times f_S$	Hz
Passband (dual)				$0.454 \times f_S$	Hz
Stop band (single)		$0.555 \times f_S$			Hz
Stop band (dual)		$0.597 \times f_S$			Hz
Passband ripple	$< 0.454 \times f_S$, $0.454 \times f_S$			±0.035	dB
Stop band attenuation	$> 0.555 \times f_S$, $0.597 \times f_S$	−75			dB
Group delay time (single)			$27/f_S$		sec
Group delay time (dual)			$17/f_S$		sec
High-pass filter frequency response	−3 dB		$0.02 \times f_S/1000$		Hz

ELECTRICAL CHARACTERISTICS: DAC Characteristics

All specifications at T_A = +25°C, VCCAD1 = VCCAD2 = VCCDA1 = VCCDA2 = 5 V, VDD1 = VDD2 = 3.3 V, f_S = 48 kHz, SCKI = 512 f_S, 24-bit data, Sampling Mode = Auto for ADC and DAC, and Interface Mode = Slave for ADC and DAC, unless otherwise noted.

PARAMETER	TEST CONDITIONS	PCM3168A, PCM3168A-Q1			UNIT
		MIN	TYP	MAX	
DAC CHARACTERISTICS					
Resolution		16	24		Bits
DC ACCURACY					
Gain mismatch channel-to-channel			±2.0	±6	% of FSR
Gain error			±2.0	±6	% of FSR
Bipolar zero error			±1.0		% of FSR
DYNAMIC PERFORMANCE[1][2]					
THD+N, V_{OUT} = 0 dB	f_S = 48 kHz		−94	−88	dB
	f_S = 96 kHz		−94		dB
	f_S = 192 kHz		−94		dB
Dynamic range	f_S = 48 kHz, EIAJ, A-weighted	105	112		dB
	f_S = 96 kHz, EIAJ, A-weighted		112		dB
	f_S = 192 kHz, EIAJ, A-weighted		112		dB
S/N ratio	f_S = 48 kHz, EIAJ, A-weighted	105	112		dB
	f_S = 96 kHz, EIAJ, A-weighted		112		dB
	f_S = 192 kHz, EIAJ, A-weighted		112		dB
Channel separation (between one channel and others)	f_S = 48 kHz	102	108		dB
	f_S = 96 kHz		108		dB
	f_S = 192 kHz		108		dB

(1) In differential mode at VOUTx± pin, f_{OUT} = 1 kHz, using Audio Precision System II, RMS mode with 20-kHz low-pass filter and 400-Hz high-pass filter.
(2) f_S = 48 kHz : SCKI = 512 f_S (single), f_S = 96 kHz : SCKI = 256 f_S (dual), f_S = 192 kHz : SCKI = 128 f_S (quad).

ELECTRICAL CHARACTERISTICS: DAC Characteristics (continued)

All specifications at T_A = +25°C, VCCAD1 = VCCAD2 = VCCDA1 = VCCDA2 = 5 V, VDD1 = VDD2 = 3.3 V, f_S = 48 kHz, SCKI = 512 f_S, 24-bit data, Sampling Mode = Auto for ADC and DAC, and Interface Mode = Slave for ADC and DAC, unless otherwise noted.

PARAMETER		TEST CONDITIONS	PCM3168A, PCM3168A-Q1			UNIT
			MIN	TYP	MAX	
ANALOG OUTPUT						
Output voltage		Differential		1.6 × VCCDA1		V_{PP}
Center voltage				0.5 × VCCDA1		V
Load impedance		To ac-coupled GND[3]	5			kΩ
		To dc-coupled GND[3]	15			kΩ
Low-pass filter frequency response		f = 20 kHz		−0.04		dB
		f = 44 kHz		−0.18		dB
DIGITAL FILTER PERFORMANCE[4]		Sharp roll-off				
Passband (single, dual)					0.454 × f_S	Hz
Passband (quad)					0.432 × f_S	Hz
Stop band (single, dual)			0.546 × f_S			Hz
Stop band (quad)			0.569 × f_S			Hz
Passband ripple		< 0.454 × f_S, 0.432 × f_S			±0.0018	dB
Stop band attenuation		> 0.546 × f_S, 0.569 × f_S	−75			dB
DIGITAL FILTER PERFORMANCE		Slow roll-off				
Passband					0.328 × f_S	Hz
Stop band			0.673 × f_S			Hz
Passband ripple		< 0.328 × f_S			±0.0013	dB
Stop band attenuation		> 0.673 × f_S	−75			dB
DIGITAL FILTER PERFORMANCE[4]						
Group delay time (single, dual)				28/f_S		sec
Group delay time (quad)				19/f_S		sec
De-emphasis error				±0.1		dB
POWER-SUPPLY REQUIREMENTS						
Voltage range	VCCxx1/2		4.5	5.0	5.5	VDC
	VDD1/2		3.0	3.3	3.6	VDC
Supply current	I_{CC}	f_S = 48 kHz/ADC, f_S = 48 kHz/DAC		162	210	mA
		f_S = 96 kHz/ADC, f_S = 192 kHz/DAC		162		mA
		Full power-down[5]		300		µA
	I_{DD}	f_S = 48 kHz/ADC, f_S = 48 kHz/DAC		106	130	mA
		f_S = 96 kHz/ADC, f_S = 192 kHz/DAC		127		mA
		Full power-down[5]		50		µA
Power dissipation		f_S = 48 kHz/ADC, f_S = 48 kHz/DAC		1160	1480	mW
		f_S = 96 kHz/ADC, f_S = 192 kHz/DAC		1230		mW
		f_S = 48 kHz/ADC, Power-down/DAC		660		mW
		Power-down/ADC, f_S = 48 kHz/DAC		633		mW
		Full power-down[5]		1.67		mW

(3) Allowable minimum input resistance of differential to single-ended converter with D to S Gain = G is calculated as (1 + 2G)/(1 + G) × 5k for ac-coupled and (1+ 0.9G)/(1 + G) × 15k for dc-coupled connection, refer to Figure 62 and Figure 63 of the *Application Information* section.
(4) Exclude single and dual at 128 f_S, 192 f_S system clock and quad at 256 f_S to 768 f_S system clock, and specifications for quad, single, and dual are respectively applied in reverse for them.
(5) Halt SCKI, BCKAD, BCKDA, LRCKAD, and LRCKDA.

ELECTRICAL CHARACTERISTICS: DAC Characteristics (continued)

All specifications at T_A = +25°C, VCCAD1 = VCCAD2 = VCCDA1 = VCCDA2 = 5 V, VDD1 = VDD2 = 3.3 V, f_S = 48 kHz, SCKI = 512 f_S, 24-bit data, Sampling Mode = Auto for ADC and DAC, and Interface Mode = Slave for ADC and DAC, unless otherwise noted.

PARAMETER		TEST CONDITIONS	PCM3168A, PCM3168A-Q1			UNIT
			MIN	TYP	MAX	
TEMPERATURE RANGE						
Operating temperature		PCM3168A Consumer grade	−40		+85	°C
		PCM3168A-Q1 Automotive audio grade	−40		+105	°C
Thermal resistance	θ_{JA}	HTQFP-64		+21		°C/W

DEVICE INFORMATION

HTQFP-64 (12 mm x 12 mm)
(10-mm x 10-mm body, 0.5-mm pitch)
(TOP VIEW)

Product Folder Link(s): PCM3168A PCM3168A-Q1
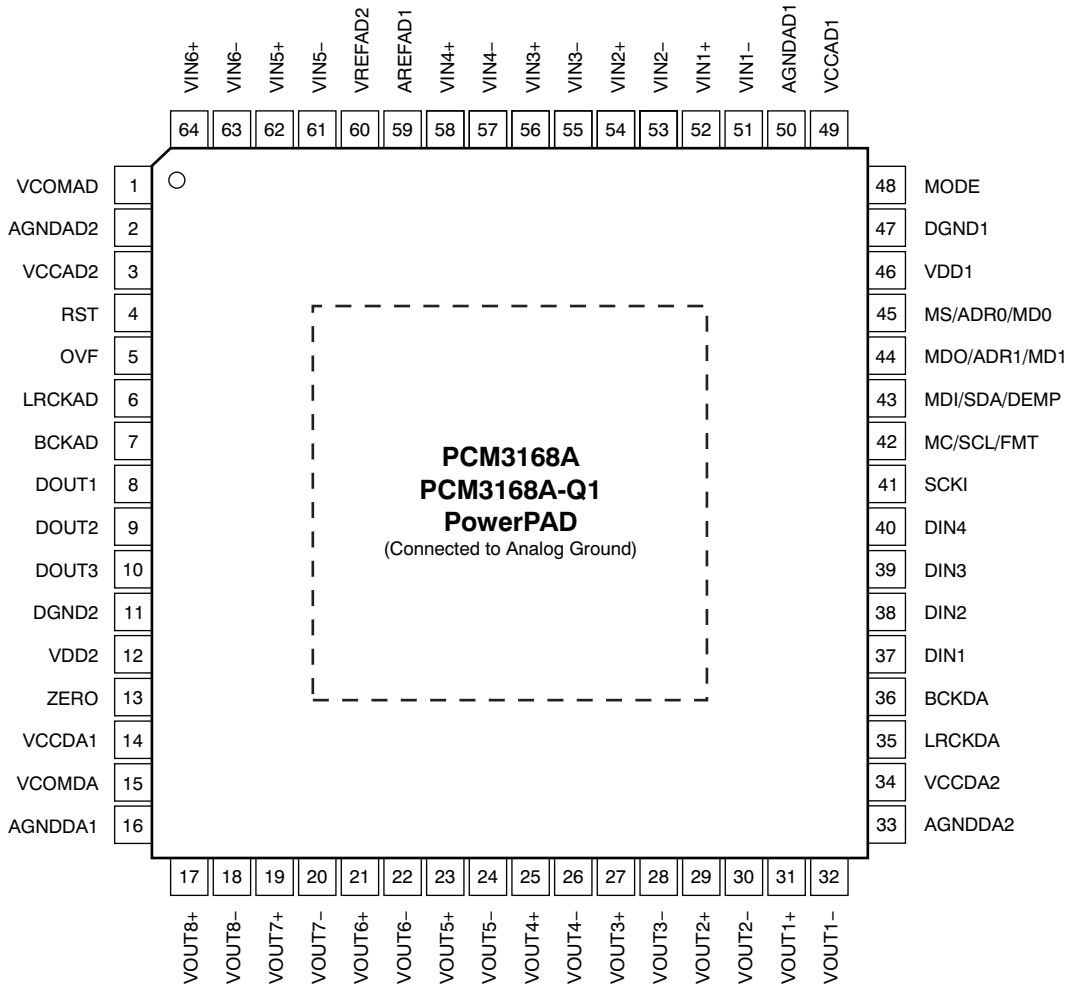
TERMINAL FUNCTIONS

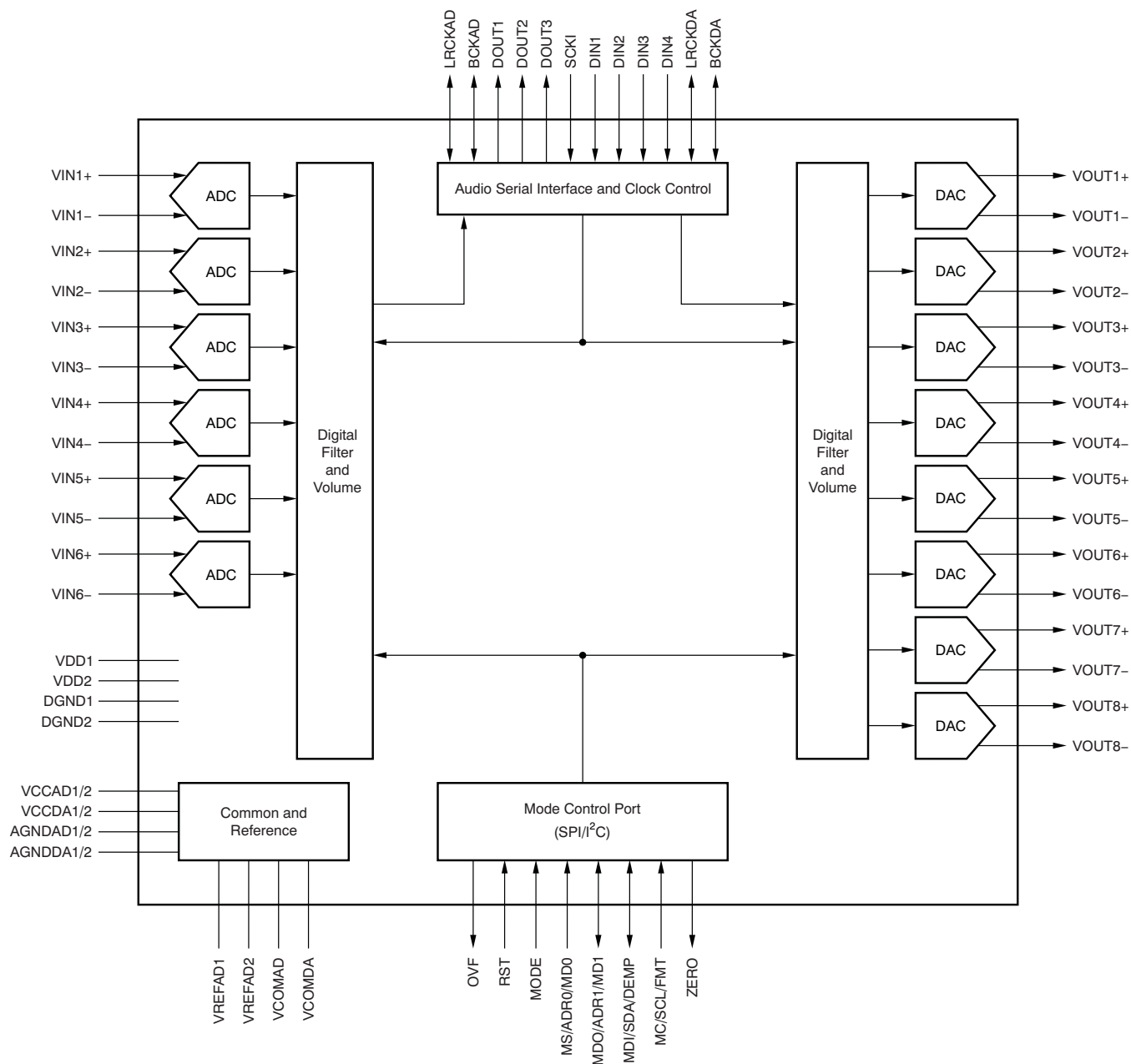| TERMINAL		I/O	PULL-DOWN	5-V TOLERANT	DESCRIPTION
NAME	PIN				
VCOMAD	1	—	No	No	ADC analog common voltage decoupling
AGNDAD2	2	—	No	No	Analog ground 2 for ADC
VCCAD2	3	—	No	No	ADC analog power supply 2, +5 V
RST	4	I	Yes	Yes	Reset and power-down control input with active low
OVF	5	O	No	No	Overflow flag output for ADC
LRCKAD	6	I/O	Yes	No	Audio data word clock input/output for ADC
BCKAD	7	I/O	Yes	No	Audio data bit clock input/output for ADC
DOUT1	8	O	No	No	Audio data digital output for ADC1 and ADC2
DOUT2	9	O	No	No	Audio data digital output for ADC3 and ADC4
DOUT3	10	O	No	No	Audio data digital output for ADC5 and ADC6
DGND2	11	—	No	No	Digital ground 2
VDD2	12	—	No	No	Digital power supply 2, +3.3 V
ZERO	13	O	No	No	Zero detect flag output for DAC
VCCDA1	14	—	No	No	DAC analog power supply 1, +5 V
VCOMDA	15	—	No	No	DAC voltage common decoupling
AGNDDA1	16	—	No	No	Analog ground 1 for DAC
VOUT8+	17	O	No	No	Positive analog output from DAC8
VOUT8−	18	O	No	No	Negative analog output from DAC8
VOUT7+	19	O	No	No	Positive analog output from DAC7
VOUT7−	20	O	No	No	Negative analog output from DAC7
VOUT6+	21	O	No	No	Positive analog output from DAC6
VOUT6−	22	O	No	No	Negative analog output from DAC6
VOUT5+	23	O	No	No	Positive analog output from DAC5
VOUT5−	24	O	No	No	Negative analog output from DAC5
VOUT4+	25	O	No	No	Positive analog output from DAC4
VOUT4−	26	O	No	No	Negative analog output from DAC4
VOUT3+	27	O	No	No	Positive analog output from DAC3
VOUT3−	28	O	No	No	Negative analog output from DAC3
VOUT2+	29	O	No	No	Positive analog output from DAC2
VOUT2−	30	O	No	No	Negative analog output from DAC2
VOUT1+	31	O	No	No	Positive analog output from DAC1
VOUT1−	32	O	No	No	Negative analog output from DAC1
AGNDDA2	33	—	No	No	Analog ground 2 for DAC
VCCDA2	34	—	No	No	DAC analog power supply 2, +5 V
LRCKDA	35	I/O	Yes	No	Audio data word clock input/output for DAC
BCKDA	36	I/O	Yes	No	Audio data bit clock input/output for DAC
DIN1	37	I	No	No	Audio data input for DAC1 and DAC2
DIN2	38	I	No	No	Audio data input for DAC3 and DAC4
DIN3	39	I	No	No	Audio data input for DAC5 and DAC6
DIN4	40	I	No	No	Audio data Input for DAC7 and DAC8
SCKI	41	I	No	Yes	System clock input
MC/SCL/FMT	42	I	No	Yes	Clock for SPI, clock for I^{2}C, format select for hardware control mode
MDI/SDA/DEMP	43	I/O	No	Yes	Input data for SPI, data for I^{2}C[1], de-emphasis control for hardware control mode

(1)   Open-drain configuration in I^{2}C.

TERMINAL FUNCTIONS (continued)

TERMINAL			PULL-DOWN	5-V TOLERANT	DESCRIPTION
NAME	PIN	I/O			
MDO/ADR1/MD1	44	I/O	No	No	Output data for SPI[2], address select 1 for I^{2}C, mode select 1 for hardware control mode
MS/ADR0/MD0	45	I	Yes	Yes	Chip select for SPI, address select 0 for I^{2}C, mode select 0 for hardware control mode
VDD1	46	—	No	No	Digital power supply 1, +3.3 V
DGND1	47	—	No	No	Digital ground 1
MODE	48	I	No	No	Control port mode selection. Tied to VDD: SPI, pull-up: H/W single-ended input, pull-down: H/W and differential input, tied to DGND: I^{2}C
VCCAD1	49	—	No	No	ADC analog power supply 1, +5 V
AGNDAD1	50	—	No	No	Analog ground 1 for ADC
VIN1−	51	I	No	No	Negative analog input to ADC1
VIN1+	52	I	No	No	Positive analog input to ADC1
VIN2−	53	I	No	No	Negative analog input to ADC2
VIN2+	54	I	No	No	Positive analog input to ADC2
VIN3−	55	I	No	No	Negative analog input to ADC3
VIN3+	56	I	No	No	Positive analog input to ADC3
VIN4−	57	I	No	No	Negative analog input to ADC4
VIN4+	58	I	No	No	Positive analog input to ADC4
VREFAD1	59	—	No	No	ADC analog reference voltage 1 decoupling
VREFAD2	60	—	No	No	ADC analog reference voltage 2 decoupling
VIN5−	61	I	No	No	Negative analog input to ADC5
VIN5+	62	I	No	No	Positive analog input to ADC5
VIN6−	63	I	No	No	Negative analog input to ADC6
VIN6+	64	I	No	No	Positive analog input to ADC6

(2)   3-state (Hi-Z) operation in SPI.

Product Folder Link(s): *PCM3168A PCM3168A-Q1*

FUNCTIONAL BLOCK DIAGRAM

PCM3168A
PCM3168A-Q1

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS
ADC Digital Filter

All specifications at T_A = +25°C, VCCAD1 = VCCAD2 = VCCDA1 = VCCDA2 = 5 V, VDD1 = VDD2 = 3.3 V, f_S = 48 kHz, SCKI = 512 f_S, 24-bit data, Sampling Mode = Auto for ADC and DAC, and Interface Mode = Slave for ADC and DAC, unless otherwise noted.
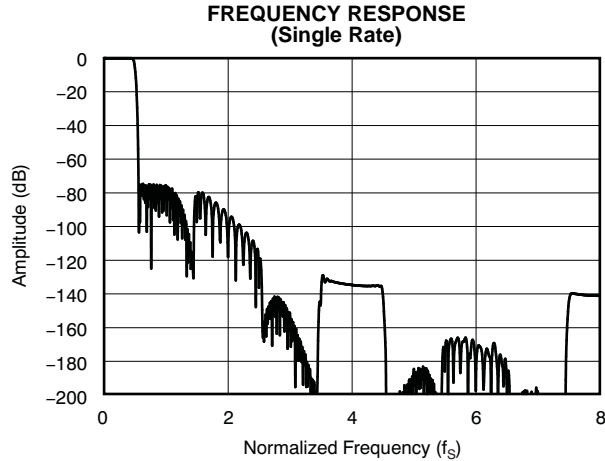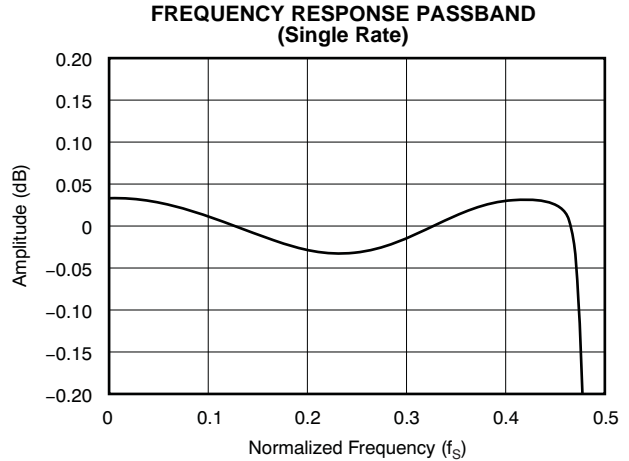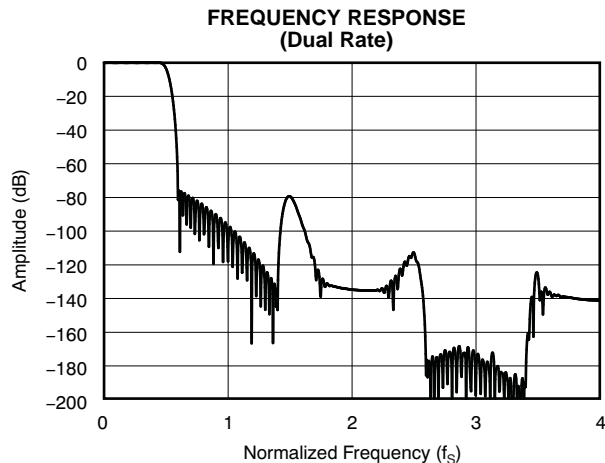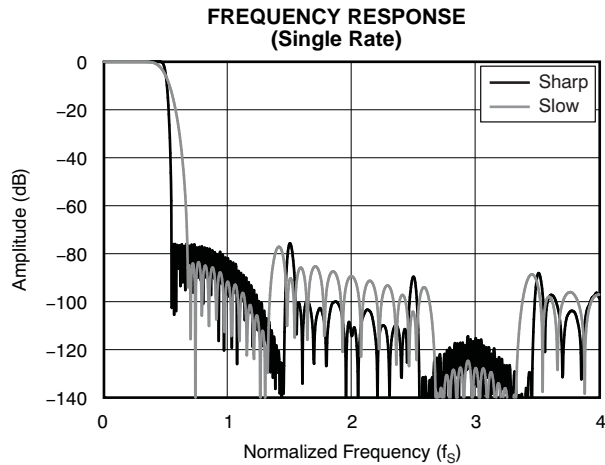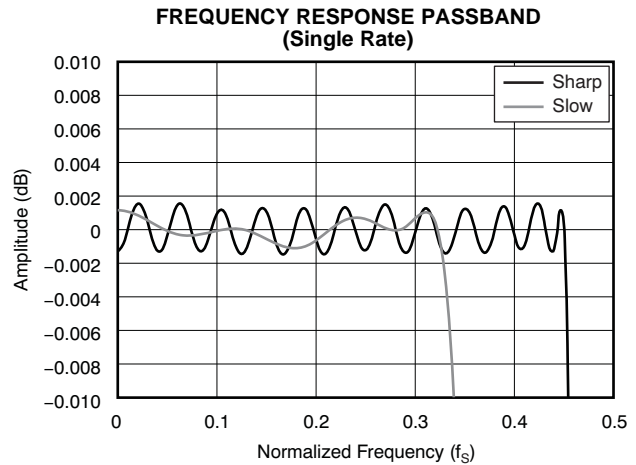
FREQUENCY RESPONSE
(Single Rate)

Figure 1.

FREQUENCY RESPONSE PASSBAND
(Single Rate)

Figure 2.

FREQUENCY RESPONSE
(Dual Rate)

Figure 3.

FREQUENCY RESPONSE PASSBAND
(Dual Rate)

Figure 4.

HPF FREQUENCY RESPONSE

Figure 5.

HPF FREQUENCY RESPONSE PASSBAND

Figure 6.

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Product Folder Link(s): *PCM3168A PCM3168A-Q1*

DAC Digital Filter

All specifications at T_A = +25°C, VCCAD1 = VCCAD2 = VCCDA1 = VCCDA2 = 5 V, VDD1 = VDD2 = 3.3 V, f_S = 48 kHz, SCKI = 512 f_S, 24-bit data, Sampling Mode = Auto for ADC and DAC, and Interface Mode = Slave for ADC and DAC, unless otherwise noted.
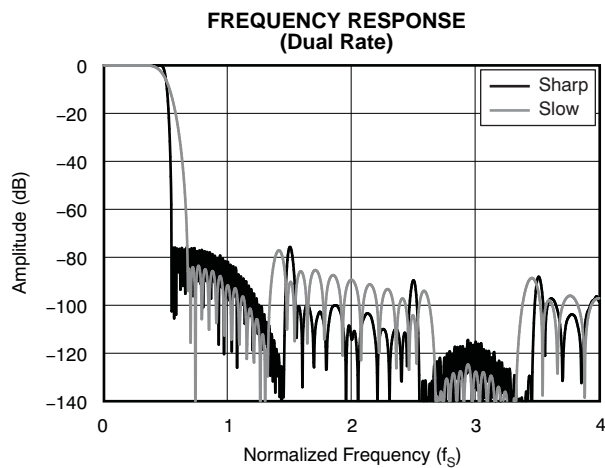
FREQUENCY RESPONSE
(Single Rate)

Figure 7.

FREQUENCY RESPONSE PASSBAND
(Single Rate)

Figure 8.

FREQUENCY RESPONSE
(Dual Rate)

Figure 9.

FREQUENCY RESPONSE PASSBAND
(Dual Rate)

Figure 10.

FREQUENCY RESPONSE
(Quad Rate)

Figure 11.

FREQUENCY RESPONSE PASSBAND
(Quad Rate)

Figure 12.

Product Folder Link(s): *PCM3168A PCM3168A-Q1*
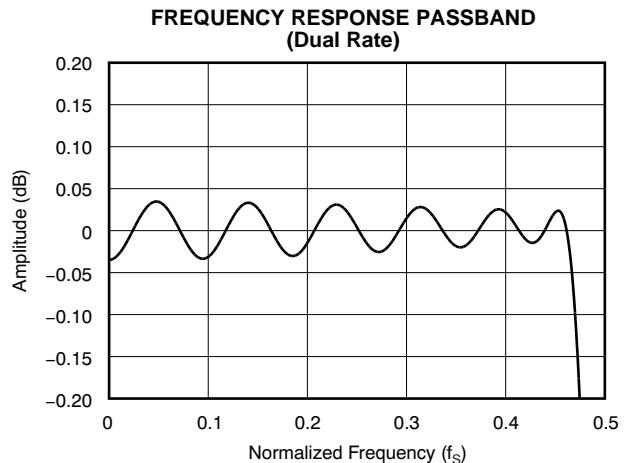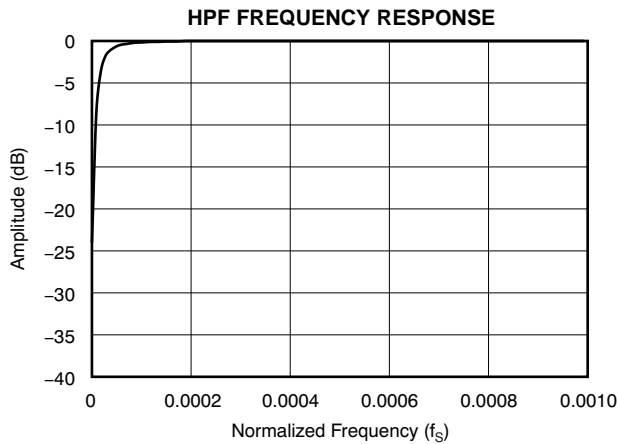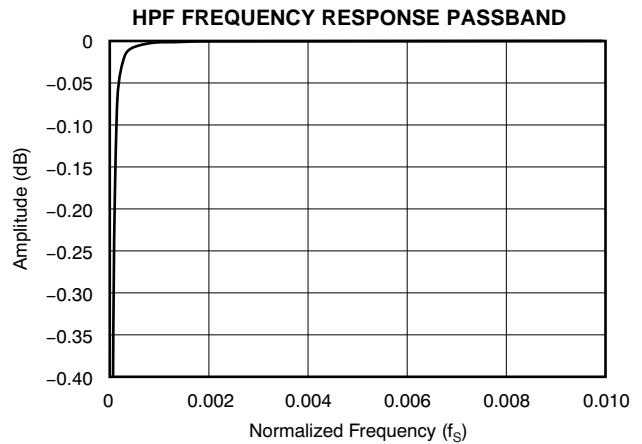
DAC Digital Filter (continued)

All specifications at T_A = +25°C, VCCAD1 = VCCAD2 = VCCDA1 = VCCDA2 = 5 V, VDD1 = VDD2 = 3.3 V, f_S = 48 kHz, SCKI = 512 f_S, 24-bit data, Sampling Mode = Auto for ADC and DAC, and Interface Mode = Slave for ADC and DAC, unless otherwise noted.
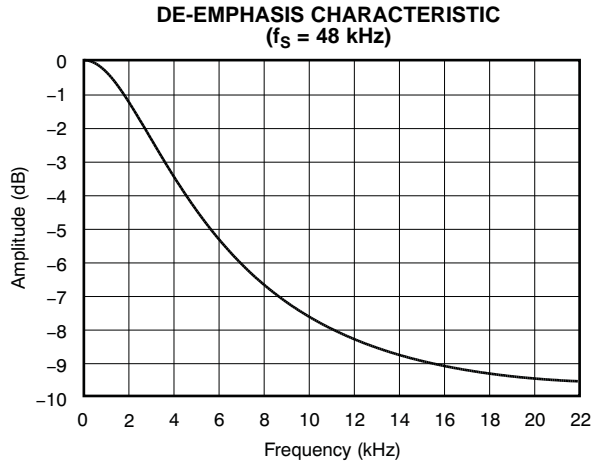

DE-EMPHASIS CHARACTERISTIC
(f_S = 48 kHz)

Figure 13.

DE-EMPHASIS CHARACTERISTIC
(f_S = 44 kHz)

Figure 14.

DE-EMPHASIS CHARACTERISTIC
(f_S = 32 kHz)

Figure 15.

ANALOG FILTER CHARACTERISTIC

Figure 16.

Product Folder Link(s): *PCM3168A PCM3168A-Q1*

ADC Performance

All specifications at T_A = +25°C, VCCAD1 = VCCAD2 = VCCDA1 = VCCDA2 = 5 V, VDD1 = VDD2 = 3.3 V, f_S = 48 kHz, SCKI = 512 f_S, 24-bit data, Sampling Mode = Auto for ADC and DAC, and Interface Mode = Slave for ADC and DAC, unless otherwise noted.
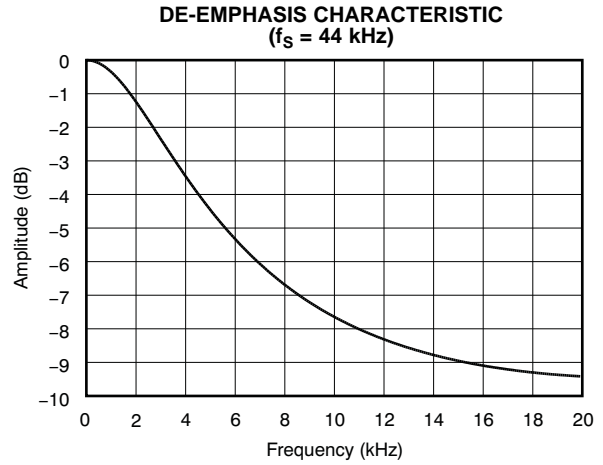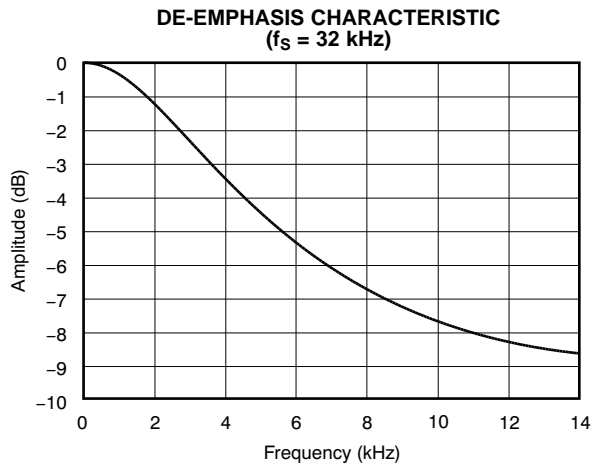
THD+N AT −1 dB
vs TEMPERATURE

Figure 17.

DYNAMIC RANGE AND SNR
vs TEMPERATURE

Figure 18.

THD+N AT −1 dB
vs SUPPLY VOLTAGE

Figure 19.

DYNAMIC RANGE AND SNR
vs SUPPLY VOLTAGE

Figure 20.

Product Folder Link(s): *PCM3168A PCM3168A-Q1*

DAC Performance

All specifications at T_A = +25°C, VCCAD1 = VCCAD2 = VCCDA1 = VCCDA2 = 5 V, VDD1 = VDD2 = 3.3 V, f_S = 48 kHz, SCKI = 512 f_S, 24-bit data, Sampling Mode = Auto for ADC and DAC, and Interface Mode = Slave for ADC and DAC, unless otherwise noted.
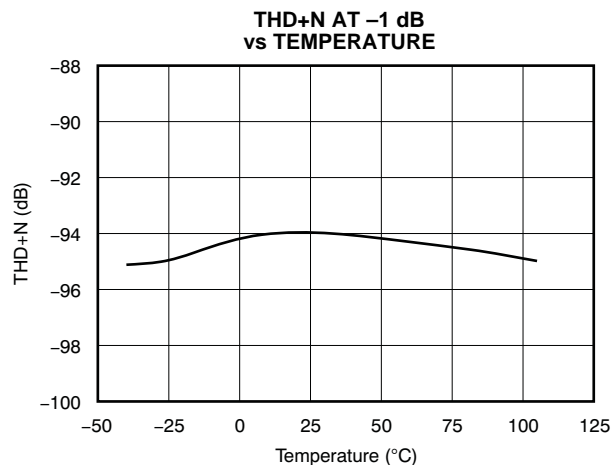
THD+N vs TEMPERATURE
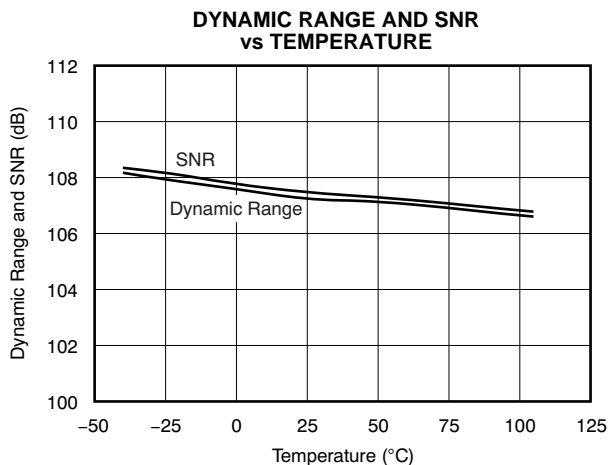
Figure 21.

DYNAMIC RANGE AND SNR
vs TEMPERATURE

Figure 22.

THD+N vs SUPPLY VOLTAGE

Figure 23.

DYNAMIC RANGE AND SNR
vs SUPPLY VOLTAGE

Figure 24.

Product Folder Link(s): *PCM3168A PCM3168A-Q1*

Output Spectrum

All specifications at T_A = +25°C, VCCAD1 = VCCAD2 = VCCDA1 = VCCDA2 = 5 V, VDD1 = VDD2 = 3.3 V, f_S = 48 kHz, SCKI = 512 f_S, 24-bit data, Sampling Mode = Auto for ADC and DAC, and Interface Mode = Slave for ADC and DAC, unless otherwise noted.
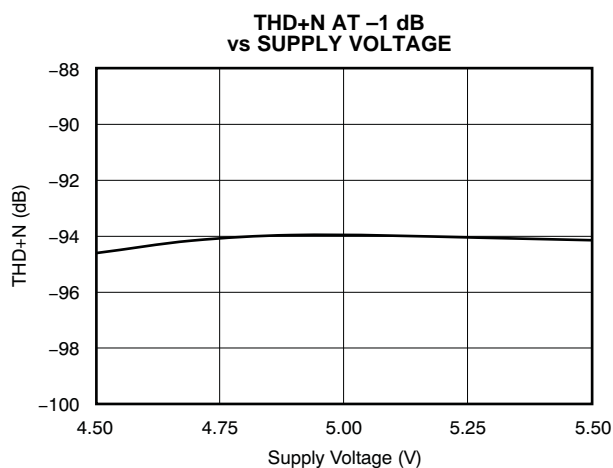
**ADC OUTPUT SPECTRUM
(−1 dB, N = 32,768)**

Figure 25.

**ADC OUTPUT SPECTRUM
(−60 dB, N = 32,768)**

Figure 26.

**DAC OUTPUT SPECTRUM
(0 dB, N = 32,768)**

Figure 27.

**DAC OUTPUT SPECTRUM
(−60 dB, N = 32,768)**

Figure 28.

Product Folder Link(s): *PCM3168A PCM3168A-Q1*

PCM3168A
PCM3168A-Q1

SBAS452−SEPTEMBER 2008

TEXAS
INSTRUMENTS

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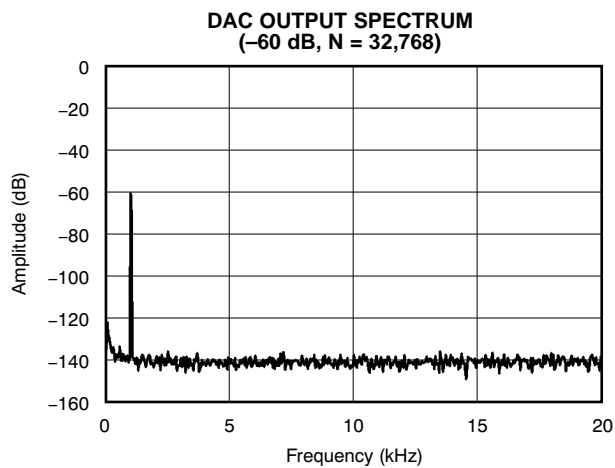
Power-Supply

All specifications at T_A = +25°C, VCCAD1 = VCCAD2 = VCCDA1 = VCCDA2 = 5 V, VDD1 = VDD2 = 3.3 V, f_S = 48 kHz, SCKI = 512 f_S, 24-bit data, Sampling Mode = Auto for ADC and DAC, and Interface Mode = Slave for ADC and DAC, unless otherwise noted.
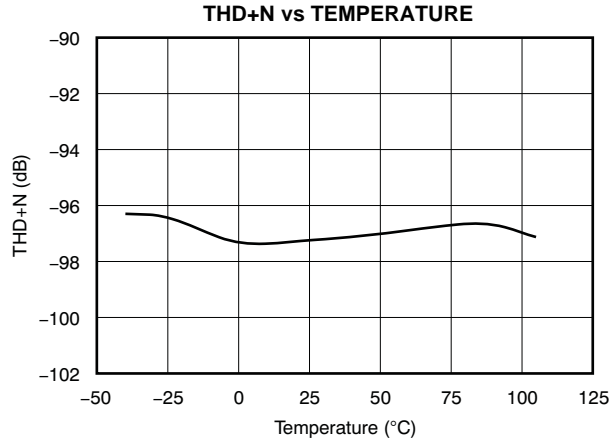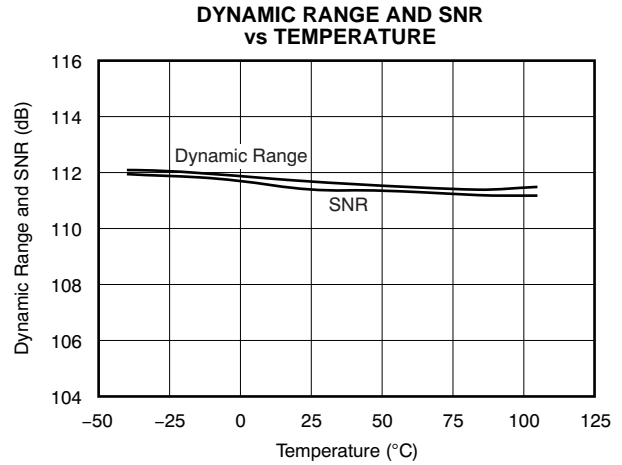
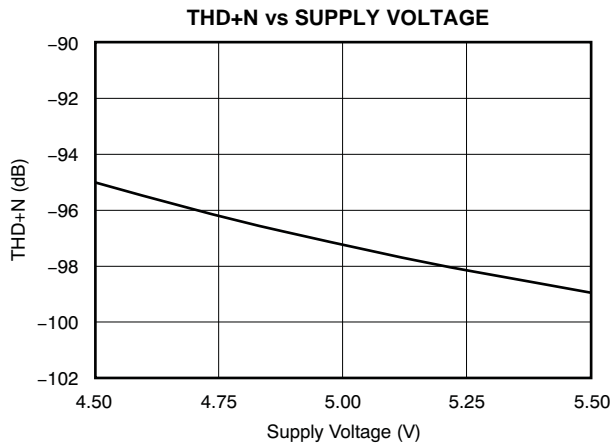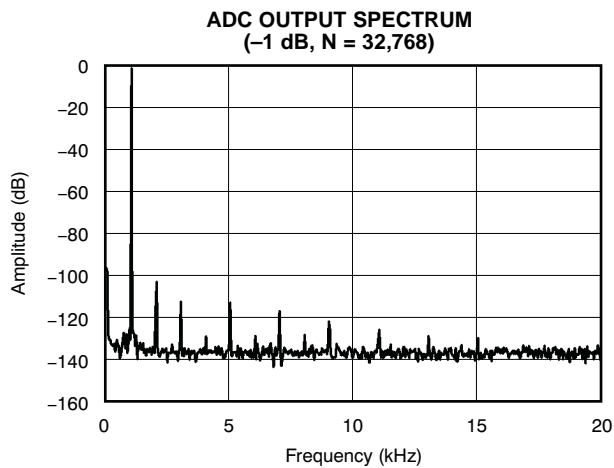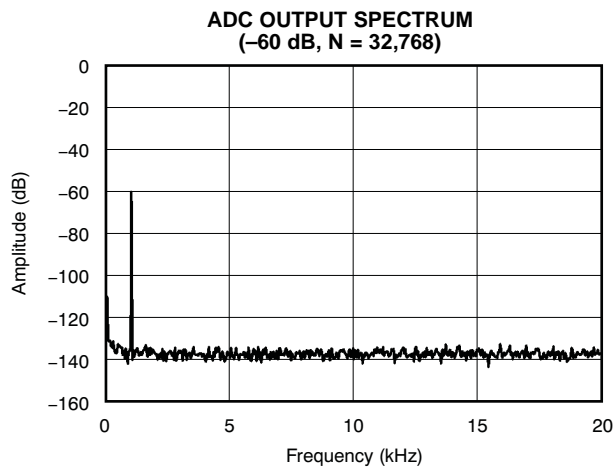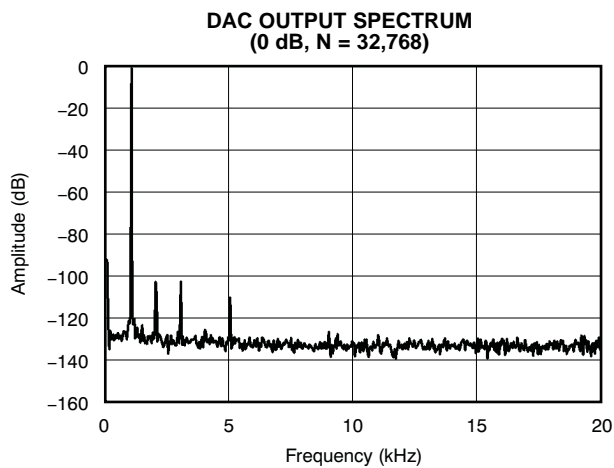**POWER-SUPPLY CURRENT vs POWER-SAVE CONDITION**
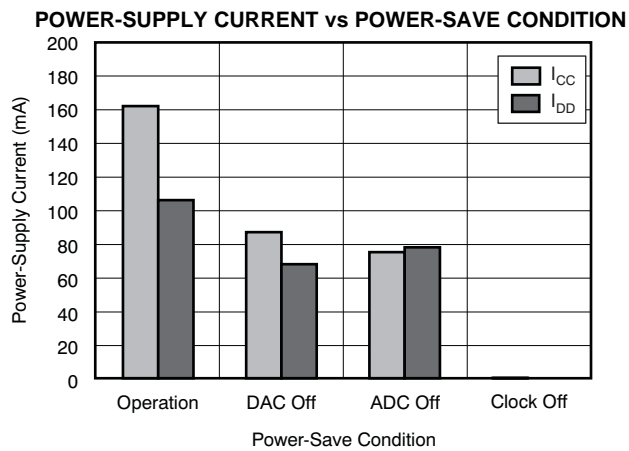
Figure 29.

Product Folder Link(s): *PCM3168A PCM3168A-Q1*

PRODUCT OVERVIEW

The PCM3168A and PCM3168A-Q1 are high-performance, multi-channel codecs targeted for automotive audio applications such as external amplifiers, as well as home multi-channel audio applications (for example, home theaters and A/V receivers). The PCM3168A and PCM3168A-Q1 consist of six-channel analog-to-digital converters (ADCs) and eight-channel digital-to-analog converters (DACs). The ADC input is selectable between single-ended and differential inputs. The DAC output type is fixed with a differential configuration. The PCM3168A and PCM3168A-Q1 support 24-bit linear PCM input and output data in standard audio formats (left-justified, right-justified, and I^{2}S), DSP and TDM formats, and various sample frequencies from 8 kHz to 192 kHz (the ADC configuration supports only up to 96 kHz). The TDM format is useful to save interface bus line numbers for multi-channel audio data communication between the codec and digital audio processor. The PCM3168A and PCM3168A-Q1 offer three modes for device control: two-wire I^{2}C software, four-wire SPI software, and hardware modes.

ANALOG INPUTS

The PCM3168A and PCM3168A-Q1 include six ADCs, each with individual pairs of differential voltage input pins, as shown in Table 1. Additionally, the PCM3168A and PCM3168A-Q1 have the capability of single-ended inputs. The full-scale input voltage is (0.2 × VCCAD1) V$_{RMS}$ at the single-ended input mode and (0.4 × VCCAD1) V$_{RMS}$ at the differential input mode. The input mode is selected by the MODE pin in hardware control mode or by register settings in the software control mode. In single-ended mode, VINx+ pins are used and VINx– pins must be terminated with AGNDAD1/2 via a capacitor or terminated with VCOMAD.

Table 1. Pin Assignments in Differential and Single-Ended Input Modes

CHANNEL	DIFFERENTIAL INPUT MODE	SINGLE-ENDED INPUT MODE
1 (ADC1)	VIN1+, VIN1–	VIN1+
2 (ADC2)	VIN2+, VIN2–	VIN2+
3 (ADC3)	VIN3+, VIN3–	VIN3+
4 (ADC4)	VIN4+, VIN4–	VIN4+
5 (ADC5)	VIN5+, VIN5–	VIN5+
6 (ADC6)	VIN6+, VIN6–	VIN6+

ANALOG OUTPUTS

The PCM3168A and PCM3168A-Q1 include eight DACs, each with individual pairs of differential voltage inputs pins, as shown in Table 2. The full-scale output voltage is (1.6 × VCCDA1) V$_{PP}$ in differential mode. DC-coupled loads are allowed in addition to ac-coupled loads if the load resistance conforms to the specification.

Table 2. Pin Assignments for Differential Output

CHANNEL	DIFFERENTIAL OUTPUT
1 (DAC1)	VOUT1+, VOUT1–
2 (DAC2)	VOUT2+, VOUT2–
3 (DAC3)	VOUT3+, VOUT3–
4 (DAC4)	VOUT4+, VOUT4–
5 (DAC5)	VOUT5+, VOUT5–
6 (DAC6)	VOUT6+, VOUT6–
7 (DAC7)	VOUT7+, VOUT7–
8 (DAC8)	VOUT8+, VOUT8–

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Product Folder Link(s): PCM3168A PCM3168A-Q1

VOLTAGE REFERENCES

The PCM3168A and PCM3168A-Q1 include two internal references for the six-channel ADCs; these references correspond to the outputs VREFAD1 and VREFAD2. Both reference pins should be connected with an analog ground via decoupling capacitors. In addition, the PCM3168A and PCM3168A-Q1 include two pins for common-mode voltage output (VCOMDA for DACs and VCOMAD for ADCs). These pins should be also connected with an analog ground via decoupling capacitors. Furthermore, both common pins can be used to bias external high-impedance circuits, if they are required.

SYSTEM CLOCK INPUT

The PCM3168A and PCM3168A-Q1 require an external system clock input applied at the SCKI input for ADC and DAC operation. The system clock operates at an integer multiple of the sampling frequency, or f_S. The multiples supported in ADC operation include 256 f_S, 384 f_S, 512 f_S, and 768 f_S; the multiples supported in DAC operation include 128 f_S, 192 f_S, 256 f_S, 384 f_S, 512 f_S, and 768 f_S. Details for these system clock multiples are shown in Table 3. Figure 30 and Table 4 show the SCKI timing requirements.

Table 3. System Clock Frequencies for Common Audio Sampling Rates

DEFAULT SAMPLING MODE	SAMPLING FREQUENCY	SYSTEM CLOCK FREQUENCY (MHz)					
	f_S (kHz)	128 f_S[1]	192 f_S[1]	256 f_S	384 f_S	512 f_S	768 f_S
Single rate	8	N/A	N/A	2.0480	3.0720[2]	4.0960	6.1440
	16	2.0480[1]	3.0720[1]	4.0960	6.1440[2]	8.1920	12.2880
	32	4.0960[1]	6.1440[1]	8.1920	12.2880[2]	16.3840	24.5760
	44.1	5.6488[1]	8.4672[1]	11.2896	16.9344[2]	22.5792	33.8688
	48	6.1440[1]	9.2160[1]	12.2880	18.4320[2]	24.5760	36.8640
Dual rate	88.2	11.2896[3]	16.9344[3]	22.5792	33.8688	N/A	N/A
	96	12.2880[3]	18.4320[3]	24.5760	36.8640	N/A	N/A
Quad rate[3]	176.4[3]	22.5792[3]	33.8688[3]	N/A	N/A	N/A	N/A
	192[3]	24.5760[3]	36.8640[3]	N/A	N/A	N/A	N/A

(1) Supported only by DAC operation
(2) Requires 50% duty cycle for stable ADC performance.
(3) Supported only by DAC operation
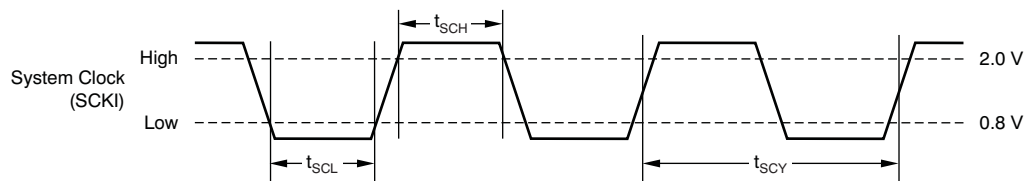
Figure 30. System Clock Timing Requirements

Table 4. Timing Requirements for Figure 30

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{SCY}	System clock pulse cycle time	27		ns
t_{SCH}	System clock pulse width high	10		ns
t_{SCL}	System clock pulse width low	10		ns
t_{DTY}	System clock pulse duty cycle	40	60	%

SAMPLING MODE

The PCM3168A and PCM3168A-Q1 support two sampling modes (single rate and dual rate) in ADC operation, and three sampling modes (single rate, dual rate, and quad rate) in DAC operation. In single rate mode, the ADC and DAC operate at an oversampling frequency of x128 (except when SCKI = 128 f_S and 192 f_S). This mode is supported for sampling frequencies less than 50 kHz. In dual rate mode, the ADC and DAC operate at an

oversampling frequency of x64; this mode is supported for sampling frequencies less than 100 kHz. In quad rate mode, the DAC operates at an oversampling frequency of x32. The sampling mode is automatically selected according to the ratio of system clock frequency and sampling frequency by default (for example, single rate for 512 f_S and 768 f_S, dual rate for 256 f_S and 384 f_S, and quad rate for 128 f_S and 192 f_S), but manual selection is also possible for specified combinations through the serial mode control resistor.

Table 5 and Figure 31 show the relation between the oversampling rate (OSR) of the ΔΣ modulator, noise-free shaped bandwidth, and each sampling mode setting for ADC operation. Table 6 and Figure 32 describe the relation between the oversampling rate of the digital filter and ΔΣ modulator, noise-free shaped bandwidth, and each sampling mode setting for DAC operation.

Table 5. ADC Modulator OSR and Noise-Free Shaped Bandwidthfor Each Sampling Mode

SAMPLING MODE REGISTER SETTING	SYSTEM CLOCK RATE (f_S)	NOISE-FREE SHAPED BANDWIDTH (kHz)		MODULATOR OSR
		f_S = 48 kHz	f_S = 96 kHz	
Auto	512, 768	40	N/A	x128
	256, 384	20	40	x64
Single	512, 768	40	N/A	x128
	256, 384	40	N/A	x128
Dual	256, 384	20	40	x64

Table 6. DAC Digital Filter OSR, Modulator OSR, and Noise-Free Shaped Bandwidth for Each Sampling Mode

SAMPLING MODE REGISTER SETTING	SYSTEM CLOCK RATE (f_S)	NOISE-FREE SHAPED BANDWIDTH			DIGITAL FILTER OSR	MODULATOR OSR
		f_S = 48 kHz	f_S = 96 kHz	f_S = 192 kHz		
Auto	512, 768	40	N/A	N/A	x8	x128
	256, 384	20	40	N/A	x8	x64
	128, 192[1][2]	10	20	40	x4	x32
Single	512, 768	40	N/A	N/A	x8	x128
	256, 384	40	N/A	N/A	x8	x128
	128, 192[1][2]	20	N/A	N/A	x4	x64
Dual	256, 384	20	40	N/A	x8	x64
	128, 192[1][2]	20	40	N/A	x4	x64
Quad	128, 192[1][2]	10	20	40	x4	x32

(1)   Supported only by DAC operation.
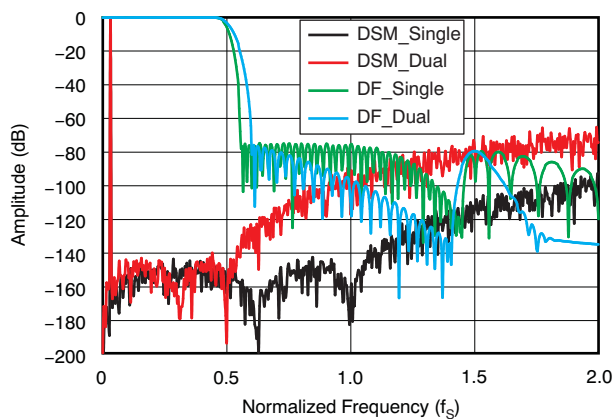(2)   Quad mode filter characteristic is applied.

Figure 31. ADC ΔΣ Modulator and Digital Filter Characteristic

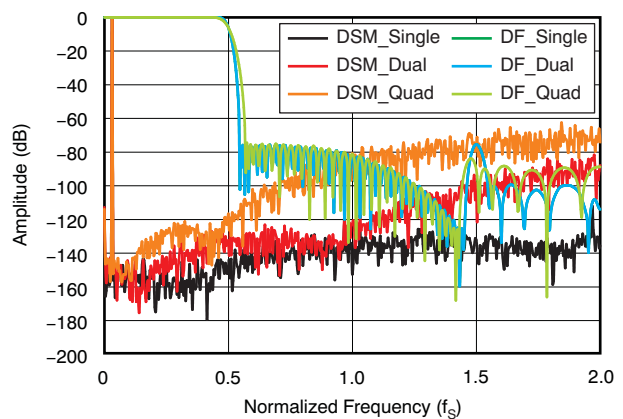Figure 32. DAC ΔΣ Modulator and Digital Filter Characteristic

Product Folder Link(s): PCM3168A PCM3168A-Q1

RESET OPERATION

The PCM3168A and PCM3168A-Q1 have both an internal power-on reset circuit and an external reset circuit. The sequences for both reset circuits are illustrated in Figure 33, Table 7, and Figure 34. Figure 33 and Table 7 describe the timing chart at the internal power-on reset. Initialization is triggered automatically at the point where VDD exceeds 2.2 V typical, and the internal reset is released after 3846 SCKI clock cycles from power-on if RST is kept high and SCKI is provided. VOUT from the DACs are forced to the VCOMDA level initially (= 0.5 × VCCDA1) and settles at a specified level according to the rising VCC. If synchronization among SCKI, BCKAD/DA, and LRCKAD/DA is maintained, VOUT starts to output with a fade-in sequence after $t_{DACDLY1}$ from the internal reset release; VOUT then provides an output that corresponds to DIN after (3846 SCKI + $t_{DACDLY1}$ + $t_{DACDLY2}$) from power-on. Meanwhile, DOUT from the ADCs begins to output with a fade-in sequence after $t_{ADCDLY1}$ from the internal reset release; DOUT then provides output corresponding to VIN after (3846 SCKI + $t_{ADCDLY1}$ + $t_{ADCDLY2}$) from power-on. If the synchronization is not held, the internal reset is not released and both operating modes are maintained at reset and power-down states; after the synchronization forms again, both the DAC and ADC return to normal operation with the above sequences.

Figure 34 illustrates a timing chart at the external reset. RST accepts an external forced reset by RST = low, and provides a device reset and power-down state that makes the lowest power dissipation state available in the PCM3168A and PCM3168A-Q1. If RST goes from high to low under synchronization among SCKI, BCKAD/DA, and LRCKAD/DA, the internal reset is asserted, all registers and memory are reset, and finally the PCM3168A and PCM3168A-Q1 enter into all power-down states. At the same time, VOUT is immediately forced into the AGNDDA1 level and DOUT becomes '0'. To begin normal operation again, toggle RST high; the same power-up sequence as power-on reset shown in Figure 33 is performed.

The PCM3168A and PCM3168A-Q1 do not require particular power-on sequences for VCC and VDD; it allows VDD on and then VCC on, or VCC on and then VDD on. From the viewpoint of the Absolute Maximum Ratings, however, simultaneous power-on is recommended for avoiding unexpected responses on VOUTx and DOUTx. Figure 33 illustrates the response for VCC on with VDD on.
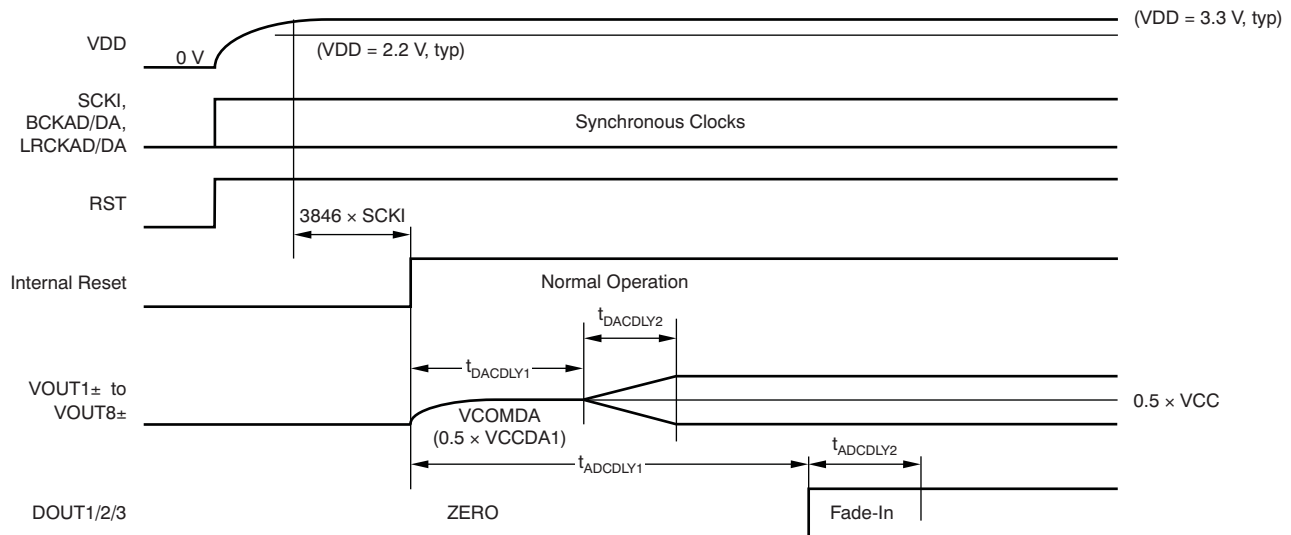
Figure 33. Power-On-Reset Timing Requirements

Table 7. Timing Requirements for Figure 33

SYMBOL	DESCRIPTION	SINGLE	DUAL	QUAD	UNIT
$t_{DACDLY1}$	DAC delay time internal reset release to VOUT start	3600	7200	14400	Period of LRCKDA
$t_{DACDLY2}$	DAC fade-in/fade-out time	2048	4096	8192	Period of LRCKDA
$t_{ADCDLY1}$	ADC delay time internal reset release to DOUT start	4800	9600	N/A	Period of LRCKAD
$t_{ADCDLY2}$	ADC fade-in/fade-out time	2048	4096	N/A	Period of LRCKAD

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Product Folder Link(s): *PCM3168A PCM3168A-Q1*
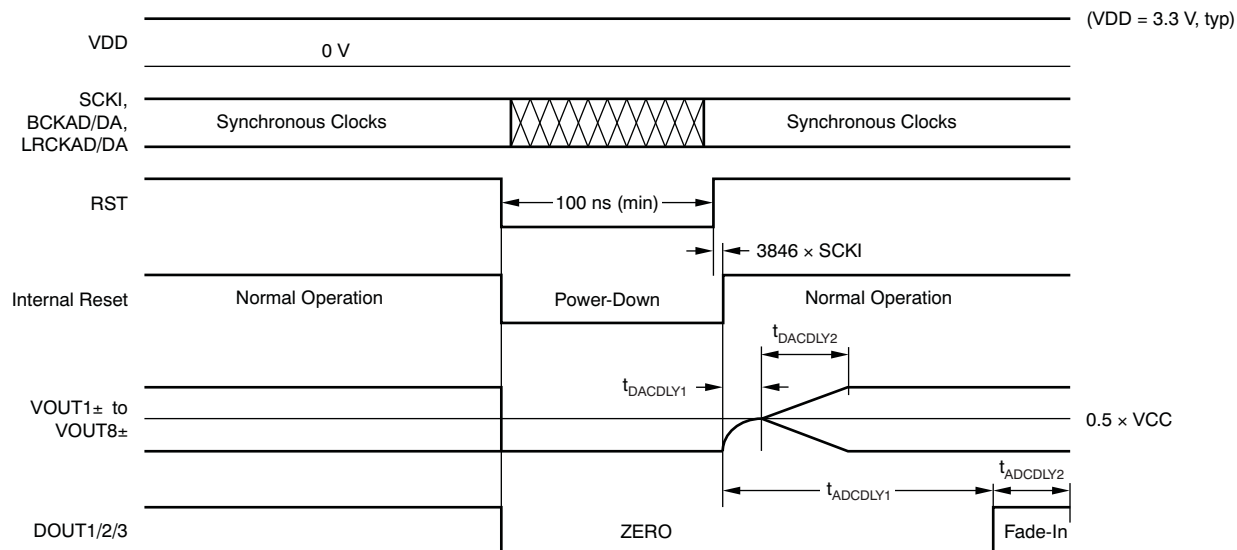
Figure 34. External Reset Timing Requirements

AUDIO SERIAL PORT OPERATION

The PCM3168A and PCM3168A-Q1 audio serial ports consist of 11 signals: BCKDA, BCKAD, LRCKDA, LRCKAD, DIN1, DIN2, DIN3, DIN4, DOUT1, DOUT2, and DOUT3. The PCM3168A and PCM3168A-Q1 also support audio interface mode, slave mode, and master mode. The BCKAD/DA is a bit clock input at the slave mode and an output at the master mode. The LRCKAD/DA is a left/right word clock or frame synchronization clock input at slave mode and output at master mode. The DIN1/2/3/4 are the audio data inputs for the DAC. The DOUT1/2/3 are the audio data outputs from the ADC. BCKAD, LRCKAD and DOUT1/2/3 are used for the ADC, and BCKDA, LRCKDA and DIN1/2/3/4 are used for the DAC.

AUDIO DATA INTERFACE FORMATS AND TIMING

The PCM3168A and PCM3168A-Q1 support eight audio data interface formats for the ADC and DAC separately in both master and slave modes: 24-bit I^{2}S, 24-bit left-justified, 24-bit right-justified, 16-bit right-justified, 24-bit left-justified mode DSP, 24-bit I^{2}S mode DSP, 24-bit left-justified mode TDM, and 24-bit I^{2}S mode TDM format. The PCM3168A and PCM3168A-Q1 also support two audio data interface formats for the DAC and slave mode: 24-bit left-justified mode high-speed TDM and 24-bit I^{2}S mode high-speed TDM format. In the case of I^{2}S, left-justified, and right-justified data formats, 64 BCKs, 48 BCKs, and 32 BCKs per LRCK period are supported, but 48 BCKs are limited in slave mode and 32 BCKs are limited in slave mode 16-bit right-justified only. In the case of TDM data format in single rate, BCKAD/DA, LRCKAD/DA, DOUT1, and DIN1 are used. In the case of TDM data format in dual rate, BCKAD/DA, LRCKAD/DA, DOUT1/2, and DIN1/2 are used. In the case of high-speed TDM format in dual rate, BCKDA, LRCKDA, and DIN1 are used. In the case of high-speed TDM format in quad rate, BCKDA, LRCKDA, and DIN1/2 are used. TDM format and high-speed TDM format are supported only at SCKI = 512 f$_S$, 256 f$_S$, 128 f$_S$, and f$_{BCK}$ ≤ f$_{SCKI}$. The audio data formats are selected by MC/SCL/FMT in hardware control mode and registers 65 and 81 in software control mode. All data must be in binary twos complement, MSB first.

Figure 35 through Figure 41 show 10 audio interface data formats. Table 8 summarizes the applicable formats and describes the relationships among them and the respective restrictions with mode control.

Table 8. Audio Data Interface Formats and Sampling Rate, Bit Clock, and System Clock Restrictions

CONTROL MODE	FORMAT	I/F MODE	DATA BITS	MAX LRCK FREQUENCY (f_S)	SCKI RATE (xf_S)	BCK RATE (xf_S)	APPLICABLE PINS
Software control	I²S/Left-Justified	Master/Slave	24	96 kHz (ADC) 192 kHz (DAC)	256 to 768 (ADC) 128 to 768 (DAC)	64, 48 (slave)[1]	DOUT1/2/3 DIN1/2/3/4
	Right-Justified		24, 16			64, 48 (slave)[1] 32 (slave, 16 bit)[1]	
	I²S/Left-Justified DSP		24			64	
	I²S/ Left-Justified TDM		24	48 kHz	256, 512	256	DOUT1, DIN1
			24	96 kHz	128 (DAC)[2], 256	128	DOUT1/2, DIN1/2
	High-Speed I²S/Left-Justified TDM	Slave and DAC Only[3]	24	96 kHz	256	256	DIN1
			24	192 kHz	128	128	DIN1/2
Hardware control	I²S	Master (ADC), Slave	24	96 kHz (ADC) 192 kHz (DAC)	256 to 768 (ADC) 128 to 768 (DAC)	64, 48 (slave)[1]	DOUT1/2/3 DIN1/2/3/4
	I²S TDM		24	48 kHz	512	256	DOUT1, DIN1
			24	96 kHz	256	128	DOUT1/2, DIN1/2

(1)   BCK = 48 f_S, 32 f_S is supported only in slave mode; BCK = 32 f_S is supported only for 16-bit data length.
(2)   SCKI = 128 f_S is supported only for DAC.
(3)   High-Speed I²S/Left-Justified TDM format is supported only for DAC operation in slave mode.

Figure 35. Audio Data Format: 24-Bit I²S
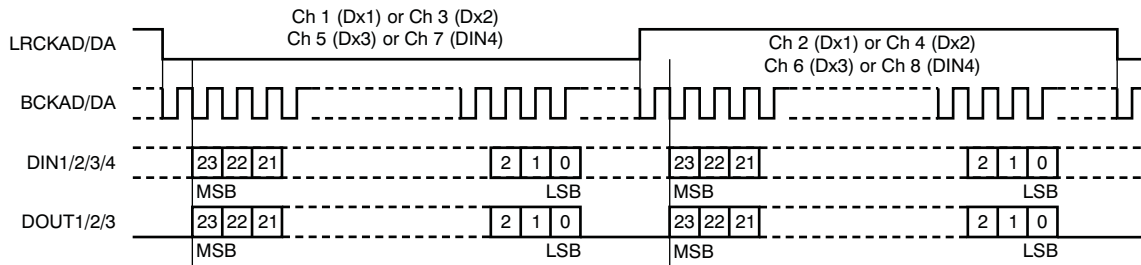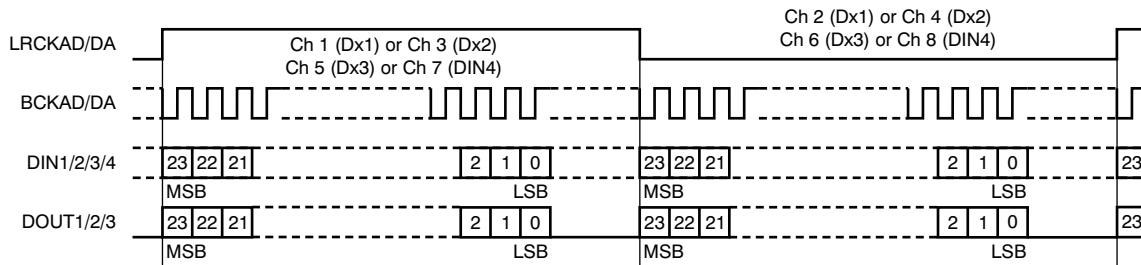

Figure 36. Audio Data Format: 24-Bit Left-Justified
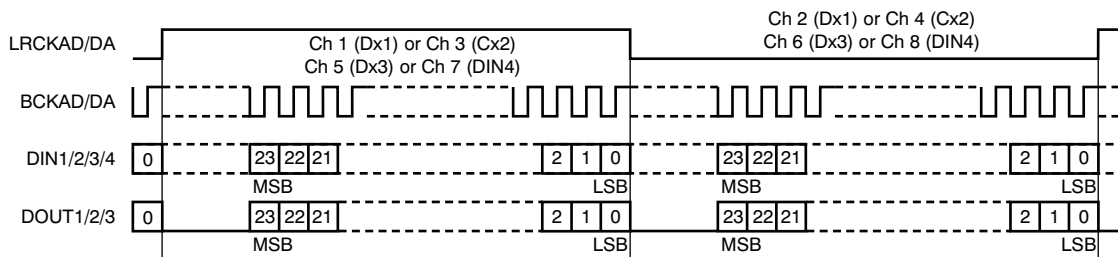
Figure 37. Audio Data Format: 24-Bit Right-Justified
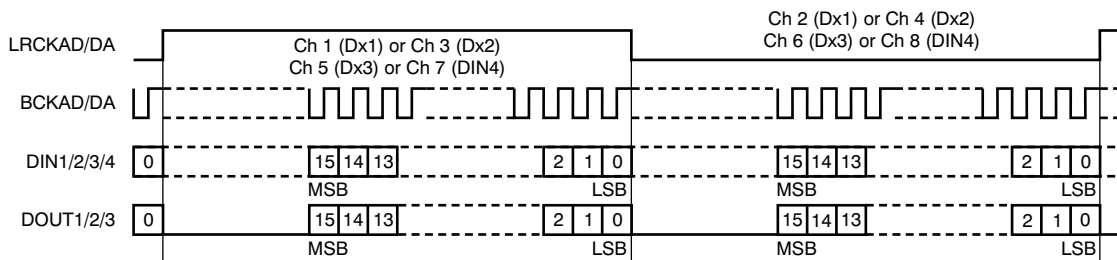
Figure 38. Audio Data Format: 16-Bit Right-Justified
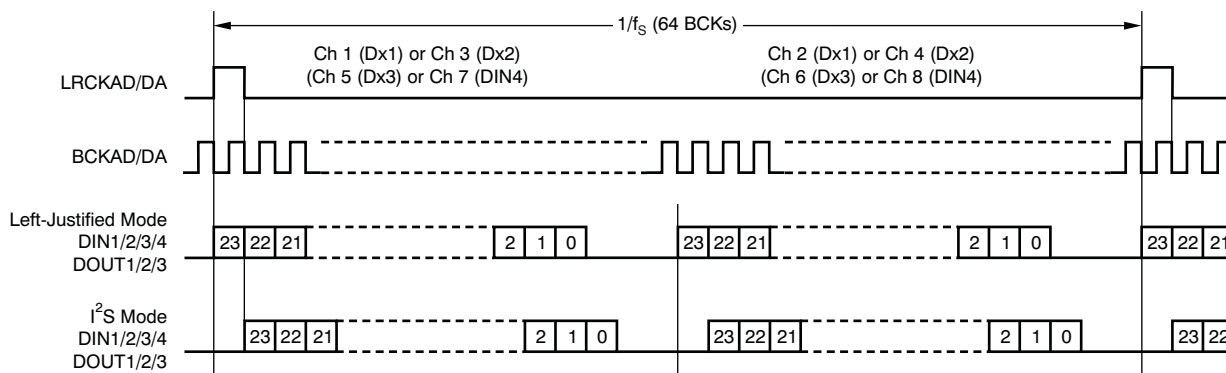
Figure 39. Audio Data Format: 24-Bit DSP Format
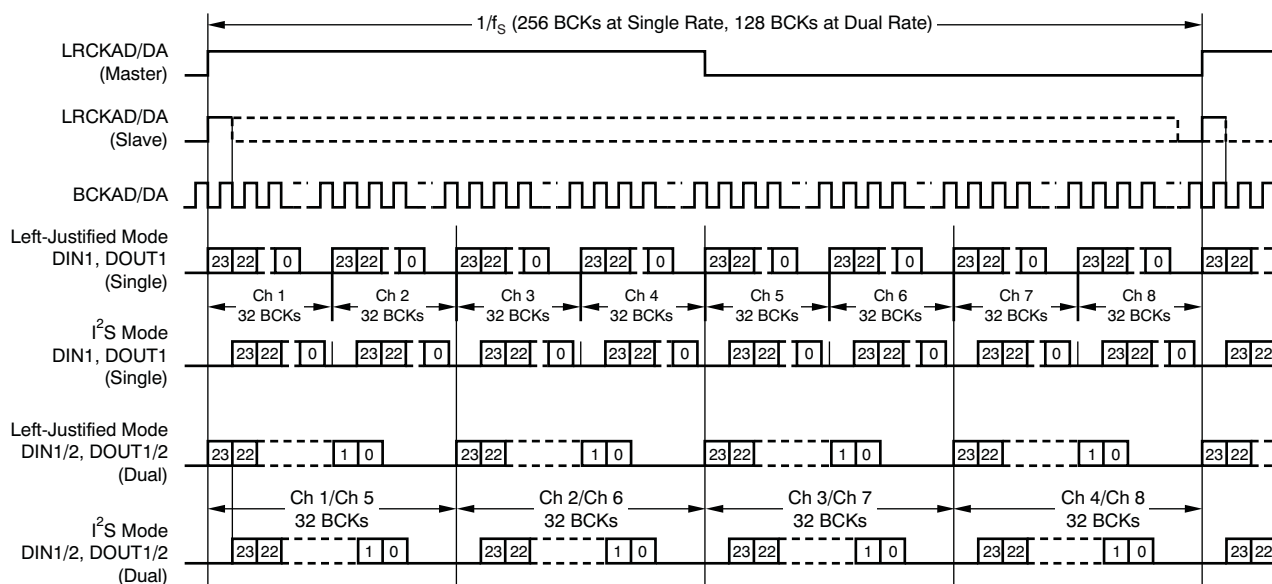
Figure 40. Audio Data Format: 24-Bit TDM Format (SCKI = 128 f_S, 256 f_S, and 512 f_S Only)

Product Folder Link(s): *PCM3168A PCM3168A-Q1*
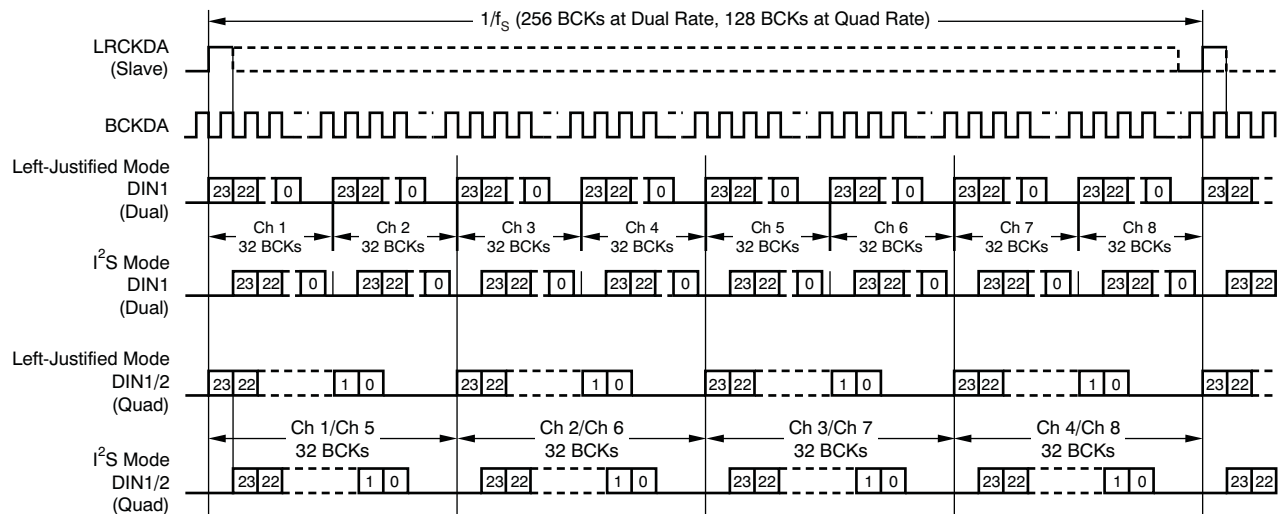
Figure 41. Audio Data Format: 24-Bit High-Speed TDM Format
(SCKI = 128 f_S, 256 f_S, DAC, and Slave Mode Only)

AUDIO INTERFACE TIMING

Figure 42 through Figure 45 describe the detailed interface timing specifications.
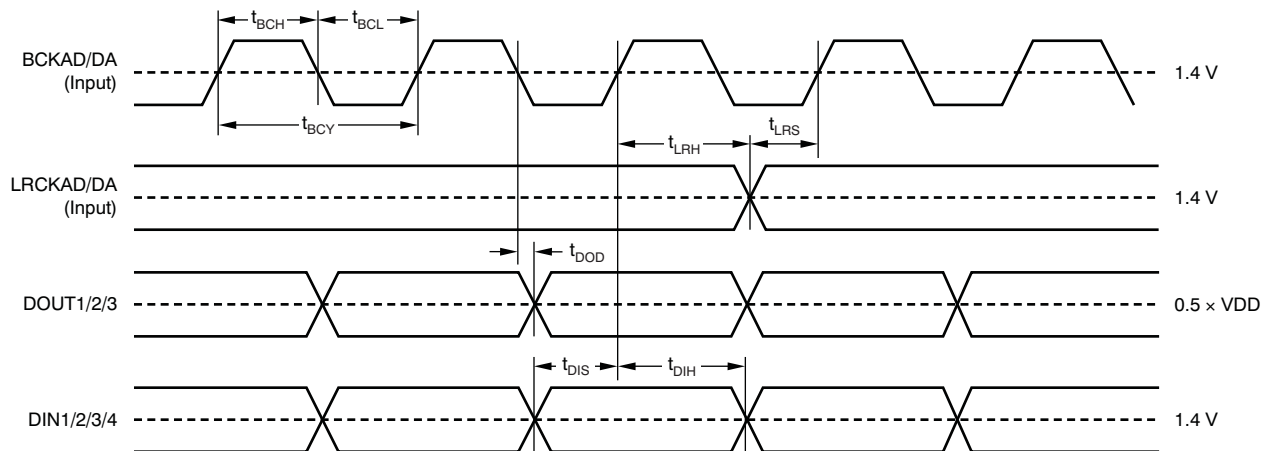
Figure 42. Audio Interface Timing Requirements for Left-Justified, Right-Justified, and I²S Data Formats
(Slave Mode)

Table 9. Timing Requirements for Figure 42[1]

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{BCY}	BCKAD/DA cycle time	75			ns
t_{BCH}	BCKAD/DA pulse width high	35			ns
t_{BCL}	BCKAD/DA pulse width low	35			ns
t_{LRS}	LRCKAD/DA setup time to BCKAD/DA rising edge	10			ns
t_{LRH}	LRCKAD/DA hold time to BCKAD/DA rising edge	10			ns
t_{DIS}	DIN1/2/3/4 setup time to BCKDA rising edge	10			ns
t_{DIH}	DIN1/2/3/4 hold time to BCKDA rising edge	10			ns
t_{DOD}	DOUT1/2/3 delay time from BCKAD falling edge	0		30	ns

(1)   Load capacitance of output is 20 pF.

Figure 43. Audio Interface Timing Requirements for Left-Justified, Right-Justified, and I²S Data Formats (Master Mode)

Timing Requirements for Figure 43[1]

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{BCY}	BCKAD/DA cycle time		$1/(64\ f_S)$		
t_{BCH}	BCKAD/DA pulse width high	$0.4\ t_{BCY}$	$0.5\ t_{BCY}$	$0.6\ t_{BCY}$	
t_{BCL}	BCKAD/DA pulse width low	$0.4\ t_{BCY}$	$0.5\ t_{BCY}$	$0.6\ t_{BCY}$	
t_{LRD}	LRCKAD/DA delay time from BCKAD/DA falling edge	−10		20	ns
t_{DIS}	DIN1/2/3/4 setup time to BCKDA rising edge	10			ns
t_{DIH}	DIN1/2/3/4 hold time to BCKDA rising edge	10			ns
t_{DOD}	DOUT1/2/3 delay time from BCKAD falling edge	−10		20	ns

(1) Load capacitance of output is 20 pF.

Figure 44. Audio Interface Timing Requirements for DSP and TDM Data Formats (Slave Mode)

Product Folder Link(s): *PCM3168A PCM3168A-Q1*

Timing Requirements for Figure 44[1]

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{BCY}	BCKAD cycle time	75			ns
	BCKDA cycle time	40			ns
t_{BCH}	BCKAD pulse width high	35			ns
	BCKDA pulse width high	15			ns
t_{BCL}	BCKAD pulse width low	35			ns
	BCKDA pulse width low	15			ns
t_{LRW}	LRCKAD/DA pulse width high (DSP format)	t_{BCY}			
	LRCKAD/DA pulse width high (TDM format)	t_{BCY}		$1/f_S - t_{BCY}$	
t_{LRS}	LRCKAD/DA setup time to BCKAD/DA rising edge	10			ns
t_{LRH}	LRCKAD/DA hold time to BCKAD/DA rising edge	10			ns
t_{DIS}	DIN1/2/3/4 setup time to BCKDA rising edge	10			ns
t_{DIH}	DIN1/2/3/4 hold time to BCKDA rising edge	10			ns
t_{DOD}	DOUT1/2/3 delay time from BCKAD falling edge	0		30	ns

(1) Load capacitance of output is 20 pF.
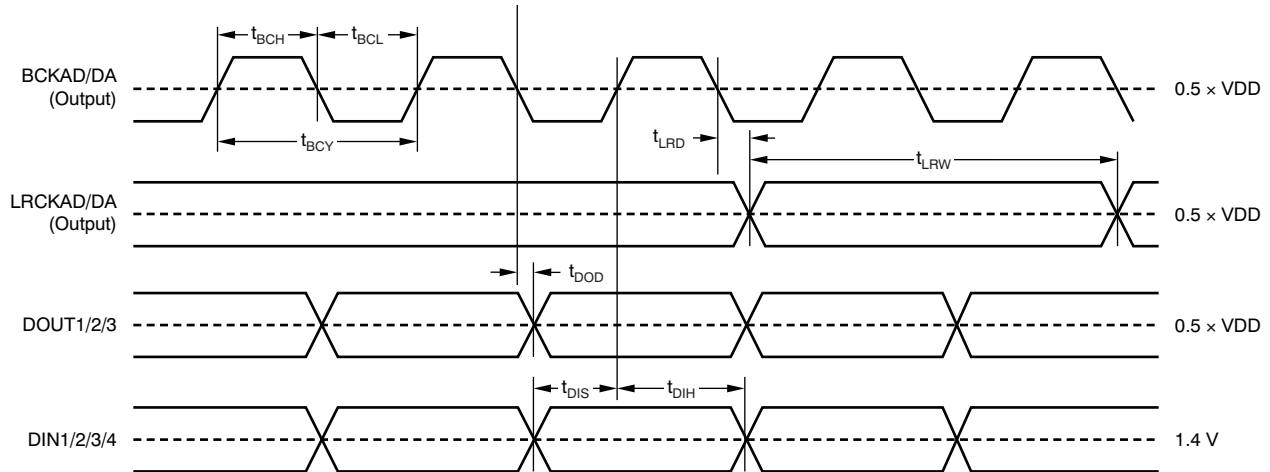
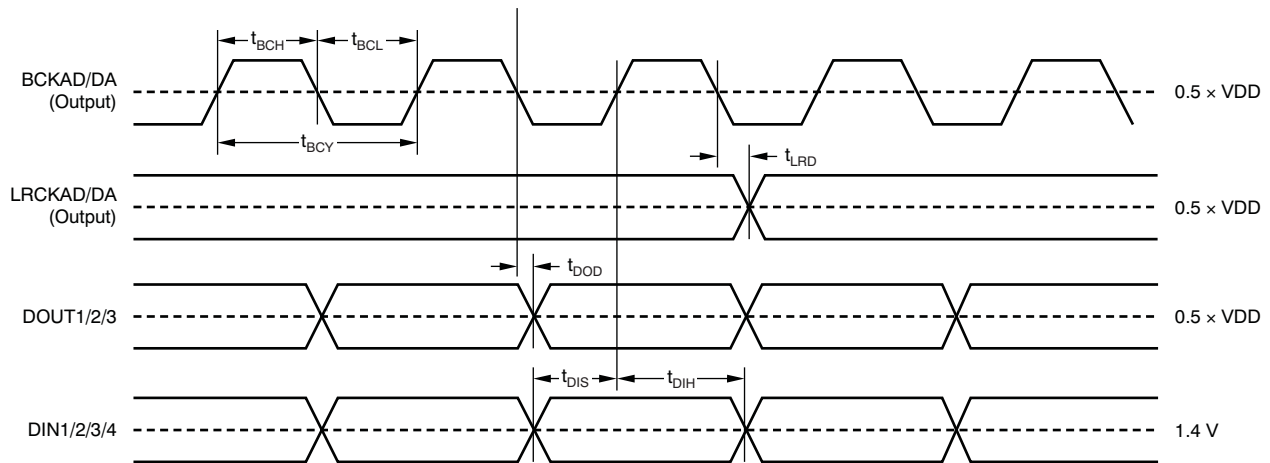**Figure 45. Audio Interface Timing Requirements for DSP and TDM Data Formats (Master Mode)**

Timing Requirements for Figure 45[1]

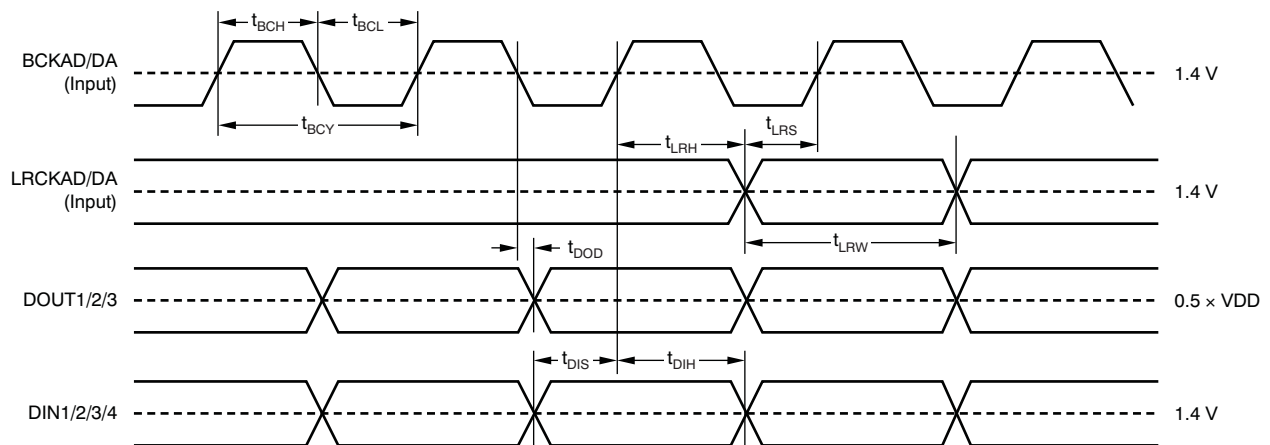| SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{BCY}	BCKAD/DA cycle time (DSP format)		$1/(64\ f_S)$		
	BCKAD/DA cycle time (TDM format, single rate)		$1/(256\ f_S)$		
	BCKAD/DA cycle time (TDM format, dual rate)		$1/(128\ f_S)$		
t_{BCH}	BCKAD/DA pulse width high	$0.4\ t_{BCY}$	$0.5\ t_{BCY}$	$0.6\ t_{BCY}$	
t_{BCL}	BCKAD/DA pulse width low	$0.4\ t_{BCY}$	$0.5\ t_{BCY}$	$0.6\ t_{BCY}$	
t_{LRW}	LRCKAD/DA pulse width high (DSP format)		t_{BCY}		
	LRCKAD/DA pulse width high (TDM format)		$1/(2\ f_S)$		
t_{LRD}	LRCKAD/DA delay time from BCKAD/DA falling edge	−10		20	ns
t_{DIS}	DIN1/2/3/4 setup time to BCKDA rising edge	10			ns
t_{DIH}	DIN1/2/3/4 hold time to BCKDA rising edge	10			ns
t_{DOD}	DOUT1/2/3 delay time from BCKAD falling edge	−10		20	ns

(1) Load capacitance of output is 20 pF.

SYNCHRONIZATION WITH THE DIGITAL AUDIO SYSTEM

The PCM3168A and PCM3168A-Q1 operate under the system clock (SCKI) and the audio sampling rate (LRCKAD/DA). Therefore, SCKI and LRCKAD/DA must have a specific relationship in slave mode. The PCM3168A and PCM3168A-Q1 do not need a specific phase relationship between the audio interface clocks (LRCKAD/DA, BCKAD/DA) and the system clock (SCKI), but does require a specific frequency relationship (ratiometric) between LRCKAD/DA, BCKAD/DA, and SCKI.

If the relationship between SCKI and LRCKDA changes more than ±2 BCKDA clocks because of jitter, sampling frequency change, etc., the DAC internal operation halts within $1/f_S$, and the analog output is forced into VCOMDA (0.5 VCCDA1) until re-synchronization between SCKI, LRCKDA, and BCKDA is completed and then $t_{DACDLY3}$ passes. If the relationship between SCKI and LRCKAD changes more than ±2 BCKADs because of jitter, sampling frequency change, etc., the ADC internal operation halts within $1/f_S$, and the digital output is forced into a '0' code until re-synchronization between SCKI, LRCKAD, and BCKAD is completed and then $t_{ADCDLY3}$ passes. In the event the change is less than ±2 BCKAD/DAs, re-synchronization does not occur, and this analog/digital output control and discontinuity do not occur.

Figure 46 shows the DAC analog output and ADC digital output for loss of synchronization. During undefined data periods, some noise may be generated in the audio signal. Also, the transition of normal to undefined data and undefined (or zero) data to normal data creates a discontinuity of data on the analog and digital outputs, which then may generate some noise in the audio signal.

Both ADC outputs (DOUTx) and DAC outputs (VOUTx) hold the previous state if the system clock halts, but the asynchronous and re-synchronization processes would occur after the system clock resumes. Figure 46 shows DAC outputs and ADC outputs for loss of synchronization.
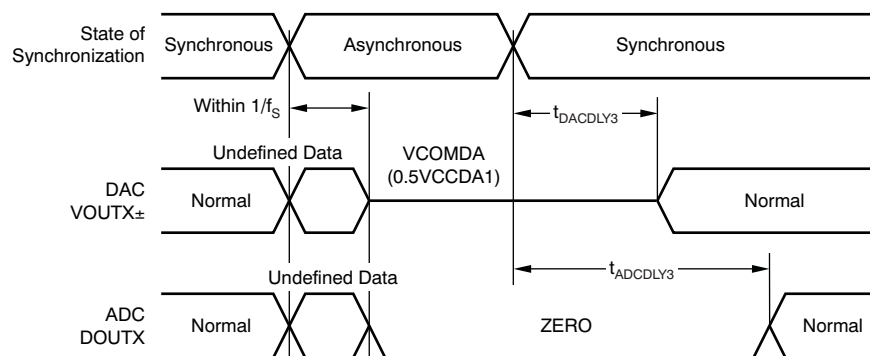
Figure 46. DAC Outputs and ADC Outputs for Loss of Synchronization

Timing Requirements for Figure 46

SYMBOL	DESCRIPTION	SINGLE	DUAL	QUAD	UNIT
$t_{DACDLY3}$	DAC delay synchronization detect to normal data	38	38	29	Period of LRCKDA
$t_{ADCDLY3}$	ADC delay synchronization detect to normal data	60	60	N/A	Period of LRCKAD

HIGH-PASS FILTER (HPF)

The PCM3168A and PCM3168A-Q1 include a high-pass filter (HPF) for all ADC channels in order to remove the dc component of the digitized input signal. The filter is located at the output of the digital decimation filter. The −3 dB corner frequency for the HPF scales with the output sampling rate, where $f_{-3\ dB} = 0.020 \times f_S/1000$. When $f_S = 48$ kHz, $f_{-3\ dB}$ is 0.96 Hz. The HPF function can be disabled (bypassed) by the BYP bits in two channels.

OVERFLOW FLAG

The PCM3168A and PCM3168A-Q1 include an overflow flag output for all ADC channels. As soon as any of the six-channel ADC digital outputs exceed the full-scale range, an overflow flag is forced high on the OVF pin. The overflow flag is held high for 1024 LRCKAD clock cycles. In parallel, overflow flag information is stored in the OVF bits of the mode control register, and the OVF bit is held until the mode control register is read. The overflow flag polarity can be changed by the OVFP bit. The OVF pin also indicates internal reset completion by transmitting a 4096 SCKI width pulse.

ZERO FLAG

The PCM3168A and PCM3168A-Q1 include a zero flag output for all DAC channels. When all of the eight-channel DACs digital inputs have continued as zero data for 1024 LRCKDA clock cycles, the zero flag is forced high on ZERO. In parallel, zero flag information is stored in the ZERO bits according to channel. The zero flag polarity can be changed by the ZREV bit. Also, the zero flag function can be selected by the AZRO bits. AND or OR logic for stereo, six channels, and eight channels can be selected.

MODE CONTROL

The PCM3168A and PCM3168A-Q1 include four-way mode control selectable by MODE pin, as shown in Table 10. The pull-up and pull-down resistors must be 220 kΩ ±5%. This mode control selection is sampled only when the internal reset is released by a power-on reset or by a low-to-high transition of the external reset (RST pin); a system clock is also required.

Table 10. Mode Control Selection

MODE	MODE CONTROL INTERFACE
Tied to DGND	Two-wire (I^{2}C) serial control, selectable analog input configuration
Tied to DGND via pull-down resistor	H/W (hardware control), differential analog input
Tied to VDD via pull-up resistor	H/W (hardware control), single-ended analog input
Tied to VDD	Four-wire (SPI) serial control, selectable analog input configuration

From the mode control selection described in Table 10, the functions of four pins are changed, as shown in Table 11.

Table 11. Pin Functions

PIN	PIN ASSIGNMENTS		
	SPI	I^{2}C	H/W
MS/ADR0/MD0	MS	ADR0	MD0
MDO/ADR1/MD1	MDO	ADR1	MD1
MDI/SDA/DEMP	MDI	SDA	DEMP
MC/SCL/FMT	MC	SCL	FMT

Both serial controls are available while RST = high and after internal reset completion, which is indicated as a negative transition (high ≥ low) of a 4096 × SCKI width pulse on the OVF pin.

HARDWARE CONTROL MODE CONFIGURATION

The data format is selected by the MC/SCL/FMT pin between I^{2}S format and I^{2}S mode in TDM format, as shown in Table 12.

Table 12. Data Format Selection

FMT	MODE CONTROL INTERFACE
Low	I^{2}S audio data format
High	I^{2}S mode, TDM audio data format (supported only for SCKI = 128 f$_S$, 256 f$_S$, or 512 f$_S$)

Product Folder Link(s): *PCM3168A PCM3168A-Q1*

The de-emphasis filter is enabled by the MDI/SDA/DEMP pin. The de-emphasis frequency is fixed at 44.1 kHz in hardware control mode, as shown in Table 13. The software mode provides full selections of 32 kHz, 44.1 kHz, and 48 kHz.

Table 13. Hardware Control Mode

DEMP (DE-EMPHASIS FILTER ENABLE)	DESCRIPTION
Low	44.1 kHz, de-emphasis disabled
High	44.1 kHz, de-emphasis enabled

The audio interface and the sampling mode are selected by the MS/ADR0/MD0 and MDO/ADR1/MD1 pins. The selectable multiple of the master mode audio interface is limited between 256 f_S, 384 f_S, and 512 f_S; the selectable sampling mode is limited as shown in Table 14. The software mode provides full selections.

Table 14. Selectable Sampling Mode

MD1	MD0	INTERFACE MODE ADC	DAC	SAMPLING MODE ADC	DAC
Low	Low	Slave[1]	Slave[1]	Auto[2]	Auto[2]
Low	High	Master, 512 f_S	Slave[1]	Single rate	Auto[2]
High	Low	Master, 384 f_S	Slave[1]	Dual rate	Auto[2]
High	High	Master, 256 f_S	Slave[1]	Dual rate	Auto[2]

(1) The multiples between system clock and sampling frequency are automatically detected; 256 f_S, 384 f_S, 512 f_S, and 768 f_S are acceptable for ADC operation, and 128 f_S, 192 f_S, 256 f_S, 384 f_S, 512 f_S, and 768 f_S are acceptable for DAC operation.
(2) The sampling mode is automatically set as single rate for 512 f_S and 768 f_S, dual rate for 256 f_S and 384 f_S, and quad rate for 128 f_S and 198 f_S, according to the detected multiples between the system clock and sampling clock.

FOUR-WIRE (SPI) SERIAL CONTROL

The PCM3168A and PCM3168A-Q1 include an SPI-compatible serial port that operates asynchronously with the audio serial interface. The control interface consists of MDI/SDA/DEMP, MDO/ADR1/MD1, MC/SCL/FMT, and MS/ADR0/MD0. MDI is the serial data input to program the mode control registers. MDO is the serial data output to read back register settings and some flags. MDO is inactive (Hi-Z, high impedance) during MS = high. MC is the serial bit clock that shifts the data into the control port. MS is the select input to enable the mode control port.

CONTROL DATA WORD FORMAT

All single write/read operations via the serial control port use 16-bit data words. Figure 47 shows the control data word format. The first bit is for read/write controls; '0' indicates a write operation and '1' indicates a read operation. Following the first bit are seven other bits, labeled ADR[6:0] that set the register address for the write/read operation. The eight least significant bits (LSBs), D[7:0] on MDI or MDO, contain the data to be written to the register specified by ADR[6:0], or the data read from the register specified by ADR[6:0].
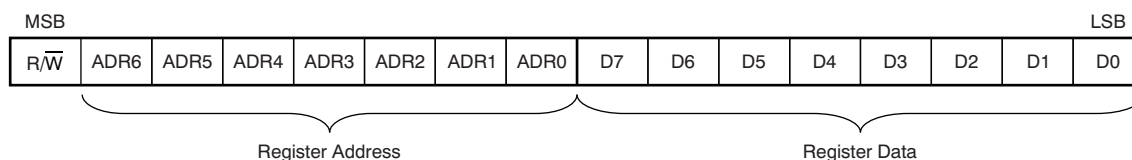

Figure 47. Control Data Word Format for MDI

PCM3168A
PCM3168A-Q1

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REGISTER WRITE OPERATION

Figure 48 shows the functional timing diagram for single write operations on the serial control port. MS is held at a high state until a register must be written. To start the register write cycle, MS is set to a low state. 16 clocks are then provided on MC, corresponding to the 16 bits of the control data word on MDI. After the 16th clock cycle has been completed, MS is set high to latch the data into the indexed mode control register.

Also, the PCM3168A and PCM3168A-Q1 support multiple write operations in addition to single write operations, which can be performed by sending the following N-times of the 8-bit register data after the first 16-bit register address and register data while keeping the MC clocks and MS at a low state. Closing a multiple write operation can be accomplished by setting MS to a high state.
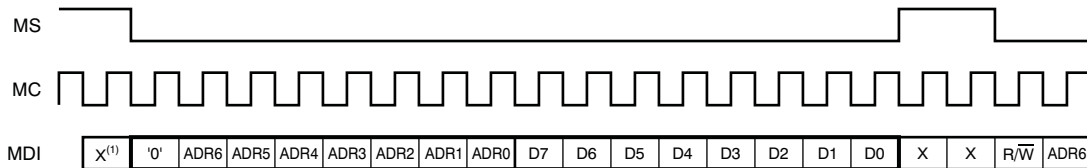
(1) X = Don't care.

Figure 48. Register Write Operation

REGISTER READ OPERATION

Figure 49 shows the functional timing diagram for single read operations on the serial control port. MS is held at a high state until a register must be read. To start the register read cycle, MS is set to a low state. 16 clocks are then provided on MC, corresponding to the first eight bits of the control data word on MDI and the second eight bits of the read-back data word from MDO. After the 16th clock cycle has been completed, MS is held high for the next write or read operation. MDO remains in a high impedance state except during the eight MC clock periods of the actual data transfer.
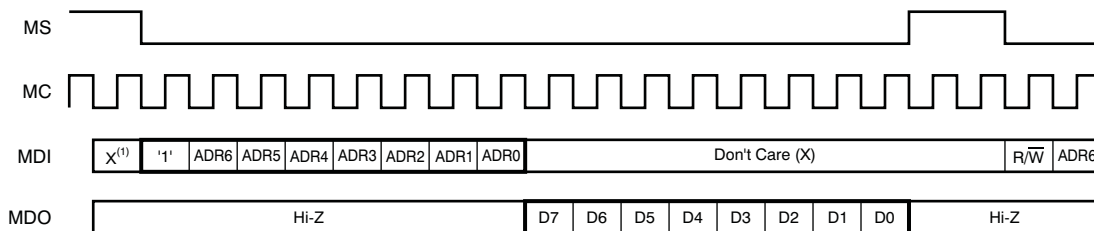
(1) X = Don't care.

Figure 49. Register Read Operation

Product Folder Link(s): *PCM3168A PCM3168A-Q1*

TIMING CHARACTERISTICS: FOUR-WIRE
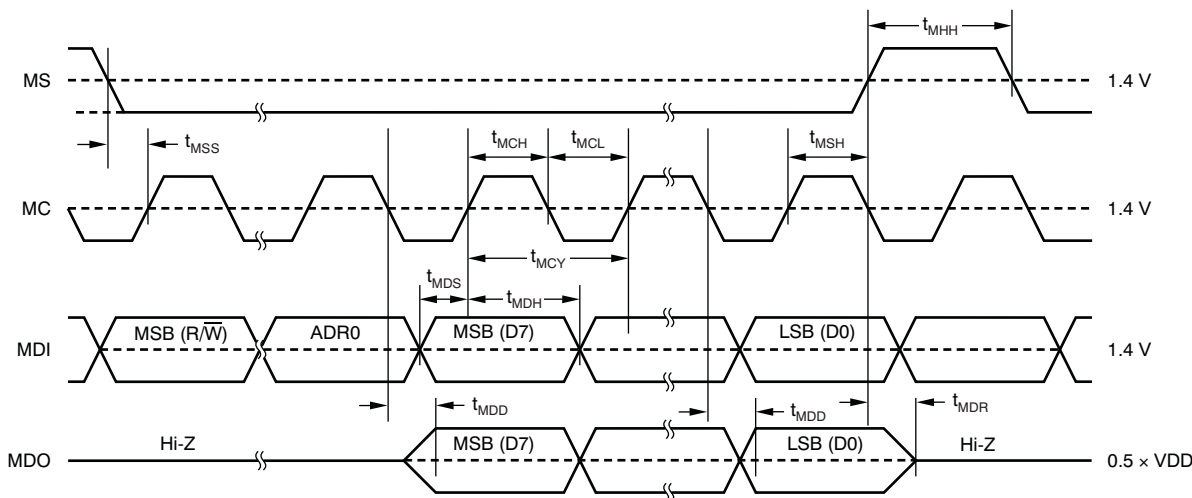
(1) These timing parameters are critical for proper control port operation.

Figure 50. Four-Wire Serial Control Interface Timing[1]

Timing Requirements for Figure 50[1]

SYMBOL	PARAMETER	PCM3168A, PCM3168A-Q1		UNIT
		MIN	MAX	
t_{MCY}	MC pulse cycle time	100		ns
t_{MCL}	MC low-level time	40		ns
t_{MCH}	MC high-level time	40		ns
t_{MHH}	MS high-level time	t_{MCY}		ns
t_{MSS}	MS falling edge to MC rising edge	30		ns
t_{MSH}	MS rising edge from MC rising edge for LSB	15		ns
t_{MDH}	MDI hold time	15		ns
t_{MDS}	MDI setup time	15		ns
t_{MDD}	MDO enable or delay time from MC falling edge	0	30	ns
t_{MDR}	MDO disable time from MS rising edge	0	30	ns

(1) These timing parameters are critical for proper control port operation.

TWO-WIRE (I²C) SERIAL CONTROL

The PCM3168A and PCM3168A-Q1 support an I²C-compatible serial bus and data transmission protocol for fast mode configured as a slave device. This protocol is explained in the I²C specification, version 2.0.

The PCM3168A and PCM3168A-Q1 have a 7-bit slave address, as shown in Figure 51. The first five bits are the most significant bits (MSB) of the slave address and are factory-preset to *10001*. The next two bits of the address byte are selectable bits that can be set by MS/ADR0/MD0 and MDO/ADR1/MD1. A maximum of four PCM3168A and PCM3168A-Q1s can be connected on the same bus at any one time. Each PCM3168A and PCM3168A-Q1 respond when it receives its own slave address.
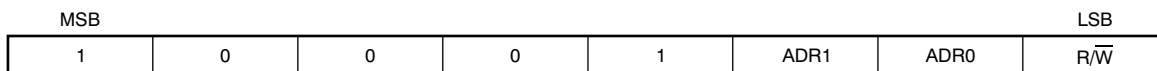
MSB   LSB

1	0	0	0	1	ADR1	ADR0	R/$\overline{W}$

Figure 51. Slave Address

PACKET PROTOCOL

A master device must control the packet protocol, which consists of the start condition, slave address with the read/write bit, data if a write operation is required, acknowledgement if a read operation is required, and stop condition. The PCM3168A and PCM3168A-Q1 support both slave receiver and transmitter functions. Details about DATA for both write and read operations are described in Figure 52.
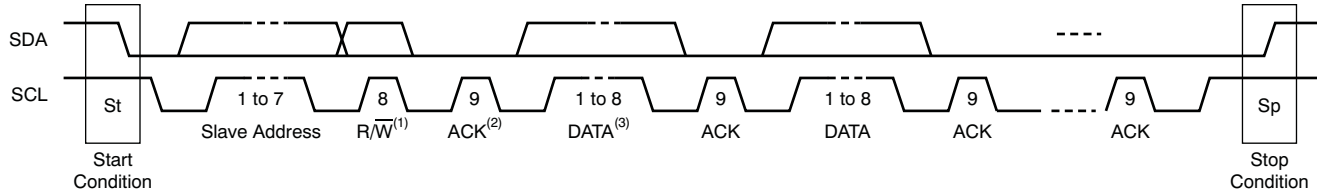
(1) R/$\overline{W}$: Read operation if '1'; write operation otherwise.

(2) ACK: Acknowledgement of a byte if '0', not Acknowledgement of a byite if '1'.

(3) DATA: Eight bits (byte); details are described in the *Write Operation* and *Read Operation* sections.

Figure 52. DATA Operation

WRITE OPERATION

The PCM3168A and PCM3168A-Q1 support a receiver function. A master device can write to any PCM3168A and PCM3168A-Q1 register using single or multiple accesses. The master sends a PCM3168A and PCM3168A-Q1 slave address with a write bit, a register address, and the data. If multiple access is required, the address is that of the starting register, followed by the data to be transferred. When the data are received properly, the index register is incremented by one automatically. When the index register reaches &h5E, the next value is &h40. When undefined registers are accessed, the PCM3168A and PCM3168A-Q1 do not send an acknowledgement. Figure 53 illustrates a diagram of the write operation. The register address and write data are in 8-bit, MSB-first format.

Transmitter	M	M	M	S	M	S	M	S	M	S		S	M
Data Type	St	Slave Address	$\overline{W}$	ACK	Reg Address	ACK	Write Data 1	ACK	Write Data 2	ACK		ACK	Sp

(1) M = Master device, S = Slave device, St = Start condition, $\overline{W}$ = Write, ACK = Acknowledge, and Sp = Stop condition.

Figure 53. Framework for Write Operation

READ OPERATION

A master device can read the registers from &h40 to &h5E of the PCM3168A and PCM3168A-Q1. The value of the register address is stored in an indirect index register in advance. The master sends the PCM3168A and PCM3168A-Q1 slave address with a read bit after storing the register address. Then the PCM3168A and PCM3168A-Q1 transfer the data that the index register points to. Figure 54 shows a diagram of the read operation.

Transmitter	M	M	M	S	M	S	M	M	M	S	S	M	M
Data Type	St	Slave Address	$\overline{W}$	ACK	Reg Address	ACK	Sr	Slave Address	R	ACK	Read Data	NACK	Sp

(1) M = Master device, S = Slave device, St = Start condition, Sr = Repeated start condition, $\overline{W}$ = Write, R = Read, ACK = Acknowledge, NACK = Not acknowledge, and Sp = Stop condition.

NOTE: The slave address after the repeated start condition must be the same as the previous address.

Figure 54. Framework for Read Operation

TIMING REQUIREMENTS: SCL AND SDA
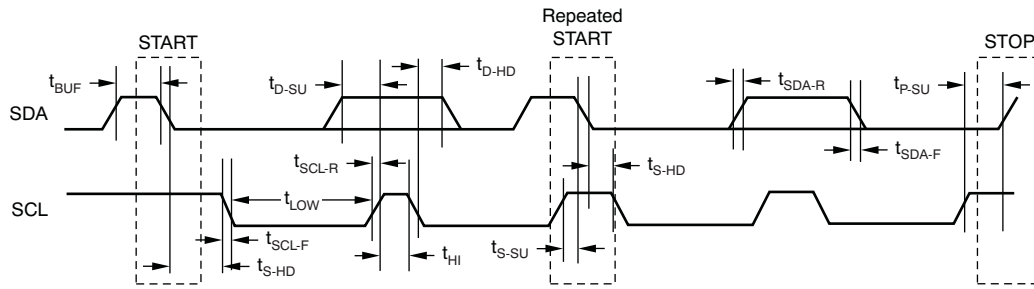
Figure 55. SCL and SDA Control Interface Timing

Timing Requirements for Figure 55

SYMBOL	PARAMETER	PCM3168A, PCM3168A-Q1				UNIT
		STANDARD MODE		FAST MODE		
		MIN	MAX	MIN	MAX	
f_{SCL}	SCL clock frequency		100		400	kHz
t_{BUF}	Bus free time between STOP and START condition	4.7		1.3		µs
t_{LOW}	Low period of the SCL clock	4.7		1.3		µs
t_{HI}	High period of the SCL clock	4.0		0.6		µs
$t_{S\text{-}SU}$	Setup time for START/Repeated START condition	4.7		0.6		µs
$t_{S\text{-}HD}$	Hold time for START/Repeated START condition	4.0		0.6		µs
$t_{D\text{-}SU}$	Data setup time	250		100		ns
$t_{D\text{-}HD}$	Data hold time	0	3450	0	900	ns
$t_{SCL\text{-}R}$	Rise time of SCL signal		1000	$20 + 0.1\,C_B$	300	ns
$t_{SCL\text{-}F}$	Fall time of SCL signal		1000	$20 + 0.1\,C_B$	300	ns
$t_{SDA\text{-}R}$	Rise time of SDA signal		1000	$20 + 0.1\,C_B$	300	ns
$t_{SDA\text{-}F}$	Fall time of SDA signal		1000	$20 + 0.1\,C_B$	300	ns
$t_{P\text{-}SU}$	Setup time for STOP condition	4.0		0.6		µs
t_{GW}	Allowable glitch width		N/A		50	
C_B	Capacitive load for SDA and SCL line		400		100	pF
V_{NH}	Noise margin at high level for each connected device (including hysteresis)	$0.2 \times VDD$		$0.2 \times VDD$		V
V_{NL}	Noise margin at low level for each connected device (including hysteresis)	$0.1 \times VDD$		$0.1 \times VDD$		V
V_{HYS}	Hysteresis of Schmitt-trigger input	N/A		$0.05 \times VDD$		V

CONTROL REGISTER DEFINITIONS (SOFTWARE MODE ONLY)

The PCM3168A and PCM3168A-Q1 have many user-programmable functions that are accessed via control registers, and are programmed through the SPI or I^{2}C serial control port. Table 15 shows the available mode control functions along with reset default conditions and associated register address. Table 16 lists the register map.

Table 15. User-Programmable Mode Control Functions

FUNCTION	RESET DEFAULT	REGISTER	LABEL
Mode control register reset for ADC and DAC operation	Normal operation	64	MRST
System reset for ADC and DAC operation	Normal operation	64	SRST
DAC sampling mode selection	Auto	64	SRDA[1:0]
DAC power-save mode selection	Power save	65	PSMDA
DAC master/slave mode selection	Slave	65	MSDA[2:0]
DAC audio interface format selection	I^{2}S	65	FMTDA[3:0]
DAC operation control	Normal operation	66	OPEDA[3:0]
DAC digital filter roll-off control	Sharp roll-off	66	FLT[3:0]
DAC output phase selection	Normal	67	REVDA[8:1]
DAC soft mute control	Mute disabled	68	MUTDA[8:1]
DAC zero flag	Not detected	69	ZERO[8:1]
DAC digital attenuation mode	Channel independent	70	ATMDDA
DAC digital attenuation speed	N × 2048/f$_S$	70	ATSPDA
DAC digital de-emphasis function control	Disabled	70	DEMP[1:0]
DAC zero flag function selection	Independent	70	AZRO[2:0]
DAC zero flag polarity selection	High for detection	70	ZREV
DAC digital attenuation level shifting	0 dB, no attenuation	71–79	ATDAx[7:0]
ADC sampling mode selection	Auto	80	SRAD[1:0]
ADC master/slave mode selection	Slave	81	MSAD[2:0]
ADC audio interface format selection	I^{2}S	81	FMTAD[2:0]
ADC power-save control	Normal operation	82	PSVAD[2:0]
ADC HPF bypass control	Normal output, HPF enabled	82	BYP[2:0]
ADC input configuration control	Differential	83	SEAD[6:1]
ADC input phase selection	Normal	84	REVAD[6:1]
ADC soft mute control	Mute disabled	85	MUTAD[6:1]
ADC overflow flag	Not detected	86	OVF[6:1]
ADC digital attenuation mode	Channel independent	87	ATMDAD
ADC digital attenuation speed	N × 2048/f$_S$	87	ATSPAD
ADC overflow flag polarity selection	High for detection	87	OVFP
ADC digital attenuation level setting	0 dB, no gain or attenuation	88–94	ATADx[7:0]

Table 16. Register Map

ADDRESS		DATA							
DAC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
64	40	MRST	SRST	—	—	—	—	SRDA1	SRDA0
65	41	PSMDA	MSDA2	MSDA1	MSDA0	FMTDA3	FMTDA2	FMTDA1	FMTDA0
66	42	OPEDA3	OPEDA2	OPEDA1	OPEDA0	FLT3	FLT2	FLT1	FLT0
67	43	REVDA8	REVDA7	REVDA6	REVDA5	REVDA4	REVDA3	REVDA2	REVDA1
68	44	MUTDA8	MUTDA7	MUTDA6	MUTDA5	MUTDA4	MUTDA3	MUTDA2	MUTDA1
69	45	ZERO8	ZERO7	ZERO6	ZERO5	ZERO4	ZERO3	ZERO2	ZERO1
70	46	ATMDDA	ATSPDA	DEMP1	DEMP0	AZRO2	AZRO1	AZRO0	ZREV
71	47	ATDA07	ATDA06	ATDA05	ATDA04	ATDA03	ATDA02	ATDA01	ATDA00
72	48	ATDA17	ATDA16	ATDA15	ATDA14	ATDA13	ATDA12	ATDA11	ATDA10
73	49	ATDA27	ATDA26	ATDA25	ATDA24	ATDA23	ATDA22	ATDA21	ATDA20
74	4A	ATDA37	ATDA36	ATDA35	ATDA34	ATDA33	ATDA32	ATDA31	ATDA30
75	4B	ATDA47	ATDA46	ATDA45	ATDA44	ATDA43	ATDA42	ATDA41	ATDA40
76	4C	ATDA57	ATDA56	ATDA55	ATDA54	ATDA53	ATDA52	ATDA51	ATDA50
77	4D	ATDA67	ATDA66	ATDA65	ATDA64	ATDA63	ATDA62	ATDA61	ATDA60
78	4E	ATDA77	ATDA76	ATDA75	ATDA74	ATDA73	ATDA72	ATDA71	ATDA70
79	4F	ATDA87	ATDA86	ATDA85	ATDA84	ATDA83	ATDA82	ATDA81	ATDA80
80	50	—	—	—	—	—	—	SRAD1	SRAD0
81	51	—	MSAD2	MSAD1	MSAD0	—	FMTAD2	FMTAD1	FMTAD0
82	52	—	PSVAD2	PSVAD1	PSVAD0	—	BYP2	BYP1	BYP0
83	53	—	—	SEAD6	SEAD5	SEAD4	SEAD3	SEAD2	SEAD1
84	54	—	—	REVAD6	REVAD5	REVAD4	REVAD3	REVAD2	REVAD1
85	55	—	—	MUTAD6	MUTAD5	MUTAD4	MUTAD3	MUTAD2	MUTAD1
86	56	—	—	OVF6	OVF5	OVF4	OVF3	OVF2	OVF1
87	57	ATMDAD	ATSPAD	—	—	—	—	—	OVFP
88	58	ATAD07	ATAD06	ATAD05	ATAD04	ATAD03	ATAD02	ATAD01	ATAD00
89	59	ATAD17	ATAD16	ATAD15	ATAD14	ATAD13	ATAD12	ATAD11	ATAD10
90	5A	ATAD27	ATAD26	ATAD25	ATAD24	ATAD23	ATAD22	ATAD21	ATAD20
91	5B	ATAD37	ATAD36	ATAD35	ATAD34	ATAD33	ATAD32	ATAD31	ATAD30
92	5C	ATAD47	ATAD46	ATAD45	ATAD44	ATAD43	ATAD42	ATAD41	ATAD40
93	5D	ATAD57	ATAD56	ATAD55	ATAD54	ATAD53	ATAD52	ATAD51	ATAD50
94	5E	ATAD67	ATAD66	ATAD65	ATAD64	ATAD63	ATAD62	ATAD61	ATAD60

Product Folder Link(s): *PCM3168A PCM3168A-Q1*

REGISTER DEFINITIONS

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
64	40	MRST	SRST	—	—	—	—	SRDA1	SRDA0

MRST **Mode control register reset for the ADC and DAC**

This bit sets the mode control register reset to the default value. Pop-noise may be generated. Returning the MRST bit to '1' is unneccesary, because it is automatically set to '1' after the mode control register is reset.

Default value = 1.

MRST	Mode control register reset
0	Set default value
1	Normal operation (default)

SRST **System reset for the ADC and DAC**

This bit controls system reset, the relation between system clock and sampling clock re-synchronization, and ADC operation and DAC operation restart. The mode control register is not reset and the PCM3168A and PCM3168A-Q1 do not go into a power-down state. The fade-in sequence is supported in the resume process, but pop-noise may be generated. Returning the SRST bit to '1' is unneccesary; it is automatically set to '1' after triggering a system reset.

Default value = 1.

SRST	System reset
0	Resynchronization
1	Normal operation (default)

SRDA[1:0] **DAC Sampling mode select**

These bits control the sampling mode of DAC operation. In Auto mode, the sampling mode is automatically set according to multiples between the system clock and sampling clock, single rate for 512 f_S and 768 f_S, dual rate for 256 f_S or 384 f_S, and quad rate for 128 f_S and 192 f_S.

Default value = 00.

SRDA	DAC Sampling mode select
00	Auto (default)
01	Single rate
10	Dual rate
11	Quad rate

Product Folder Link(s): *PCM3168A PCM3168A-Q1*

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
65	41	PSMDA	MSDA2	MSDA1	MSDA0	FMTDA3	FMTDA2	FMTDA1	FMTDA0

PSMDA   **DAC Power-save mode select**

This bit selects the power-save mode for the OPEDA[3:0] function. OPEDA[3:0] is the control of power-save mode and normal operation for PSMDA = 0, or OPEDA[3:0] works as the control of DAC disable (not power-save mode) and normal operation for PSMDA = 1.

Default value: 0.

PSMDA	DAC Power-save mode select
0	Power-save enable mode (default)
1	Power-save disable mode

MSDA[2:0]   **DAC Master/slave mode select**

These bits control the audio interface mode for DAC operation.

Default value: 000 (slave mode).

MSDA	DAC Master/slave mode select
000	Slave mode (default)
001	Master mode, 768 f_S
010	Master mode, 512 f_S
011	Master mode, 384 f_S
100	Master mode, 256 f_S
101	Master mode, 192 f_S
110	Master mode, 128 f_S
111	Reserved

FMTDA[3:0] **DAC Audio interface format select**

These bits control the audio interface format for DAC operation. Details of the format, and any related restrictions with the system clock and master/slave mode, are described in the *Audio Data Interface Formats and Timing* section.

Default value: 0000 (24-bit I²S format).

FMTDA	DAC Audio interface format select
0000	24-bit I²S format (default)
0001	24-bit left-justified format
0010	24-bit right-justified format
0011	16-bit right-justified format
0100	24-bit I²S mode DSP format
0101	24-bit left-justified mode DSP format
0110	24-bit I²S mode TDM format
0111	24-bit left-justified mode TDM format
1000	24-bit high-speed I²S mode TDM format
1001	24-bit high-speed left-justified mode TDM format
101x	Reserved
11xx	Reserved

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
66	42	OPEDA3	OPEDA2	OPEDA1	OPEDA0	FLT3	FLT2	FLT1	FLT0

OPEDA[3:0] DAC Operation control

These bits control the DAC operation mode. In operation disable mode, the DAC output is cut off from DIN with a fade-out sequence, and the internal DAC data is reset. DAC output is forced into VCOMDA if PSMDA = 1, or DAC output is forced into AGNDDA and goes into a power-down state if PSMDA = 0. For normal operating mode, a fade-in sequence is applied on the DAC output in resume process. The serial mode control is effective during operation disable mode. A wait time greater than $t_{DACDLY2}$ is required for the status change because of power-save control turning on/off.

Default value: 0000.

OPEDA	DAC Operation control
xxx0	DAC1/2 normal operation
xxx1	DAC1/2 operation disable with or without power save
xx0x	DAC3/4 normal operation
xx1x	DAC3/4 operation disable with or without power save
x0xx	DAC5/6 normal operation
x1xx	DAC5/6 operation disable with or without power save
0xxx	DAC7/8 normal operation
1xxx	DAC7/8 operation disable with or without power save

FLT[3:0]   DAC Digital filter roll-off control

The FLT[3:0] bits allow users to select the digital filter roll-off that is best suited to their applications. Sharp and Slow filter roll-off selections are available. The filter responses for these selections are shown in the Typical Characteristics section of this data sheet.

Default value: 0000.

FLT	DAC Digital filter roll-off control
xxx0	DAC1/2 sharp roll-off
xxx1	DAC1/2 slow roll-off
xx0x	DAC3/4 sharp roll-off
xx1x	DAC3/4 slow roll-off
x0xx	DAC5/6 sharp roll-off
x1xx	DAC5/6 slow roll-off
0xxx	DAC7/8 sharp roll-off
1xxx	DAC7/8 slow roll-off

Product Folder Link(s): *PCM3168A PCM3168A-Q1*

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
67	43	REVDA8	REVDA7	REVDA6	REVDA5	REVDA4	REVDA3	REVDA2	REVDA1

REVDA[8:1] DAC Output phase select

The REVDA[8:1] bits are used to control the phase of DAC analog signal outputs.

Default value: 0000 0000.

REVDA	DAC Output phase select
xxxx xxx0	DAC1 normal output
xxxx xxx1	DAC1 inverted output
xxxx xx0x	DAC2 normal output
xxxx xx1x	DAC2 inverted output
xxxx x0xx	DAC3 normal output
xxxx x1xx	DAC3 inverted output
xxxx 0xxx	DAC4 normal output
xxxx 1xxx	DAC4 inverted output
xxx0 xxxx	DAC5 normal output
xxx1 xxxx	DAC5 inverted output
xx0x xxxx	DAC6 normal output
xx1x xxxx	DAC6 inverted output
x0xx xxxx	DAC7 normal output
x1xx xxxx	DAC7 inverted output
0xxx xxxx	DAC8 normal output
1xxx xxxx	DAC8 inverted output

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Product Folder Link(s): *PCM3168A PCM3168A-Q1*

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
68	44	MUTDA8	MUTDA7	MUTDA6	MUTDA5	MUTDA4	MUTDA3	MUTDA2	MUTDA1

MUTDA[8:1] DAC Soft Mute control

These bits are used to enable or disable the Soft Mute function for the corresponding DAC outputs, VOUT. The Soft Mute function is incorporated into the digital attenuators.
When Mute is disabled (MUTDA[8:1] = 0), the attenuator and DAC operate normally. When Mute is enabled by setting MUTDA[8:1] = 1, the digital attenuator for the corresponding output decreases from the current setting to infinite attenuation with an s-curve response and time set by ATSPDA.
By setting MUTDA[8:1] = 0, the attenuator increases to the last attenuation level with s-curve response in the same manner as it is for decreasing levels. This configuration provides *pop and zipper noise-free* muting of the DAC output.
The Soft Mute control uses the same digital attenuation level resource setting as the DAC. Mute control has priority over the digital attenuation level setting.

Default value: 0000 0000.

MUTDA	DAC Soft Mute control
xxxx xxx0	DAC1 Mute disabled
xxxx xxx1	DAC1 Mute enabled
xxxx xx0x	DAC2 Mute disabled
xxxx xx1x	DAC2 Mute enabled
xxxx x0xx	DAC3 Mute disabled
xxxx x1xx	DAC3 Mute enabled
xxxx 0xxx	DAC4 Mute disabled
xxxx 1xxx	DAC4 Mute enabled
xxx0 xxxx	DAC5 Mute disabled
xxx1 xxxx	DAC5 Mute enabled
xx0x xxxx	DAC6 Mute disabled
xx1x xxxx	DAC6 Mute enabled
x0xx xxxx	DAC7 Mute disabled
x1xx xxxx	DAC7 Mute enabled
0xxx xxxx	DAC8 Mute disabled
1xxx xxxx	DAC8 Mute enabled

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
69	45	ZERO8	ZERO7	ZERO6	ZERO5	ZERO4	ZERO3	ZERO2	ZERO1

ZERO[8:1]   **DAC Zero flag (read-only)**

These bits indicate the present status of the zero detect circuit for each DAC channel; these bits are read-only.

ZERO	DAC Zero flag
xxxx xxx0	DAC1 zero input not detected
xxxx xxx1	DAC1 zero input detected
xxxx xx0x	DAC2 zero input not detected
xxxx xx1x	DAC2 zero input detected
xxxx x0xx	DAC3 zero input not detected
xxxx x1xx	DAC3 zero input detected
xxxx 0xxx	DAC4 zero input not detected
xxxx 1xxx	DAC4 zero input detected
xxx0 xxxx	DAC5 zero input not detected
xxx1 xxxx	DAC5 zero input detected
xx0x xxxx	DAC6 zero input not detected
xx1x xxxx	DAC6 zero input detected
x0xx xxxx	DAC7 zero input not detected
x1xx xxxx	DAC7 zero input detected
0xxx xxxx	DAC8 zero input not detected
1xxx xxxx	DAC8 zero input detected

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
70	46	ATMDDA	ATSPDA	DEMP1	DEMP0	AZRO2	AZRO1	AZRO0	ZREV

ATMDDA   **DAC Attenuation mode**

This bit controls the DAC attenuation mode. ATDA1[7:0] to ATDA8[7:0] are simply used for ATMDDA = 0, and ATDA0[7:0] + ATDA1[7:0] to ATDA0[7:0] + ATDA8[7:0] in decibel number are used for ATMDDA = 1.

Default value: 0.

ATMDDA	DAC Attenuation mode
0	Each channel with independent data (default)
1	All channels with preset (independent) data + master (common) data in decibel number

ATSPDA   **DAC Attenuation speed**

This bit controls the DAC attenuation speed. $N \times 2048/f_S$ for ATSPDA = 0 and $N \times 4096/f_S$ for ATSPDA = 1. N is automatically selected according to the DAC sampling mode, SRDA, N = 1 for single rate, N = 2 for dual rate, and N = 4 for quad rate.

Default value: 0.

ATSPDA	DAC Attenuation speed
0	$N \times 2048/f_S$ (default)
1	$N \times 4096/f_S$

DEMP[1:0]   **DAC Digital de-emphasis function/sampling rate control**

These bits are used to control the enable/disable and sampling frequency of the digital de-emphasis function.

Default value: 00.

DEMP	DAC Digital de-emphasis function/sampling rate control
00	Disable (default)
01	48 kHz enable
10	44.1 kHz enable
11	32 kHz enable

AZRO[2:0]   **DAC Zero flag function select**

The AZRO[2:0] bits are used to select the function of the zero flag pin.

Default value: 000.

AZRO	DAC Zero flag function select
000	DAC1/2/3/4/5/6/7/8 (8 channel) zero input detect with AND logic (default)
001	DAC1/2/3/4/5/6/7/8 (8 channel) zero input detect with OR logic
010	DAC1/2/3/4/5/6 (6 channel) zero input detect with AND logic
011	DAC1/2/3/4/5/6 (6 channel) zero input detect with OR logic
100	DAC7/8 (2 channel) zero input detect with AND logic
101	DAC7/8 (2 channel) zero input detect with OR logic
11x	Reserved

ZREV   **DAC Zero flag polarity select**

This bit controls the polarity of the zero flag pin.

Default value: 0.

ZREV	DAC Zero flag polarity select
0	High for zero detect (default)
1	Low for zero detect

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
71	47	ATDA07	ATDA06	ATDA05	ATDA04	ATDA03	ATDA02	ATDA01	ATDA00
72	48	ATDA17	ATDA16	ATDA15	ATDA14	ATDA13	ATDA12	ATDA11	ATDA10
73	49	ATDA27	ATDA26	ATDA25	ATDA24	ATDA23	ATDA22	ATDA21	ATDA20
74	4A	ATDA37	ATDA36	ATDA35	ATDA34	ATDA33	ATDA32	ATDA31	ATDA30
75	4B	ATDA47	ATDA46	ATDA45	ATDA44	ATDA43	ATDA42	ATDA41	ATDA40
76	4C	ATDA57	ATDA56	ATDA55	ATDA54	ATDA53	ATDA52	ATDA51	ATDA50
77	4D	ATDA67	ATDA66	ATDA65	ATDA64	ATDA63	ATDA62	ATDA61	ATDA60
78	4E	ATDA77	ATDA76	ATDA75	ATDA74	ATDA73	ATDA72	ATDA71	ATDA70
79	4F	ATDA87	ATDA86	ATDA85	ATDA84	ATDA83	ATDA82	ATDA81	ATDA80

ATDAx[7:0]   **DAC Digital attenuation level setting**

Where x = 0 and 1 to 8, corresponding to the DAC channel, DACx (x = 1 to 8).

Each DAC channel (VOUTx) has a digital attenuator function. The attenuation level can be set from 0 dB to −100 dB in 0.5-dB steps, and also can be set to infinite attenuation (mute). The attenuation level change from current value to target value is performed by incrementing or decrementing with s-curve responses and a time set by ATSPDA. While an attenuation level change sequence is in progress, new processing of the attenuation level change for new commands are ignored; any new commands are overwritten into the command buffer. The last command for the attenuation level change is performed after the present attenuation level change sequence is finished.

The attenuation level for each channel can be set individually using the following formula; the table below shows attenuation levels for various settings.

Attenuation level (dB) = 0.5 × (ATDAx[7:0]DEC – 255), where ATDAx[7:0]DEC = 0 through 255 for ATDAx[7:0]DEC = 0 through 54, attenuation is set to infinite attenuation (Mute).

ATDA0[7:0] are used to control all channels at the same time with attenuation data of ATDA0[7:0] + ATDAx[7:0] in decibel number, when ATMDDA is set to '1'. This scheme provides preset and master volume operation.

Default value: 1111 1111.

ATDAx	Decimal value	Attenuation level setting
1111 1111	255	0 dB, no attenuation (default)
1111 1110	254	−0.5 dB
1111 1101	253	−1.0 dB
...	...	...
1000 0001	129	−63.0 dB
1000 0000	128	−63.5 dB
0111 1111	127	−64 dB
...	...	...
0011 1000	56	−99.5 dB
0011 0111	55	−100 dB
0011 0110	54	Mute
...	...	...
0000 0000	0	Mute

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
80	50	—	—	—	—	—	—	SRAD1	SRAD0

SRAD[1:0]   ADC Sampling mode select

These bits control the sampling mode of ADC operation. In Auto mode, the sampling mode is automatically set according to multiples between system clock and sampling clock, single rate for 512 f_S and 768 f_S, and dual rate for 256 f_S and 384 fS.

Default value: 00.

SRAD	ADC Sampling mode select
00	Auto (default)
01	Single rate
10	Dual rate
11	Reserved

Product Folder Link(s): *PCM3168A PCM3168A-Q1*

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
81	51	—	MSAD2	MSAD1	MSAD0	—	FMTAD2	FMTAD1	FMTAD0

MSAD[2:0]   **ADC Master/slave mode select**

These bits control the audio interface mode for ADC operation.

Default value: 000 (slave mode).

MSAD	ADC Master/slave mode select
000	Slave mode (default)
001	Master mode, 768 f_S
010	Master mode, 512 f_S
011	Master mode, 384 f_S
100	Master mode, 256 f_S
101	Reserved
110	Reserved
111	Reserved

FMTAD[2:0]   **ADC Audio interface format select**

These bits control the audio interface format for ADC operation. The format details and restrictions related to the system clock and master/slave mode are described in the *Audio Data Interface Formats and Timing* section.

Default value: 000 (24-bit I^{2}S format).

FMTAD	ADC Audio interface format select
000	24-bit I^{2}S format (default)
001	24-bit left-justified format
010	24-bit right-justified format
011	16-bit right-justified format
100	24-bit I^{2}S mode DSP format
101	24-bit left-justified mode DSP format
110	24-bit I^{2}S mode TDM format
111	24-bit left-justified mode TDM format

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
82	52	—	PSVAD2	PSVAD1	PSVAD0	—	BYP2	BYP1	BYP0

PSVAD[2:0]   ADC Power-save control

These bits control the ADC power-save mode. In power-save mode, DOUT is forced into ZERO with a fade-out sequence, the internal ADC data are reset, and the ADC goes into a power-down state. For power-save mode release, a fade-in sequence is applied on DOUT in resume process. The serial mode control is enabled during this mode. Wait times greater than $t_{ADCDLY2}$ are required for the status change because of the power-save control turning on/off.

Default value: 000.

PSVAD	ADC Power-save control
xx0	ADC1/2 normal operation
xx1	ADC1/2 power-save mode
x0x	ADC3/4 normal operation
x1x	ADC3/4 power-save mode
0xx	ADC5/6 normal operation
1xx	ADC5/6 power-save mode

BYP[2:0]   ADC HPF bypass control

These bits control the HPF function and dc components of the input signal; internal dc offset is converted in bypass mode.

Default value: 000.

BYP	ADC HPF bypass control
xx0	ADC1/2 normal output, HPF enabled
xx1	ADC1/2 bypassed output, HPF disabled
x0x	ADC3/4 normal output, HPF enabled
x1x	ADC3/4 bypassed output, HPF disabled
0xx	ADC5/6 normal output, HPF enabled
1xx	ADC5/6 bypassed output, HPF disabled

Product Folder Link(s): *PCM3168A PCM3168A-Q1*

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
83	53	—	—	SEAD6	SEAD5	SEAD4	SEAD3	SEAD2	SEAD1

SEAD[6:1]   **ADC Input configuration control**

These bits control the input configuration of each ADC channel, differential or single-ended.

Default value: 00 0000 (all ADC channels have differential inputs).

SEAD	ADC Input configuration
xx xxx0	ADC1 differential input
xx xxx1	ADC1 single-ended input
xx xx0x	ADC2 differential input
xx xx1x	ADC2 single-ended input
xx x0xx	ADC3 differential input
xx x1xx	ADC3 single-ended input
xx 0xxx	ADC4 differential input
xx 1xxx	ADC4 single-ended input
x0 xxxx	ADC5 differential input
x1 xxxx	ADC5 single-ended input
0x xxxx	ADC6 differential input
1x xxxx	ADC6 single-ended input

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
84	54	—	—	REVAD6	REVAD5	REVAD4	REVAD3	REVAD2	REVAD1

REVAD[6:1] ADC Input phase select

These bits are used to control the phase of analog signal inputs.

Default value: 00 0000.

REVAD	ADC Input phase select
xx xxx0	ADC1 normal input
xx xxx1	ADC1 inverted input
xx xx0x	ADC2 normal input
xx xx1x	ADC2 inverted input
xx x0xx	ADC3 normal input
xx x1xx	ADC3 inverted input
xx 0xxx	ADC4 normal input
xx 1xxx	ADC4 inverted input
x0 xxxx	ADC5 normal input
x1 xxxx	ADC5 inverted input
0x xxxx	ADC6 normal input
1x xxxx	ADC6 inverted input

Product Folder Link(s): *PCM3168A PCM3168A-Q1*

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
85	55	—	—	MUTAD6	MUTAD5	MUTAD4	MUTAD3	MUTAD2	MUTAD1

MUTAD[6:1] ADC Soft Mute control

These bits are used to enable or disable the Soft Mute function for the corresponding ADC outputs, DOUT. The Soft Mute function is incorporated into the digital attenuators.

When Mute is disabled (MUTAD[6:1] = 0), the attenuator and ADC operate normally. When Mute is enabled by setting MUTAD[6:1] = 1, the digital attenuator for the corresponding output decreases from the current setting to infinite attenuation with an s-curve responses and time set by ATSPAD.

By setting MUTAD[6:1] = 0, the attenuator increases to the last attenuation level with the s-curve response in same manner as for decreasing levels. This provides *pop and zipper noise-free* muting for the ADC input.

The Soft Mute control uses the same digital attenuation level resource setting as the ADC. Mute control has priority over the digital attenuation level setting.

Default value: 00 0000.

MUTAD	ADC Soft Mute control
xx xxx0	ADC1 Mute disabled
xx xxx1	ADC1 Mute enabled
xx xx0x	ADC2 Mute disabled
xx xx1x	ADC2 Mute enabled
xx x0xx	ADC3 Mute disabled
xx x1xx	ADC3 Mute enabled
xx 0xxx	ADC4 Mute disabled
xx 1xxx	ADC4 Mute enabled
x0 xxxx	ADC5 Mute disabled
x1 xxxx	ADC5 Mute enabled
0x xxxx	ADC6 Mute disabled
1x xxxx	ADC6 Mute enabled

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
86	56	—	—	OVF6	OVF5	OVF4	OVF3	OVF2	OVF1

OVF[6:1]   ADC Overflow flag (read-only)

These bits indicate the status information of an overflow detect circuit for each ADC channel; these bits are read only. '1' means an overflow has been detected in the past, and reading this register resets all OVF bits.

OVF	ADC Overflow flag
xx xxx0	ADC1 overflow input not detected
xx xxx1	ADC1 overflow input detected
xx xx0x	ADC2 overflow input not detected
xx xx1x	ADC2 overflow input detected
xx x0xx	ADC3 overflow input not detected
xx x1xx	ADC3 overflow input detected
xx 0xxx	ADC4 overflow input not detected
xx 1xxx	ADC4 overflow input detected
x0 xxxx	ADC5 overflow input not detected
x1 xxxx	ADC5 overflow input detected
0x xxxx	ADC6 overflow input not detected
1x xxxx	ADC6 overflow input detected

Product Folder Link(s): *PCM3168A PCM3168A-Q1*

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
87	57	ATMDAD	ATSPAD	—	—	—	—	—	OVFP

ATMDAD   **ADC Attenuation mode**

This bit controls the ADC attenuation mode. ATAD1[7:0] to ATAD6[7:0] are simply used for ATMDAD = 0, and ATAD0[7:0] + ATAD1[7:0] to ATAD0[7:0] + ATAD6[7:0] in decibel number are used for ATMDAD = 1.

Default value: 0.

ATMDAD	ADC Attenuation mode
0	Each channel with independent data (default)
1	All channels with preset (independent) data + master (common) data in decibel number

ATSPAD   **ADC Attenuation speed**

This bit controls the ADC attenuation Speed, N × 2048/f_S for ATSPAD = 0 and N × 4096/f_S for ATSPAD = 1. N is automatically selected according to the ADC sampling mode, SRAD: N = 1 for single and N = 2 for dual rate.

Default value: 0.

ATSPAD	ADC Attenuation speed
0	N × 2048/f_S (default)
1	N × 4096/f_S

OVFP   **ADC Overflow flag polarity select**

This bit controls the polarity of the overflow flag pin.

Default value: 0.

OVFP	ADC Overflow flag polarity select
0	High for overflow detect (default)
1	Low for overflow detect

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
88	58	ATAD07	ATAD06	ATAD05	ATAD04	ATAD03	ATAD02	ATAD01	ATAD00
89	59	ATAD17	ATAD16	ATAD15	ATAD14	ATAD13	ATAD12	ATAD11	ATAD10
90	5A	ATAD27	ATAD26	ATAD25	ATAD24	ATAD23	ATAD22	ATAD21	ATAD20
91	5B	ATAD37	ATAD36	ATAD35	ATAD34	ATAD33	ATAD32	ATAD31	ATAD30
92	5C	ATAD47	ATAD46	ATAD45	ATAD44	ATAD43	ATAD42	ATAD41	ATAD40
93	5D	ATAD57	ATAD56	ATAD55	ATAD54	ATAD53	ATAD52	ATAD51	ATAD50
94	5E	ATAD67	ATAD66	ATAD65	ATAD64	ATAD63	ATAD62	ATAD61	ATAD60

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ATADx[7:0]   ADC Digital attenuation level setting

Where x = 0 and 1 to 6, corresponding to the ADC channel, ADCx (x = 1 to 6).

Each ADC channel has a digital attenuator function with 20-dB gain. The attenuation level can be set from 20 dB to −100 dB in 0.5-dB steps, and also can be set to infinite attenuation (mute). The attenuation level change from current value to target value is performed by increment or decrement with s-curve response and time set by ATSPAD. While the attenuation level change sequence is in progress, new processing of an attenuation level change for a new command is ignored; the new command is overwritten into the command buffer. The last command for an attenuation level change is performed after the present attenuation level change sequence is finished.

The attenuation level for each channel can be set individually using the following formula, and the above table shows attenuation levels for various settings.

Attenuation level (dB) = 0.5 × (ATADx[7:0]DEC − 215), where ATADx[7:0]DEC = 0 through 255 for ATADx[7:0]DEC = 0 through 14, attenuation is set to infinite attenuation (Mute).

ATAD0[7:0] is used to control all channels at the same time with attenuation data of ATAD0[7:0] + ATADx[7:0] in decibel number, though maximum level is limited within +20 dB, when ATMDAD is set to '1'. This scheme provides preset and master volume operation.

Default value: 1101 0111.

ATADx	Decimal value	Attenuation level setting
1111 1111	255	+20.0 dB
1111 1110	254	+19.5 dB
1111 1101	253	+19.0 dB
...	...	...
1101 1000	216	+0.5 dB
1101 0111	215	0 dB, no attenuation (default)
1101 0110	214	−0.5 dB
...	...	...
0001 0000	16	−99.5 dB
0000 1111	15	−100.0 dB
0000 1110	14	Mute
...	...	...
0000 0000	0	Mute

Product Folder Link(s): *PCM3168A PCM3168A-Q1*

APPLICATION INFORMATION

A typical circuit connection for six-channel analog in and eight-channel analog out is shown in Figure 56.
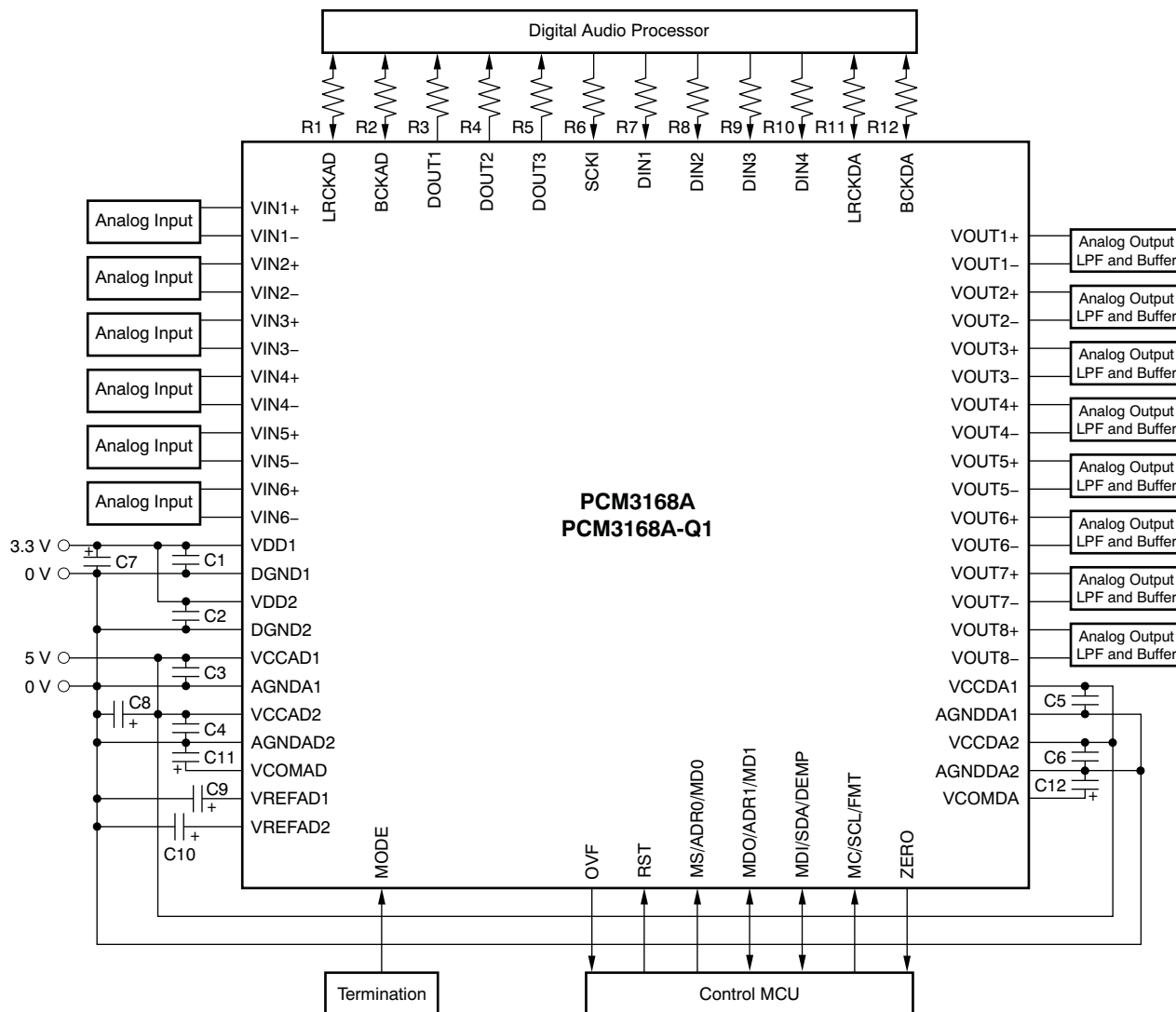
C_1 through C_6 are 1-μF ceramic capacitors dependent on power-supply quality. C_7 and C_8 are 10-μF electrolytic capacitors dependent on power-supply quality. C_9 and C_{10} are 10-μF electrolytic capacitors. C_{11} and C_{12} are 10-μF electrolytic capacitors. R_1 through R_{12} are 22-Ω to 100-Ω resistors.

Figure 56. Example Board Layout

Termination for mode control: any one of the circuits shown in Figure 57 must be applied according to the necessary mode/configuration. Resistor value must be 220 kΩ, ±5% tolerant. The PowerPAD must be tied to the ground plane with enough electrical and thermal conductivity; see the example board layout in Figure 56.
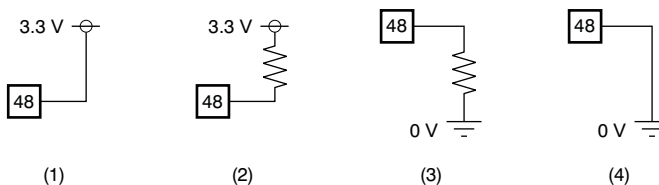
Figure 57. Typical Circuit Connections

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Typical interface circuits for analog input and analog output are shown in Figure 58 through Figure 63.
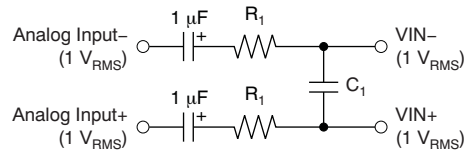
R_1 = 47-Ω to 470-Ω resistor, C_1 = 0.01-pF to 0.001-µF capacitor; $f_{-3\ dB}$ = 160 kHz.

NOTE: The signal source impedance must be low enough to apply this configuration.

Figure 58. Basic Differential Input Circuit with Anti-Aliasing LPF for Differential ADC Input
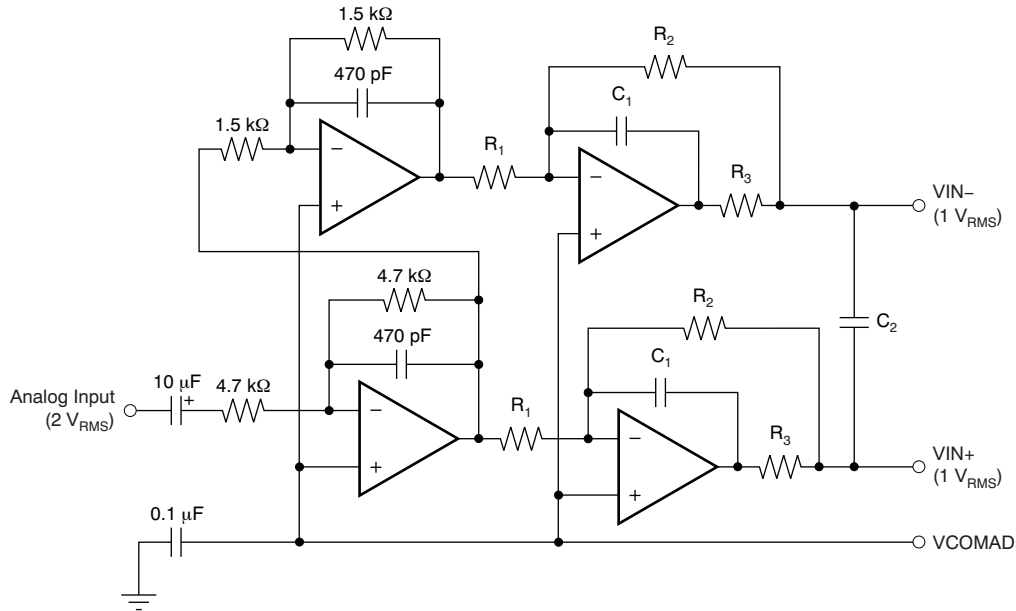
Amplifier is an NE5532A x2 or OPA2134 x2; R_1 = 1.5-kΩ resistor; R_2 = 750-Ω resistor; R_3 = 47-Ω resistor; C_1 = 3300-pF capacitor; C_2 = 0.01-µF capacitor; Gain = 1; $f_{-3\ dB}$ = 45 kHz.

Figure 59. Single-Ended to Differential Buffer and Anti-Aliasing LPF for Differential ADC Input
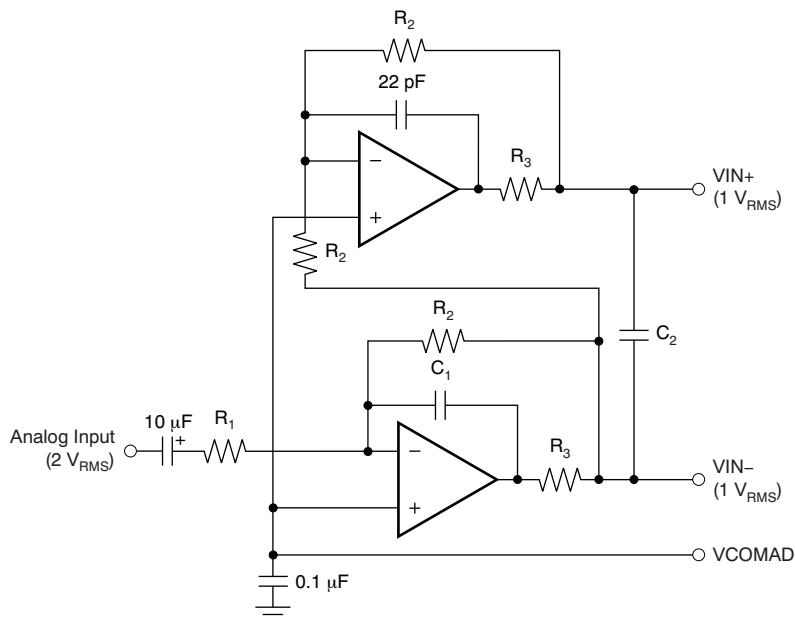
Product Folder Link(s): *PCM3168A PCM3168A-Q1*

Amplifier is an NE5532A x1 or OPA2134 x1; R_1 = 3-kΩ resistor; R_2 = 1.5-kΩ resistor; R_3 = 47-Ω resistor; C_1 = 2200-pF capacitor; C_2 = 0.01-µF capacitor; Gain = 1; $f_{-3\ dB}$ = 48 kHz.

Figure 60. Single-Ended to Differential Buffer and Anti-Aliasing LPF for Differential ADC Input
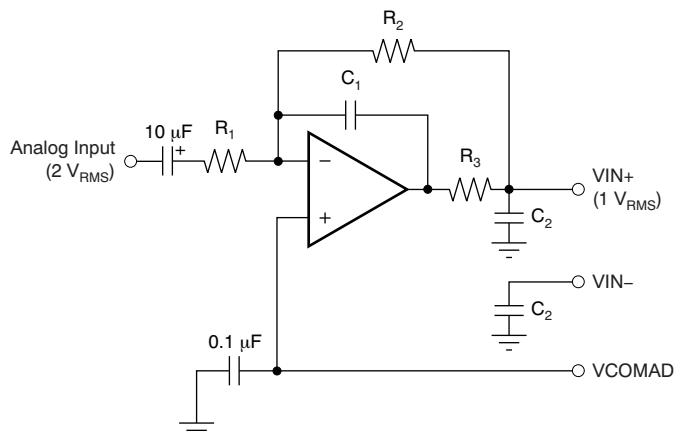
Amplifier is an NE5532A x1 or OPA2134 x1; R_1 = 3-kΩ resistor; R_2 = 1.5-kΩ resistor; R_3 = 47-Ω resistor; C_1 = 2200-pF capacitor; C_2 = 0.022-µF capacitor; Gain = 0.5; $f_{-3\ dB}$ = 48 kHz.

Figure 61. Buffer and Anti-Aliasing LPF for Single-Ended ADC Input

Product Folder Link(s): *PCM3168A PCM3168A-Q1*
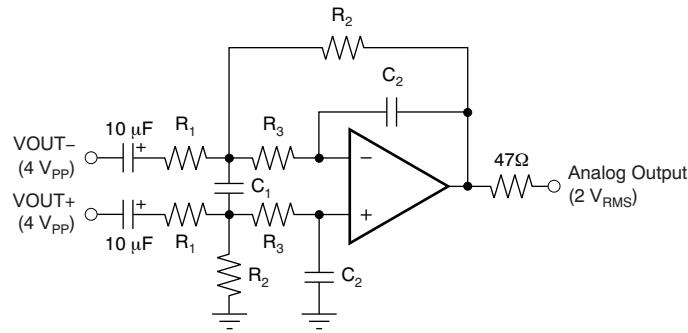
Amplifier is an NE5532A x1/2 or OPA2134 x1/2; R_1 = 7.5-kΩ resistor; R_2 = 5.6-kΩ resistor; R_3 = 360-Ω resistor; C_1 = 3300-pF capacitor; C_2 = 680-pF capacitor; Gain = 0.747; $f_{-3\ dB}$ = 53 kHz.

Figure 62. Post-LPF and Differential to Single-Ended Buffer for DAC Output (AC-Coupled)
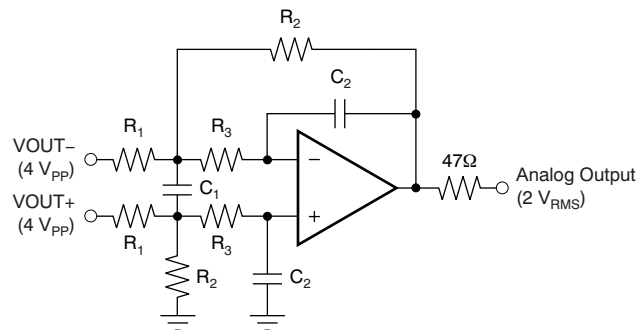
Amplifier is an NE5532A x1/2 or OPA2134 x1/2; R_1 = 15-kΩ resistor; R_2 = 11-kΩ resistor; R_3 = 820-Ω resistor; C_1 = 1500-pF capacitor; C_2 = 330-pF capacitor; Gain = 0.733; $f_{-3\ dB}$ = 54 kHz.

Figure 63. Post-LPF and Differential to Single-Ended Buffer for DAC Output (DC-Coupled)

Product Folder Link(s): *PCM3168A PCM3168A-Q1*

DESIGN AND LAYOUT CONSIDERATIONS

Power-Supply Pins (VCCAD1/2, VCCDA1/2, and VDD1/2)

The digital and analog power-supply pins of the PCM3168A and PCM3168A-Q1 should be bypassed to the corresponding ground pins with 1-μF ceramic capacitors placed as close to the pins as possible. Each power-supply line (VCC, VDD) to the PCM3168A and PCM3168A-Q1 should be bypassed to the corresponding ground pins with 10-μF electrolytic capacitors to maximize the dynamic performance of the ADC and DAC.

Although the PCM3168A and PCM3168A-Q1 have two power lines to maximize the potential of dynamic performance, using one common source (for instance, a +5-V power supply for VCC and a +3.3-V power supply for VDD generated from one common source) is recommended to avoid unexpected power-supply trouble such as latch-up or incorrect power-supply conditions. Also, simultaneous power-on/off of VCC and VDD is recommended to avoid unexpected transient responses in outputs, though the power-supply sequence of VCC and VDD is not specified in the operation and absolute maximum ratings point of view.

Grounding (AGNDAD1/2, AGNDDA1/2, and DGND1/2)

To maximize the dynamic performance of the PCM3168A and PCM3168A-Q1, the analog and digital grounds are not connected internally. These pins should have very low impedances to avoid digital noise and signal components feeding back into the analog ground. All ground pins should be connected directly to each other under the part, and the device should be connected to the analog ground of the application, as with acceptable analog layout practices; this layout reduces the potential of noise problems.

VIN1±, VIN2±, VIN3±, VIN4±, VIN5±, and VIN6± Pins

In case of direct interface to VINx±, 1-μF electrolytic capacitors are recommended because the ac-coupling capacitor (which gives a 2-Hz HPF corner frequency and 47 Ω and 0.1 μF to 470 Ω and 0.001 μF differential LPF) is recommended as the anti-aliasing filter that gives a 160-kHz LPF corner frequency. If signal source impedance is not enough (too low) or input line length to the VINx± is not enough (too short), insertion of an analog front-end buffer (see Figure 59 to Figure 61) is recommended to maximize the dynamic performance. The voltage coefficient of the capacitor for an anti-aliasing filter should be considered to maximize the THD performance. A film-type capacitor is recommended; if a ceramic capacitor is used, a relatively higher voltage type is recommended.

There are three ways to terminate any unused input pins. First, terminate these pins to AGNDAD with 0.001-μF to 1-μF capacitors. This termination is applied on unused pins whose channels are configured in single-ended mode. The second form of termination is to connect the positive (+) pin and negative (−) pins together and terminating these to AGNDAD with 0.001-μF to 1-μF capacitors. This option applies to unused pins with channels that are configured in differential mode. The last termination method is to terminat the pins directly to VCOMAD; this option can be applied on unused pins with unused channels combined into two channels that are then configured in power-save mode.

VCOMAD and VCOMDA Pins

10-μF electrolytic capacitors are recommended between VCOMAD and AGNDAD, and VCOMDA and AGNDDA to ensure a low source impedance of ADC and DAC common voltages. These capacitors should be located as close to each pin as possible to reduce dynamic errors on the ADC and DAC common voltages.

VREFAD1/2 Pins

10-μF electrolytic capacitors are recommended between VREFAD1/2 and AGNDAD to ensure low source impedances of ADC references. These capacitors should be located as close to each pin as possible to reduce dynamic errors on ADC references.

VOUT1±, VOU2±, VOUT3±, VOUT4±, VOUT5±, VOUT6±, VOU7±, and VOUT8± Pins

The differential to single-ended buffer with post LPF can be directly connected (without capacitors) to these output pins (see Figure 63), thereby minimizing the use of coupling capacitors for the 2-V_{RMS} outputs. The op amp and resistors should be determined with consideration of degrading some performance through this differential to single-ended and LPF buffer; there is about 1.5-dB degradation seen in the examples of Figure 62 and Figure 63.

MODE Pin

This pin is a logic input with quad-state input capability. The MODE pin is high when connected to VDD, low when connected to DGND, and pulled up or pulled down through an external resistor and for the two mid-states in order to distinguish the four input states. The pull-up or pull-down resistor must be 220 kΩ, ±5% in tolerance. Note that the state of the MODE pin is only sampled by a power-on or a low-to-high transition of the RST pin.

RST Pin

When the MODE pin setting changes to change the operating mode, the new mode setting does not take effect immediately; a RST pin toggle is required to make the new mode setting valid, and for the new mode to take effect.

OVF Pin

The OVF pin has two functions. It is primarily the flag for ADC overflow occurrence detection. It is also used to indicate that the internal reset sequence is complete and that the device is ready to enter serial mode control.

System Clock and Audio Interface Clocks

The quality of SCKI may influence dynamic performance, because the PCM3168A and PCM3168A-Q1 (both the ADC and DAC) operate based on SCKI. Therefore, it may be required to consider the jitter, duty, and rise/fall time of the system clock.

In slave mode, the PCM3168A and PCM3168A-Q1 do not require a specific timing relationship between BCKAD/LRCKAD and SCKI, and BCKDA/LRCKDA and SCKI; however, there is a possibility of performance degradation with a certain timing relationship between them. In that case, specific timing relationship control might resolve this performance degradation.

In master mode, there is a possibility of performance degradation because of heavy loads on BCKAD/LRCKAD, BCKDA/LRCKDA, and DOUT1/2/3. It is recommended to load these pins as lightly as possible. Note that all output clocks and signals go low; they do not go into a high-impedance state during power-save mode.

PowerPAD

The PowerPAD of the PCM3168A and PCM3168A-Q1 is internally connected to the substrate of the silicon. It should be connected to the ground plane with sufficient low conductance in electrical and thermal; see Figure 56. The PowerPAD size is 7,25 mm x 7,00 mm (0,725 cm × 0.7 cm).

External Mute Control

For power-down ON/OFF control without the pop-noise that is generated by a dc level change on the DAC output, the external mute control is generally required. Use of the following control sequence is recommended: external mute ON, codec power-down ON, SCKI stop and resume if necessary, codec power-down OFF, and external mute OFF control.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
PCM3168APAP	ACTIVE	HTQFP	PAP	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	PCM3168A	Samples
PCM3168APAPR	ACTIVE	HTQFP	PAP	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	PCM3168A	Samples
PCM3168APAPRG4	ACTIVE	HTQFP	PAP	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	PCM3168A	Samples
PCM3168ATPAPQ1	ACTIVE	HTQFP	PAP	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	PCM3168AQ1	Samples
PCM3168ATPAPRQ1	ACTIVE	HTQFP	PAP	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	PCM3168AQ1	Samples
PCM3168ATPAPRQ1G4	ACTIVE	HTQFP	PAP	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	PCM3168AQ1	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF PCM3168A, PCM3168A-Q1 :

- Catalog: PCM3168A

- Automotive: PCM3168A-Q1

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM3168APAPR	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2
PCM3168ATPAPRQ1	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM3168APAPR	HTQFP	PAP	64	1000	367.0	367.0	45.0
PCM3168ATPAPRQ1	HTQFP	PAP	64	1000	367.0	367.0	45.0

PAP (S−PQFP−G64)   PowerPAD ™ PLASTIC QUAD FLATPACK

Thermal Pad
(See Note D)

0,50
0,27
0,17
⊕ 0,08 Ⓜ

48   33

49   32

64   17

1   16

7,50 TYP

10,20
9,80 SQ

12,20
11,80 SQ

1,05
0,95

1,20 MAX

Seating Plane

⌔ 0,08

0,13 NOM

Gage Plane

0,25

0,15
0,05

0,75
0,45

0°−7°

4147702/C 08/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion
         D.   This package is designed to be soldered to a thermal pad on the board.   Refer to Technical Brief, PowerPad
              Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding
              recommended board layout.   This document is available at www.ti.com <http://www.ti.com>.

         E.   Falls within JEDEC MS−026

PowerPAD is a trademark of Texas Instruments.

PAP (S−PQFP−G64)   PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

Exposed Thermal Pad Dimensions

4206326−9/0 10/13

NOTES: A. All linear dimensions are in millimeters

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PAP (S−PQFP−G64) PowerPAD™ PLASTIC QUAD FLATPACK

Example Board Layout
Via pattern and copper area under solder mask
may vary depending on layout constraints

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).
Reference table below for other
solder stencil thicknesses

36x⌀0,3
Centered
on Pad

60x0,5

1,3

1,3

7,26 8,0 11,2

7,00
8,0
11,2

Solder Mask
Over Copper

Pin 1

Solder Mask
Defined Pad
(See Note C, D)

64x1,55 60x0,5

64x0,25

Pin 1

7,26 Y

7,00

X

11,2

11,2

(See Note E)

Example
Solder Mask Opening
(See Note F)

0,3

1,6

0,05
All Around

Example
Pad Geometry

CENTER POWER PAD SOLDER STENCIL OPENING		
STENCIL THICKNESS	X	Y
0.1mm	7.50	7.7
0.127mm	7.00	7.26
0.152mm	6.60	6.8
0.178mm	6.20	6.4

4208775−9/F 09/10

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad
Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets
for specific thermal information, via requirements, and recommended board layout. These documents are available at
www.ti.com <http://www.ti.com>. Publication IPC−7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
metal load solder paste. Refer to IPC−7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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