SoundPlus™ High-Performance, JFET-Input AUDIO OPERATIONAL AMPLIFIERS

Check for Samples: OPA1641, OPA1642, OPA1644

FEATURES

- **SUPERIOR SOUND QUALITY**
- **TRUE JFET INPUT OP AMP WITH LOW INPUT BIAS CURRENT**
- **LOW NOISE: 5.1nV/√Hz at 1kHz**
- **ULTRALOW DISTORTION: 0.00005% at 1kHz**
- **HIGH SLEW RATE: 20V/μs**
- **UNITY GAIN STABLE**
- **NO PHASE REVERSAL**
- **LOW QUIESCENT CURRENT: 1.8mA per Channel**
- **RAIL-TO-RAIL OUTPUT**
- **WIDE SUPPLY RANGE: ±2.25V to ±18V**
- **SINGLE, DUAL, AND QUAD VERSIONS AVAILABLE**

APPLICATIONS

- **PROFESSIONAL AUDIO EQUIPMENT**
- **ANALOG AND DIGITAL MIXING CONSOLES**
- **BROADCAST STUDIO EQUIPMENT**
- **HIGH-END A/V RECEIVERS**
- **HIGH-END BLU-RAY™ PLAYERS**

DESCRIPTION

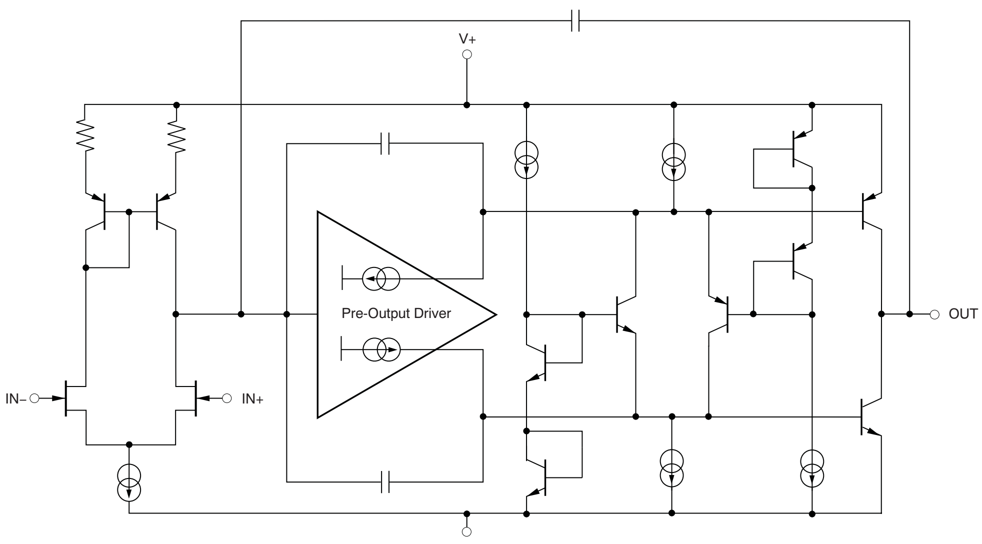
The OPA1641 (single), OPA1642 (dual), and OPA1644 (quad) series are JFET-input, ultralow distortion, low-noise operational amplifiers fully specified for audio applications.

The OPA1641, OPA1642, and OPA1644 rail-to-rail output swing allows increased headroom, making these devices ideal for use in any audio circuit. Features include 5.1nV/√Hz noise, low THD+N (0.00005%), a low input bias current of 2pA, and low quiescent current of 1.8mA per channel.

These devices operate over a very wide supply voltage range of ±2.25V to ±18V. The OPA1641, OPA1642, and OPA1644 series of op amps are unity-gain stable and provide excellent dynamic behavior over a wide range of load conditions.

The dual and quad versions feature completely independent circuitry for lowest crosstalk and freedom from interactions between channels, even when overdriven or overloaded.

The OPA1641, OPA1642, and OPA1644 are specified from –40°C to +85°C.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		VALUE	UNIT
Supply Voltage, V_S = (V+) – (V–)		40	V
Input Voltage(2)		(V–) –0.5 to (V+) +0.5	V
Input Current(2)		±10	mA
Differential Input Voltage		$\pm V_S$	V
Output Short-Circuit(3)		Continuous	
Operating Temperature, T_A		–55 to +125	°C
Storage Temperature, T_A		–65 to +150	°C
Junction Temperature, T_J		+150	°C
ESD Ratings	Human Body Model (HBM)	3000	V
	Charged Device Model (CDM)	1000	V
	Machine Model (MM)	100	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less.
(3) Short-circuit to $V_S/2$ (ground in symmetrical dual-supply setups), one amplifier per package.

PACKAGE INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA1641	SO-8	D	O1641A
	MSOP-8	DGK	1641
OPA1642	SO-8	D	O1642A
	MSOP-8	DGK	1642
OPA1644	SO-14	D	O1644AG4
	TSSOP-14	PW	O1644A

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ELECTRICAL CHARACTERISTICS: V_S = +4.5V to +36; ±2.25V to ±18V

At T_A = +25°C, R_L = 2kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		CONDITIONS	OPA1641, OPA1642, OPA1644 MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE						
Total Harmonic Distortion + Noise	THD+N	G = +1, f = 1kHz, V_O = $3V_{RMS}$		0.00005		%
				–126		dB
Intermodulation Distortion	IMD	G = +1, V_O = $3V_{RMS}$				
		SMPTE/DIN Two-Tone, 4:1 (60Hz and 7kHz)		0.00004		%
				–128		dB
		DIM 30 (3kHz square wave and 15kHz sine wave)		0.00008		%
				–122		dB
		CCIF Twin-Tone (19kHz and 20kHz)		0.00007		%
				–123		dB
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW	G = +1		11		MHz
Slew Rate	SR	G = +1		20		V/μs
Full-Power Bandwidth(1)		V_O = $1V_P$		3.2		MHz
Overload Recovery Time(2)		G = –10		600		ns
Channel Separation (Dual and Quad)		f = 1kHz		–126		dB
NOISE						
Input Voltage Noise		f = 20Hz to 20kHz		4.3		μV_{PP}
Input Voltage Noise Density	e_n	f = 10Hz		8		$nV/\sqrt{Hz}$
		f = 100Hz		5.8		$nV/\sqrt{Hz}$
		f = 1kHz		5.1		$nV/\sqrt{Hz}$
Input Current Noise Density	I_n	f = 1kHz		0.8		$fA/\sqrt{Hz}$
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = ±18V		1	3.5	mV
vs Power Supply	PSRR	V_S = ±2.25V to ±18V		0.14	2	μV/V
INPUT BIAS CURRENT						
Input Bias Current	I_B	V_{CM} = 0V		±2	±20	pA
Input Offset Current	I_{OS}	V_{CM} = 0V		±2	±20	pA
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V–)-0.1		(V+)–3.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = (V–) – 0.1V to (V+) – 3.5V, V_S = ±18V	120	126		dB
INPUT IMPEDANCE						
Differential				10^{13} ǁ 8		Ω ǁ pF
Common-Mode		V_{CM} = (V–) – 0.1V to (V+) – 3.5V		10^{13} ǁ 6		Ω ǁ pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	(V–) + 0.2V ≤ V_O ≤ (V+) – 0.2V, R_L = 10kΩ	120	134		dB
		(V–) + 0.35V ≤ V_O ≤ (V+) – 0.35V, R_L = 2kΩ	114	126		dB

(1) Full power bandwidth = SR/(2π × V_P), where SR = slew rate.
(2) See Figure 21 and Figure 22.

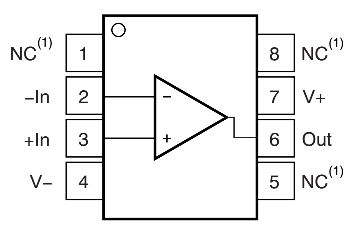
ELECTRICAL CHARACTERISTICS: V_S = +4.5V to +36; ±2.25V to ±18V (continued)

At T_A = +25°C, R_L = 2kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		CONDITIONS	OPA1641, OPA1642, OPA1644			UNIT
			MIN	TYP	MAX	
OUTPUT						
Voltage Output Swing from Rail	V_O	R_L = 10kΩ, A_{OL} ≥ 120dB	(V–)+0.2		(V+)–0.2	V
		R_L = 2kΩ, A_{OL} ≥ 114dB	(V–)+0.35		(V+)–0.35	V
Output Current	I_{OUT}		See Typical Characteristics			
Open-Loop Output Impedance	Z_O		See Typical Characteristics			Ω
Short-Circuit Current	I_{SC}	Source		+36		mA
	I_{SC}	Sink		–30		mA
Capacitive Load Drive	C_{LOAD}		See Typical Characteristics			
POWER SUPPLY						
Specified Voltage	V_S		±2.25		±18	V
Quiescent Current (per amplifier)	I_Q	I_{OUT} = 0A		1.8	2.3	mA
TEMPERATURE RANGE						
Specified Range			–40		+85	°C
Operating Range			–55		+125	°C
Thermal Resistance	θ_{JA}					
SO-8				138		°C/W
MSOP-8				180		°C/W
SO-14				97		°C/W
TSSOP-14				135		°C/W

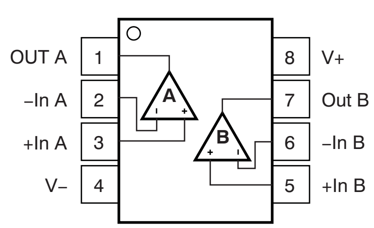
PIN ASSIGNMENTS

OPA1641
SO-8, MSOP-8
(TOP VIEW)

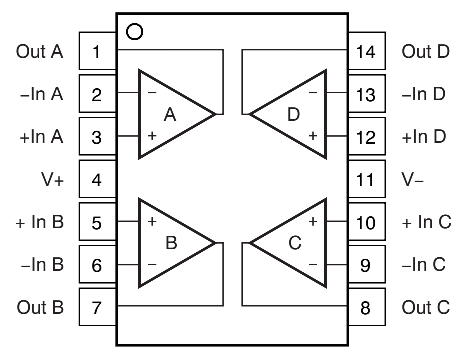


(1) NC denotes no internal connection.

OPA1642
SO-8, MSOP-8
(TOP VIEW)



OPA1644
SO-14, TSSOP-14
(TOP VIEW)



TYPICAL CHARACTERISTICS: V_S = ±18V

At T_A = +25°C, R_L = 2kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

INPUT VOLTAGE NOISE DENSITY vs FREQUENCY

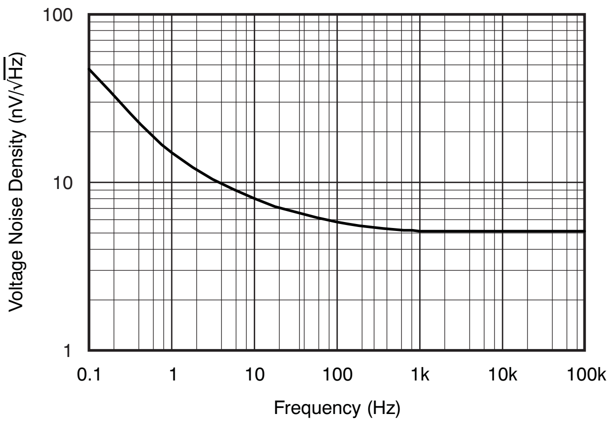


Figure 1.

0.1Hz to 10Hz NOISE

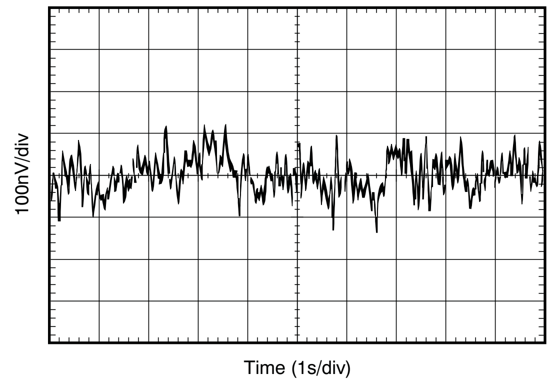


Figure 2.

MAXIMUM OUTPUT VOLTAGE vs FREQUENCY

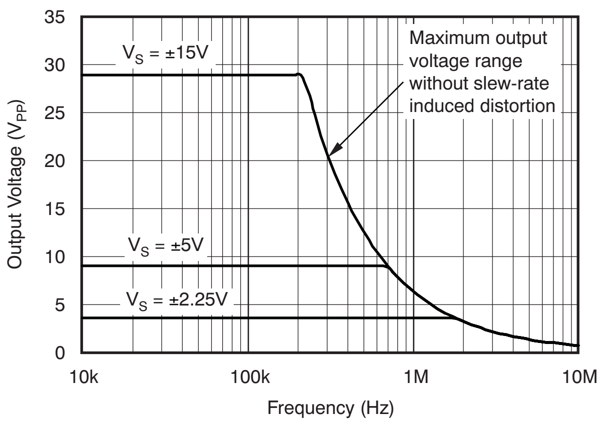


Figure 3.

CMRR AND PSRR vs FREQUENCY (Referred to Input)

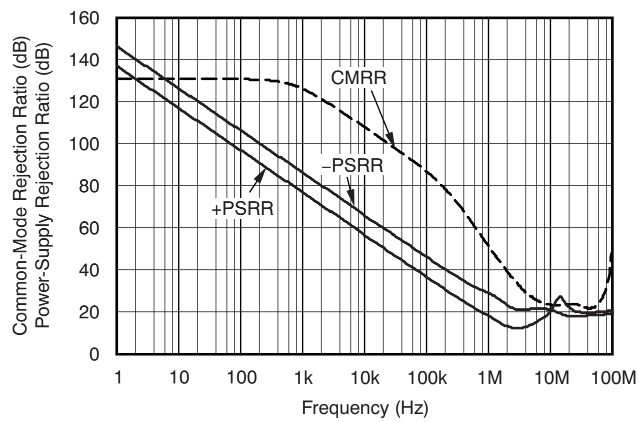


Figure 4.

GAIN AND PHASE vs FREQUENCY

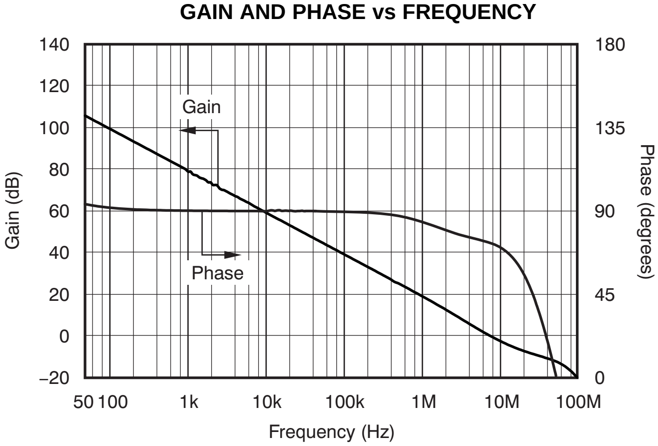


Figure 5.

CLOSED-LOOP GAIN vs FREQUENCY

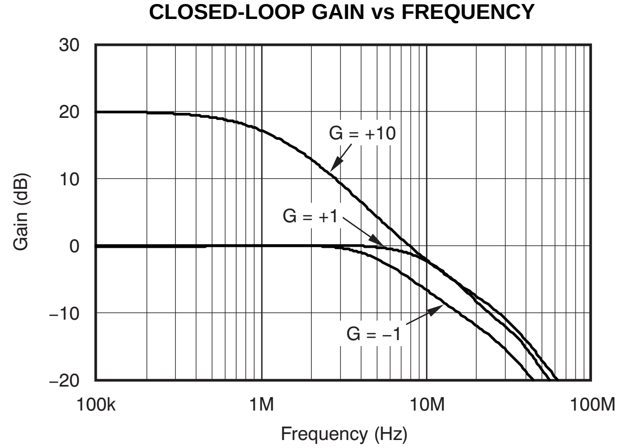


Figure 6.

TYPICAL CHARACTERISTICS: V_S = ±18V (continued)

At T_A = +25°C, R_L = 2kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

THD+N RATIO vs FREQUENCY

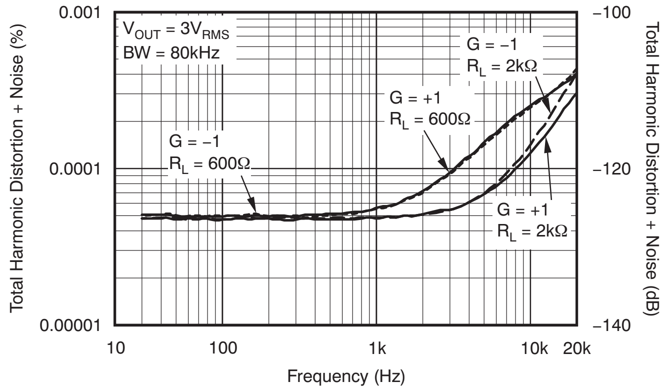


Figure 7.

THD+N RATIO vs FREQUENCY

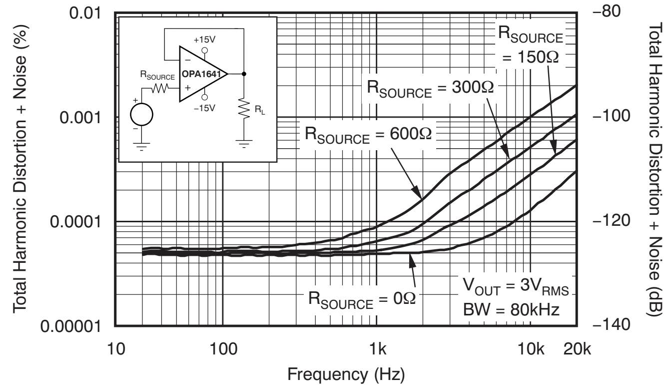


Figure 8.

THD+N RATIO vs FREQUENCY

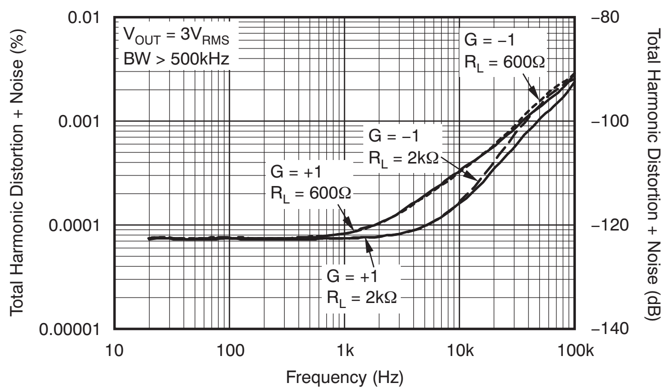


Figure 9.

THD+N RATIO vs FREQUENCY

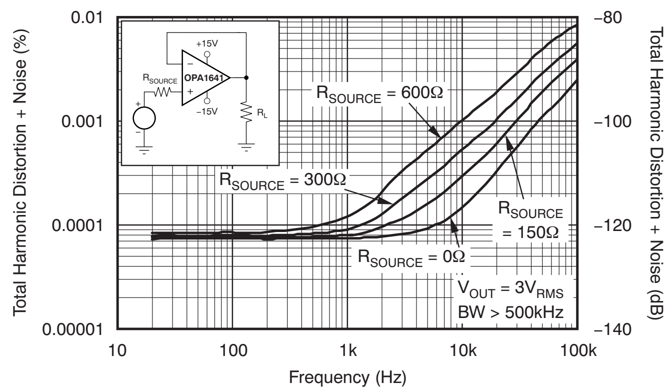


Figure 10.

THD+N RATIO vs OUTPUT AMPLITUDE

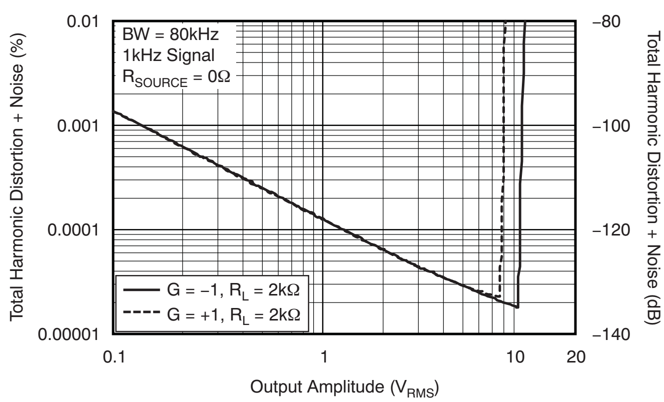


Figure 11.

INTERMODULATION DISTORTION vs OUTPUT AMPLITUDE

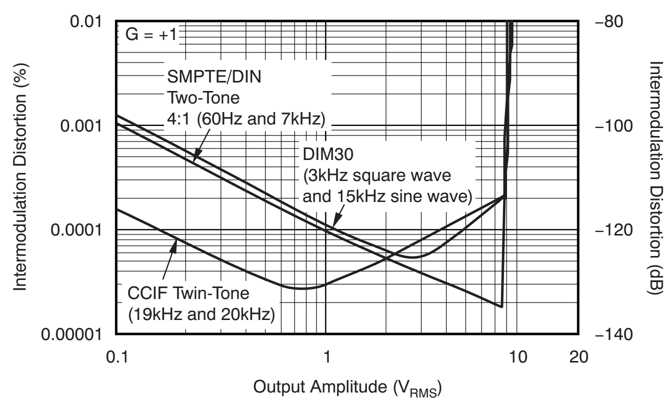


Figure 12.

TYPICAL CHARACTERISTICS: V_S = ±18V (continued)

At T_A = +25°C, R_L = 2kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

CHANNEL SEPARATION vs FREQUENCY

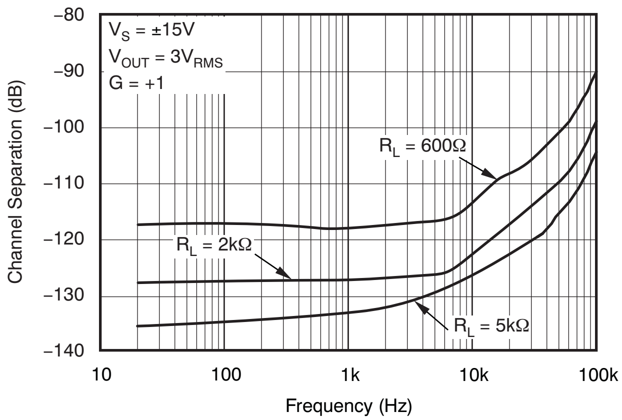


Figure 13.

NO PHASE REVERSAL

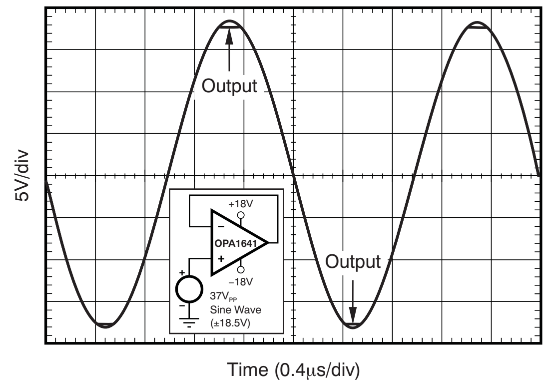


Figure 14.

SMALL-SIGNAL STEP RESPONSE (100mV)

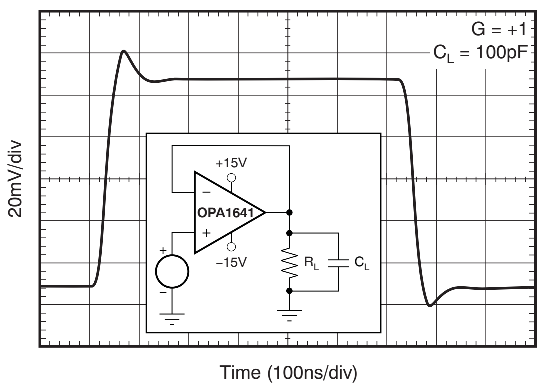


Figure 15.

SMALL-SIGNAL STEP RESPONSE (100mV)

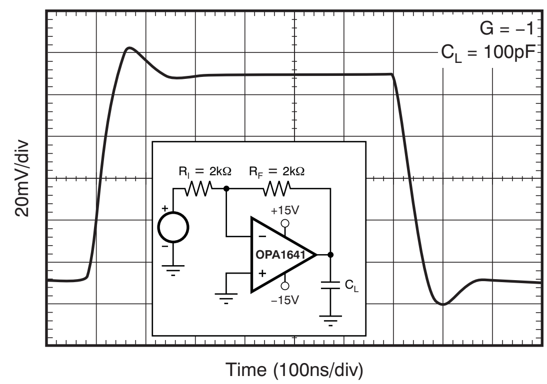


Figure 16.

LARGE-SIGNAL STEP RESPONSE

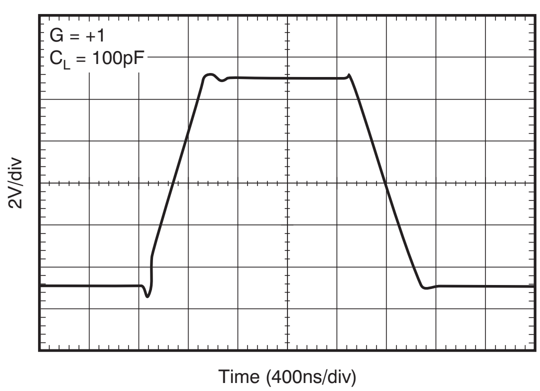


Figure 17.

LARGE-SIGNAL STEP RESPONSE

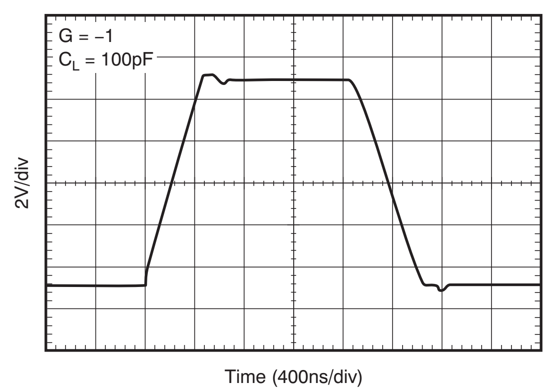


Figure 18.

TYPICAL CHARACTERISTICS: V_S = ±18V (continued)

At T_A = +25°C, R_L = 2kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

POSITIVE OVERLOAD RECOVERY

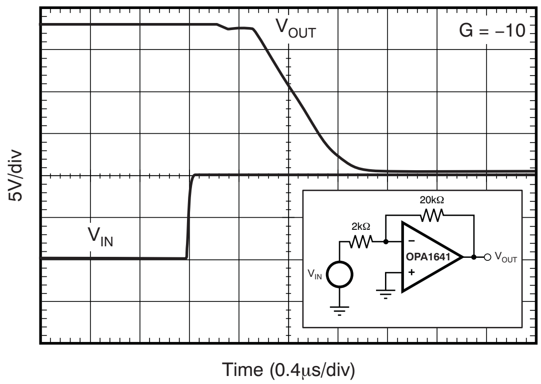


Figure 19.

NEGATIVE OVERLOAD RECOVERY

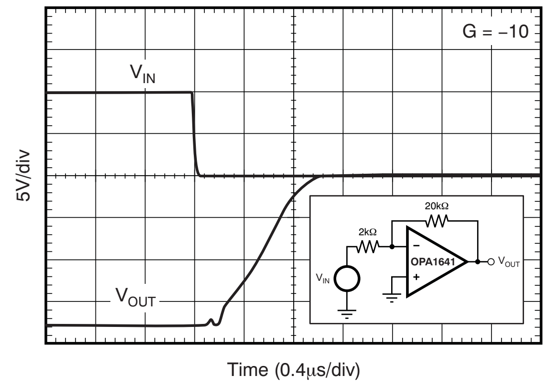


Figure 20.

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD (100mV Output Step)

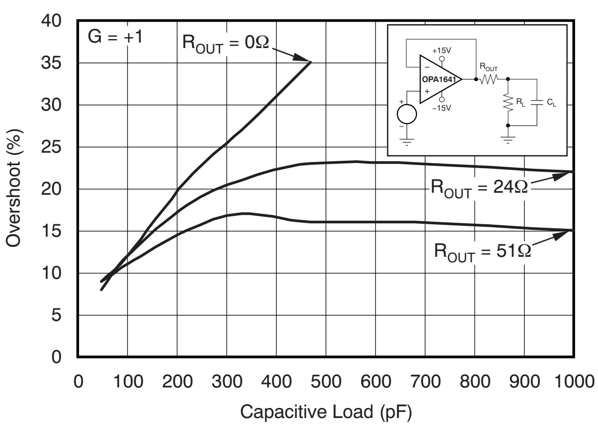


Figure 21.

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD (100mV Output Step)

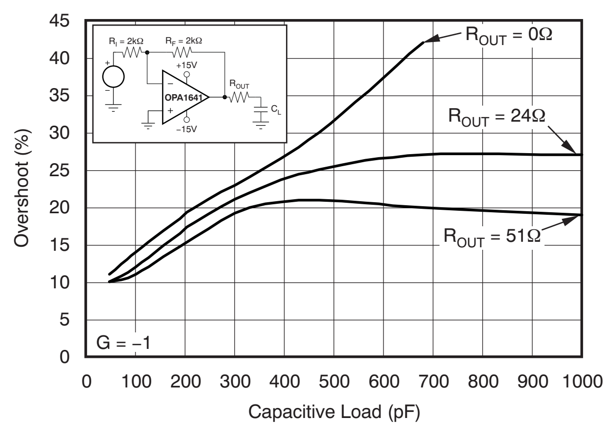


Figure 22.

OPEN-LOOP GAIN vs TEMPERATURE

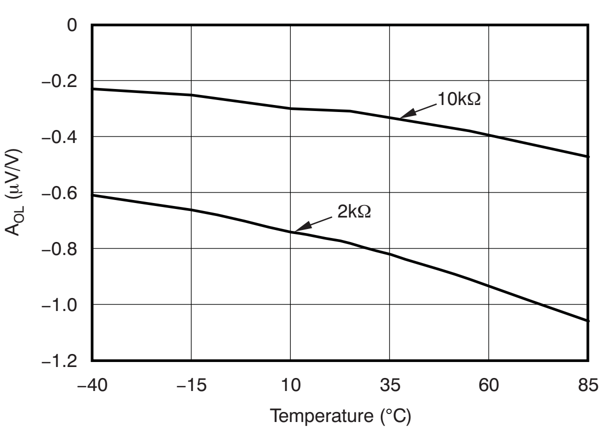


Figure 23.

I_B AND I_{OS} vs TEMPERATURE

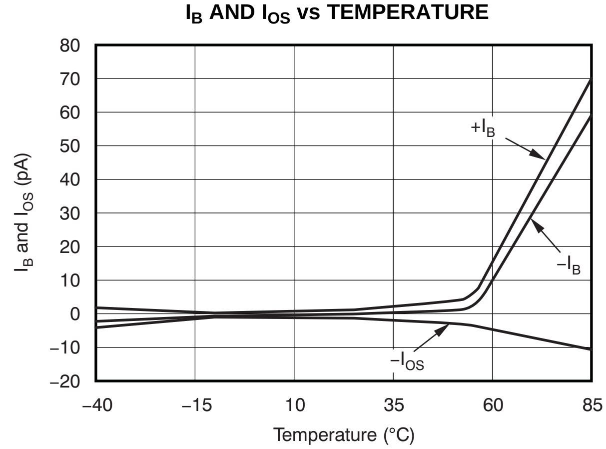


Figure 24.

TYPICAL CHARACTERISTICS: V_S = ±18V (continued)

At T_A = +25°C, R_L = 2kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

I_B AND I_{OS} vs COMMON-MODE VOLTAGE

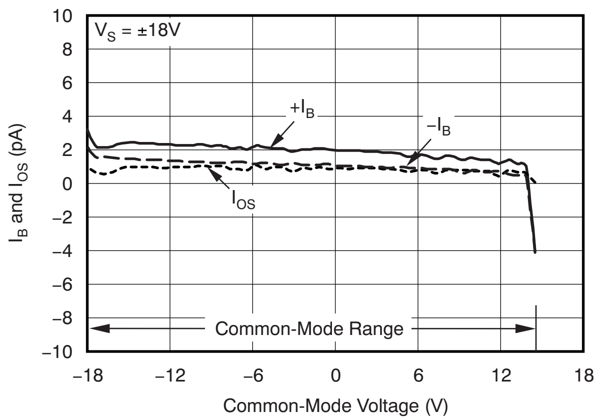


Figure 25.

QUIESCENT CURRENT vs TEMPERATURE

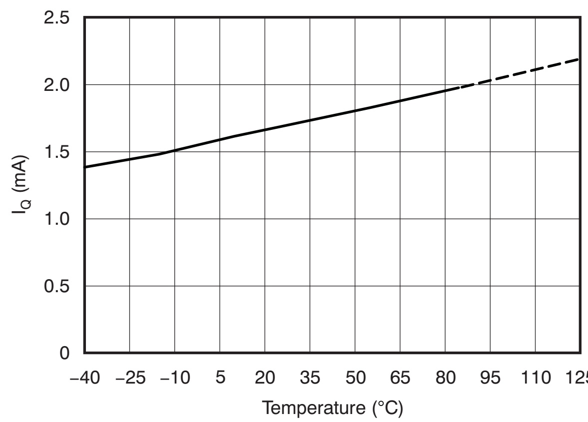


Figure 26.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

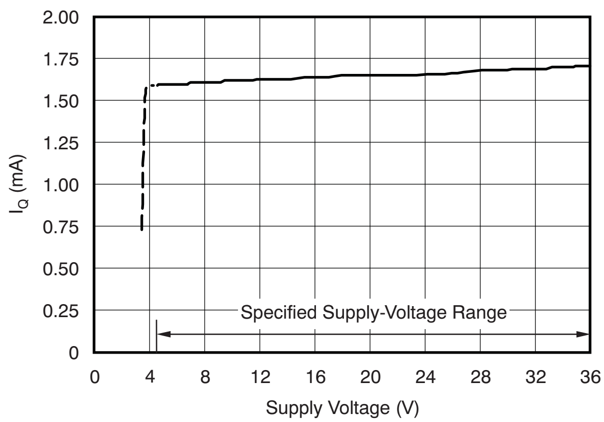


Figure 27.

SHORT-CIRCUIT CURRENT vs TEMPERATURE

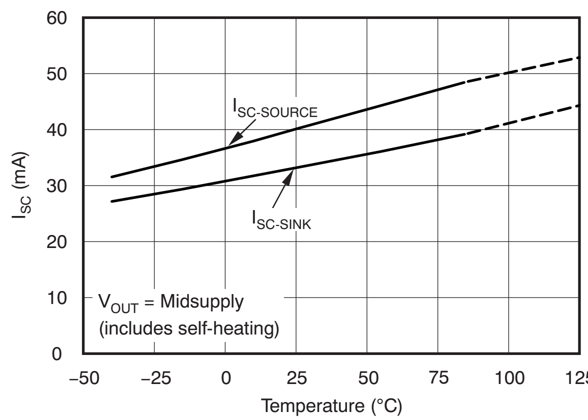


Figure 28.

OUTPUT VOLTAGE vs OUTPUT CURRENT

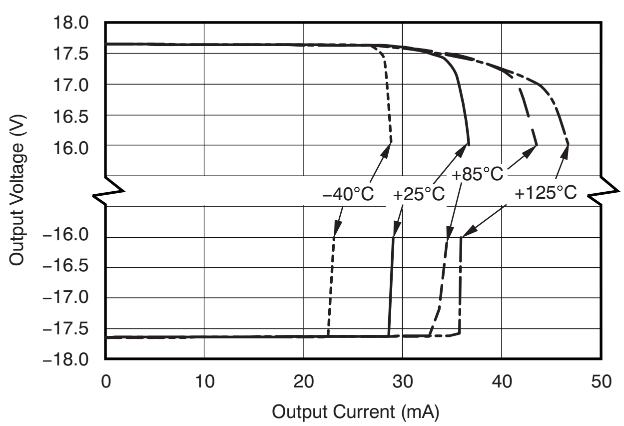


Figure 29.

OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY

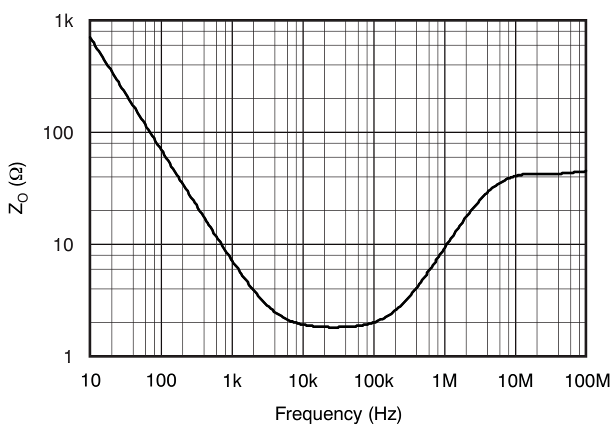


Figure 30.

APPLICATION INFORMATION

The OPA1641, OPA1642, and OPA1644 are unity-gain stable, audio operational amplifiers with very low noise, input bias current, and input offset voltage. Applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1μF capacitors are adequate. The front-page drawing shows a simplified schematic of the OPA1641.

OPERATING VOLTAGE

The OPA1641, OPA1642, and OPA1644 series of op amps can be used with single or dual supplies from an operating range of V_S = +4.5V (±2.25V) and up to V_S = +36V (±18V). These devices do not require symmetrical supplies; it only requires a minimum supply voltage of +4.5V (±2.25V). For V_S less than ±3.5V, the common-mode input range does not include midsupply. Supply voltages higher than +40V can permanently damage the device; see Absolute Maximum Ratings table. Key parameters are specified over the operating temperature range, T_A = –40°C to +85°C. Key parameters that vary over the supply voltage or temperature range are shown in the Typical Characteristics section of this data sheet.

NOISE PERFORMANCE

Figure 31 shows the total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (with no feedback resistor network and therefore no additional noise contributions). The OPA1641, OPA1642, and OPA1644 are shown with total circuit noise calculated. The op amp itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The OPA1641, OPA1642, and OPA1644 family has both low voltage noise and extremely low current noise because of the FET input of the op amp. As a result, the current noise contribution of the OPA164x series is negligible for any practical source impedance, which makes it the better choice for applications with high source impedance.

The equation in Figure 31 shows the calculation of the total circuit noise, with these parameters:

- e_n = voltage noise
- I_n = current noise
- R_S = source impedance
- k = Boltzmann's constant = 1.38 × 10^{-23} J/K
- T = temperature in degrees Kelvin (K)

For more details on calculating noise, see the next section on Basic Noise Calculations.

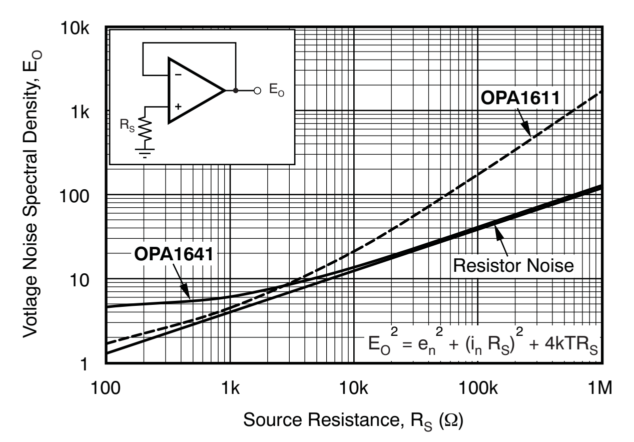


Figure 31. Noise Performance of the OPA1611 and OPA1641 in Unity-Gain Buffer Configuration

BASIC NOISE CALCULATIONS

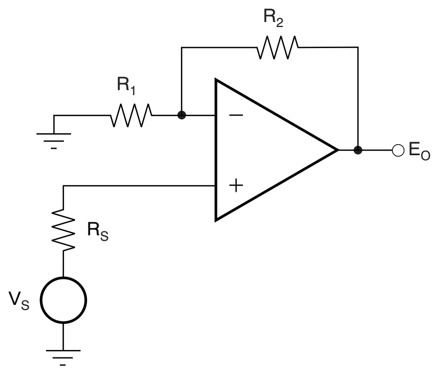
Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on overall op amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in Figure 31. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 32 illustrates both noninverting (A) and inverting (B) op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. In general, the current noise of the op amp reacts with the feedback resistors to create additional noise components. However, the extremely low current noise of the OPA164x means that its current noise contribution can be neglected.

The feedback resistor values can generally be chosen to make these noise sources negligible. Note that low impedance feedback resistors will load the output of the amplifier. The equations for total noise are shown for both configurations.

A) Noise in Noninverting Gain Configuration



Noise at the output:

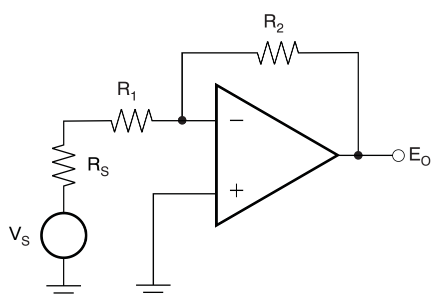
$$E_O^2 = \left[1 + \frac{R_2}{R_1}\right]^2 e_n^2 + \left[\frac{R_2}{R_1}\right]^2 e_1^2 + e_2^2 + \left[1 + \frac{R_2}{R_1}\right]^2 e_s^2$$

Where $e_S = \sqrt{4kTR_S}$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1}$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

B) Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left[1 + \frac{R_2}{R_1 + R_S}\right]^2 e_n^2 + \left[\frac{R_2}{R_1 + R_S}\right]^2 e_1^2 + e_2^2 + \left[\frac{R_2}{R_1 + R_S}\right]^2 e_s^2$$

Where $e_S = \sqrt{4kTR_S}$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1}$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

For the OPA164x series op amps at 1kHz, $e_n = 5.1\text{nV}/\sqrt{\text{Hz}}$

Figure 32. Noise Calculation in Gain Configurations

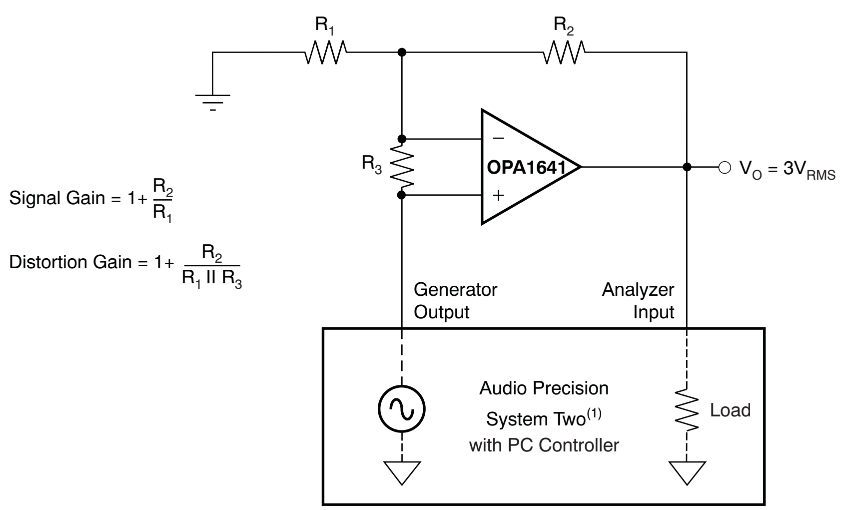
TOTAL HARMONIC DISTORTION MEASUREMENTS

The OPA164x series op amps have excellent distortion characteristics. THD + Noise is below 0.00005% (G = +1, V_O = $3V_{RMS}$, BW = 80kHz) throughout the audio frequency range, 20Hz to 20kHz, with a 2kΩ load (see Figure 7 for characteristic performance).

The distortion produced by the OPA164x series op amps is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit (such as Figure 33 shows) can be used to extend the measurement capabilities.

Op amp distortion can be considered an internal error source that can be referred to the input. Figure 33 shows a circuit that causes the op amp distortion to be 101 times (or approximately 40dB) greater than that normally produced by the op amp. The addition of R_3 to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101, thus extending the resolution by 101. Note that the input signal and load applied to the op amp are the same as with conventional feedback without R_3. The value of R_3 should be kept small to minimize its effect on the distortion measurements.

Validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an Audio Precision System Two distortion/noise analyzer, which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.



SIGNAL GAIN	DISTORTION GAIN	R_1	R_2	R_3
1	101	∞	1kΩ	10Ω
11	101	100Ω	1kΩ	11Ω

(1) For measurement bandwidth, see Figure 7 through Figure 12.

Figure 33. Distortion Test Circuit

SOURCE IMPEDANCE AND DISTORTION

For lowest distortion with a source or feedback network, the impedance seen by the positive and negative inputs in noninverting applications should be matched. The n-channel JFETs in the FET input stage exhibit a varying input capacitance with applied common-mode input voltage. In inverting configurations, the input does not vary with input voltage because the inverting input is held at virtual ground. However, in noninverting applications, the inputs do vary, and the gate-to-source voltage is not constant. This effect produces increased distortion as a result of the varying capacitance for unmatched source impedances.

To maintain low distortion, match unbalanced source impedance with appropriate values in the feedback network as shown in Figure 34. Of course, the unbalanced impedance may be from gain-setting resistors in the feedback path. If the parallel combination of R_1 and R_2 is greater than 2kΩ, a matching impedance on the noninverting input should be used. As always, resistor values should be minimized to reduce the effects of thermal noise.

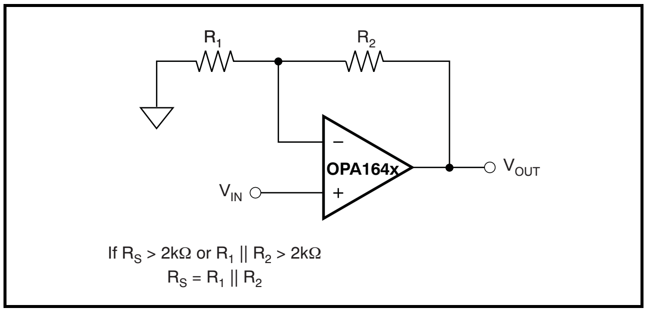


Figure 34. Impedance Matching for Maintaining Low Distortion in Noninverting Circuits

CAPACITIVE LOAD AND STABILITY

The dynamic characteristics of the OPA164x have been optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (R_{OUT} equal to 50Ω, for example) in series with the output.

Figure 21 and Figure 22 illustrate graphs of *Small-Signal Overshoot vs Capacitive Load* for several values of R_{OUT}. Also, refer to Applications Bulletin AB-028 (literature number SBOA015, available for download from the TI web site) for details of analysis techniques and application circuits.

PHASE-REVERSAL PROTECTION

The OPA1641, OPA1642, and OPA1644 family has internal phase-reversal protection. Many FET- and bipolar-input op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input circuitry of the OPA1641, OPA1642, and OPA1644 prevents phase reversal with excessive common-mode voltage; instead, the output limits into the appropriate rail (see Figure 14).

OUTPUT CURRENT LIMIT

The output current of the OPA164x series is limited by internal circuitry to +36mA/–30mA (sourcing/sinking), to protect the device if the output is accidentally shorted. This short-circuit current depends on temperature, as shown in Figure 28.

Although it is uncommon for most modern audio applications to require 600Ω load drive capability, many audio op amp applications continue to specify the total harmonic distortion (THD+N) at 600Ω load for comparative purposes. Figure 7 and Figure 9 provide typical THD+N measurement curves for the OPA164x series, where the output drives a $3V_{RMS}$ signal into a 600Ω load. However, it should be noted that correct device operation cannot be ensured when driving 600Ω loads at full supply. Depending on supply voltage and temperature, it may well trigger the output current limit circuitry of the device.

POWER DISSIPATION AND THERMAL PROTECTION

The OPA164x series of op amps are capable of driving 2kΩ loads with power-supply voltages of up to ±18V over the specified temperature range. In a single-supply configuration, where the load is connected to the negative supply voltage, the minimum load resistance is 2.8kΩ at a supply voltage of +36V. For lower supply voltages (either single-supply or symmetrical supplies), a lower load resistance may be used, as long as the output current does not exceed 13mA; otherwise, the device short-circuit current protection circuit may activate.

Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the OPA1641, OPA1642, and OPA1644 series devices improves heat dissipation compared to conventional materials. PCB layout can also help reduce a possible increase in junction temperature. Wide copper traces help dissipate the heat by acting as an additional heatsink. Temperature rise can be further minimized by soldering the devices directly to the PCB rather than using a socket.

Although the output current is limited by internal protection circuitry, accidental shorting of one or more output channels of a device can result in excessive heating. For instance, when an output is shorted to mid-supply, the typical short-circuit current of 36mA leads to an internal power dissipation of over 600mW at a supply of ±18V. In case of a dual OPA1642 in an MSOP-8 package (thermal resistance θ_{JA} = 180°C/W), such a power dissipation would lead the die temperature to be 220°C above ambient temperature, when both channels are shorted. This temperature increase would destroy the device.

In order to prevent such excessive heating that can destroy the device, the OPA164x series has an internal thermal shutdown circuit, which shuts down the device if the die temperature exceeds approximately +180°C. Once this thermal shutdown circuit activates, a built-in hysteresis of 15°C ensures that the die temperature must drop to about +165°C before the device switches on again.

ELECTRICAL OVERSTRESS

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. Figure 35 illustrates the ESD circuits contained in the OPA164x series (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA164x but below the device breakdown voltage level. Once this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

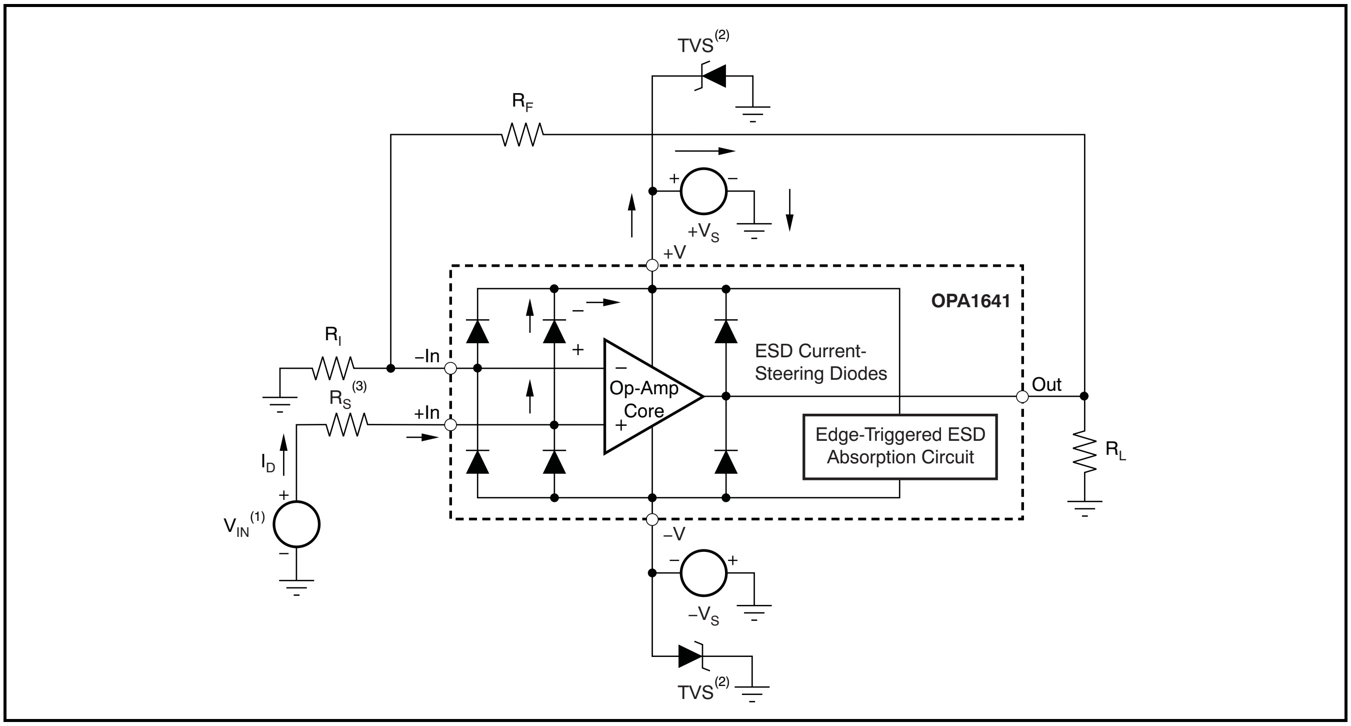
When the operational amplifier connects into a circuit such as the one Figure 35 shows, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

Figure 35 depicts a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the datasheet specifications recommend that applications limit the input current to 10mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ and/or $–V_S$ are at 0V. Again, it depends on the supply characteristic while at 0V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source via the current steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins as shown in Figure 35. The zener voltage must be selected such that the diode does not turn on during normal operation. However, its zener voltage should be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.



(1) $V_{IN} = +V_S + 500mV$.

(2) TVS: $+V_{S(max)} > V_{TVSBR\ (Min)} > +V_S$

(3) Suggested value approximately 1kΩ.

Figure 35. Equivalent Internal ESD Circuitry and Its Relation to a Typical Circuit Application

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April, 2010) to Revision B **Page**

- Removed product-preview information for MSOP-8 package version of OPA1641 2

Changes from Original (December, 2009) to Revision A **Page**

- Removed product-preview information for OPA1644 device packages throughout document 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
OPA1641AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA1641AIDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
OPA1641AIDGKT	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
OPA1641AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA1642AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA1642AIDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
OPA1642AIDGKT	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
OPA1642AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA1644AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA1644AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA1644AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA1644AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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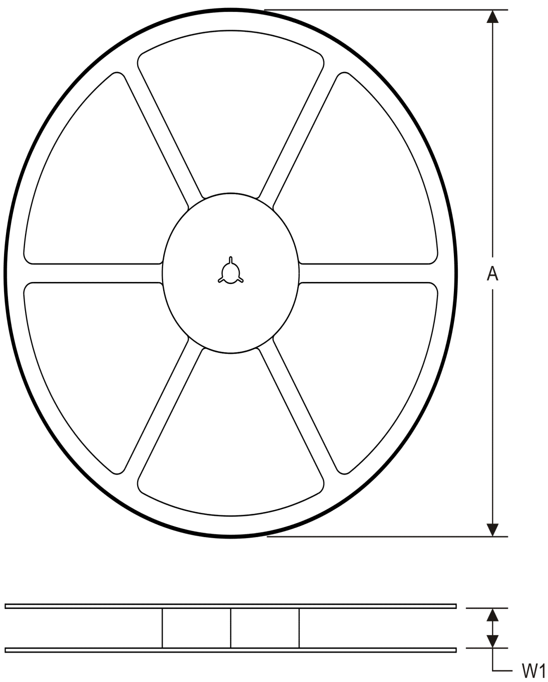
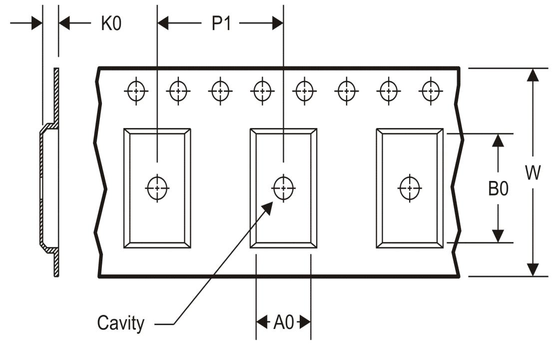
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



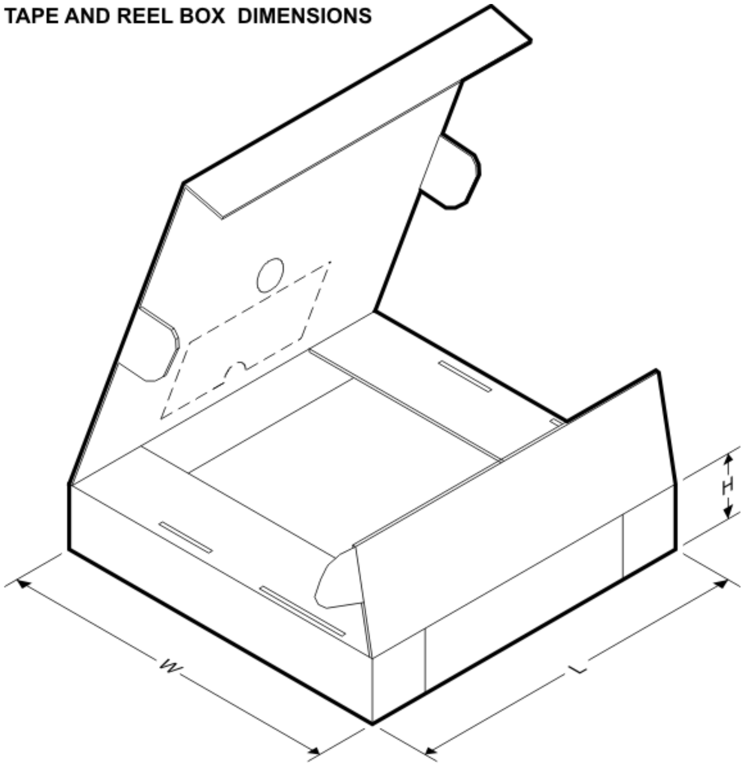
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA1641AIDGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA1641AIDGKT	MSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA1641AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA1642AIDGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA1642AIDGKT	MSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA1642AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA1644AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA1644AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

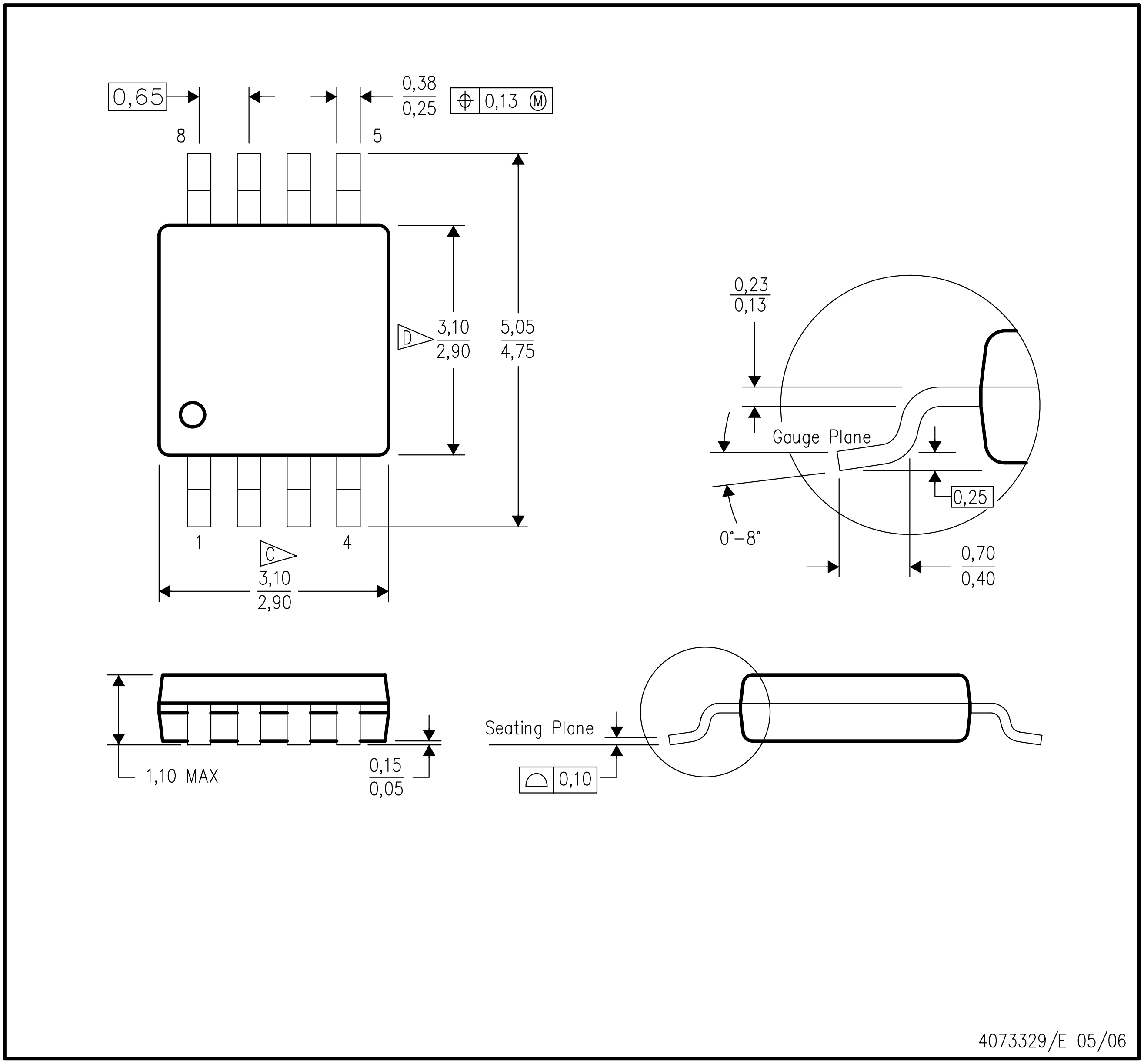
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

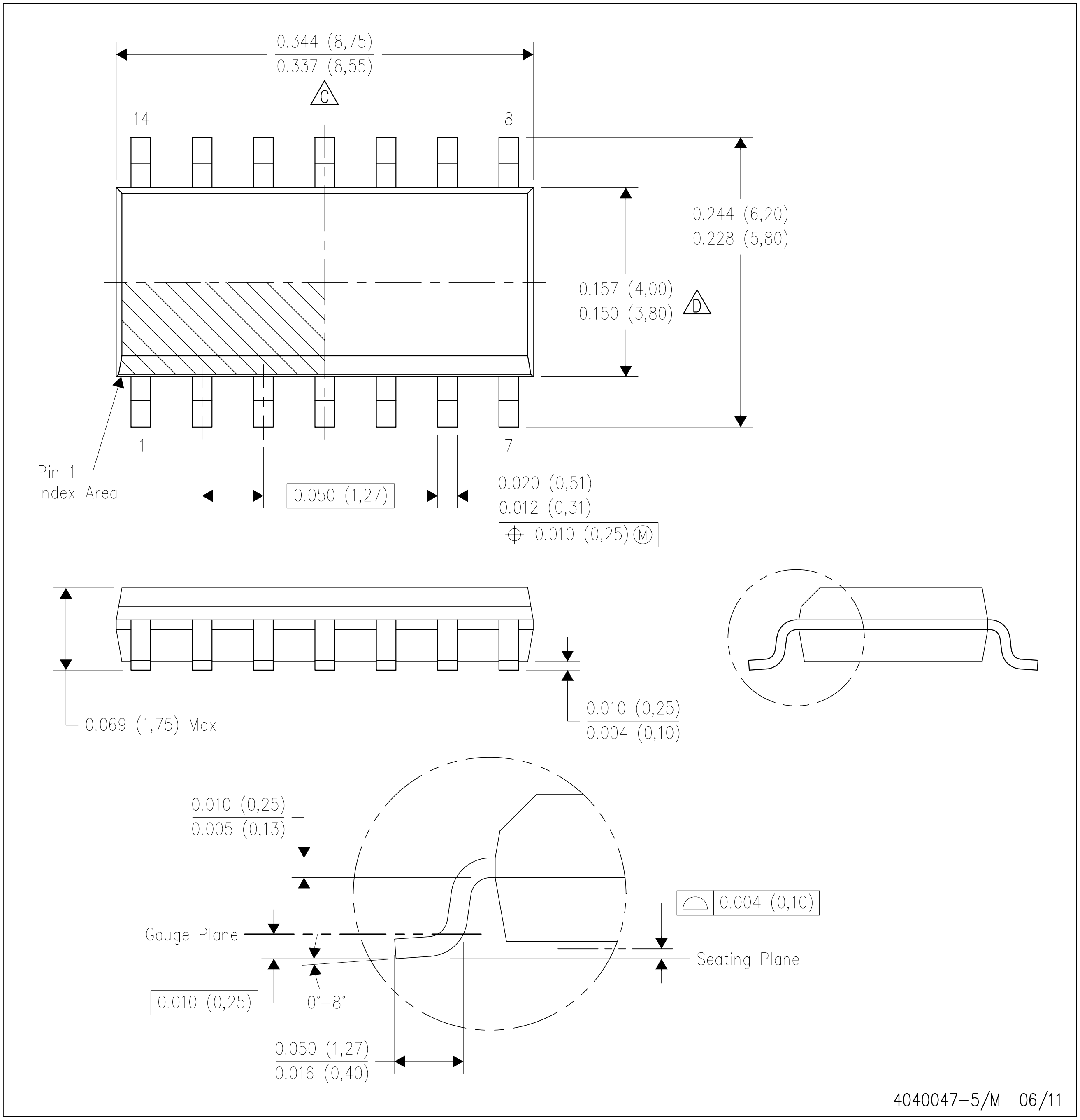
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA1641AIDGKR	MSOP	DGK	8	2500	346.0	346.0	29.0
OPA1641AIDGKT	MSOP	DGK	8	250	210.0	185.0	35.0
OPA1641AIDR	SOIC	D	8	2500	346.0	346.0	29.0
OPA1642AIDGKR	MSOP	DGK	8	2500	346.0	346.0	29.0
OPA1642AIDGKT	MSOP	DGK	8	250	210.0	185.0	35.0
OPA1642AIDR	SOIC	D	8	2500	346.0	346.0	29.0
OPA1644AIDR	SOIC	D	14	2500	346.0	346.0	33.0
OPA1644AIPWR	TSSOP	PW	14	2000	346.0	346.0	29.0

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



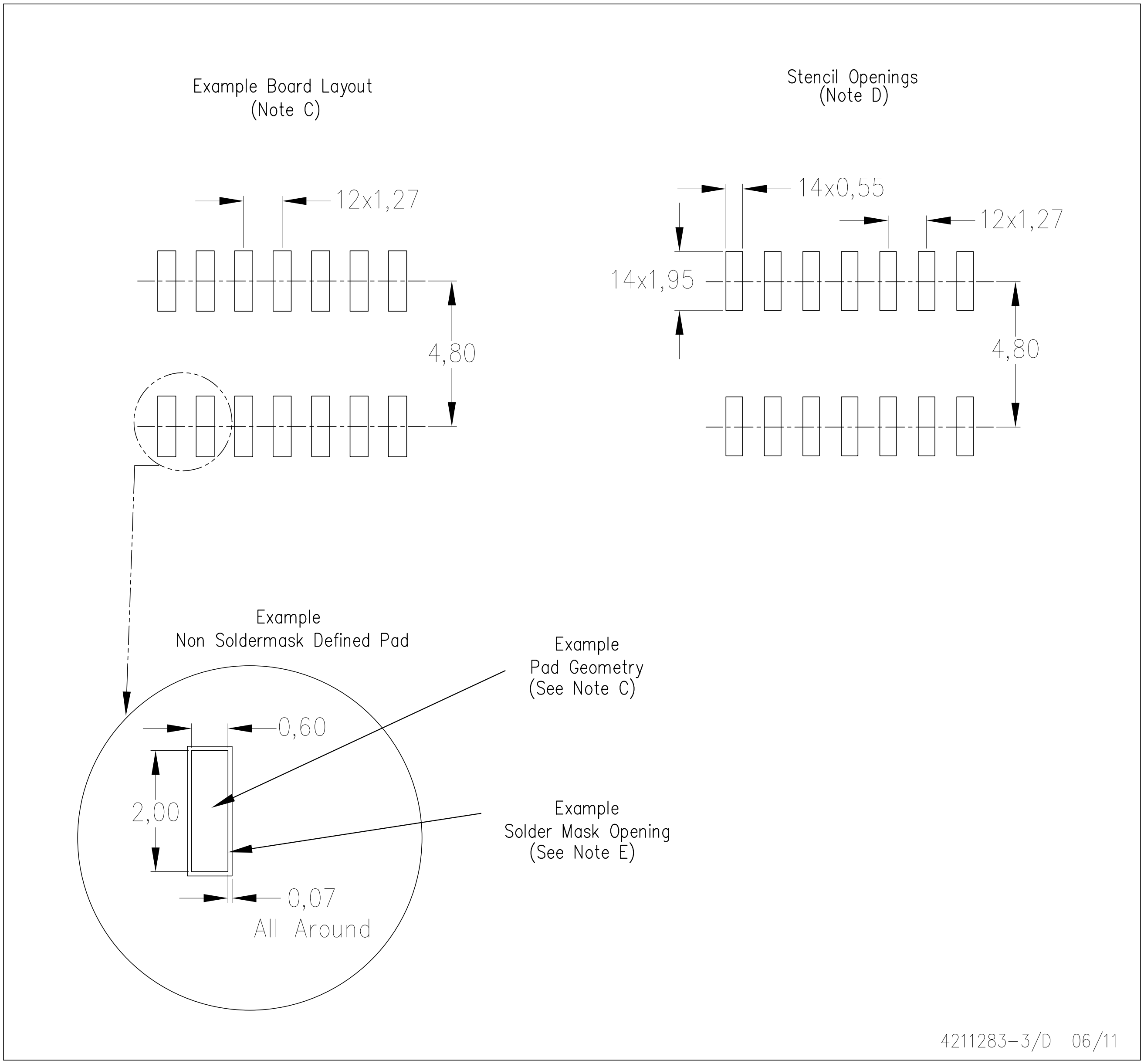
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



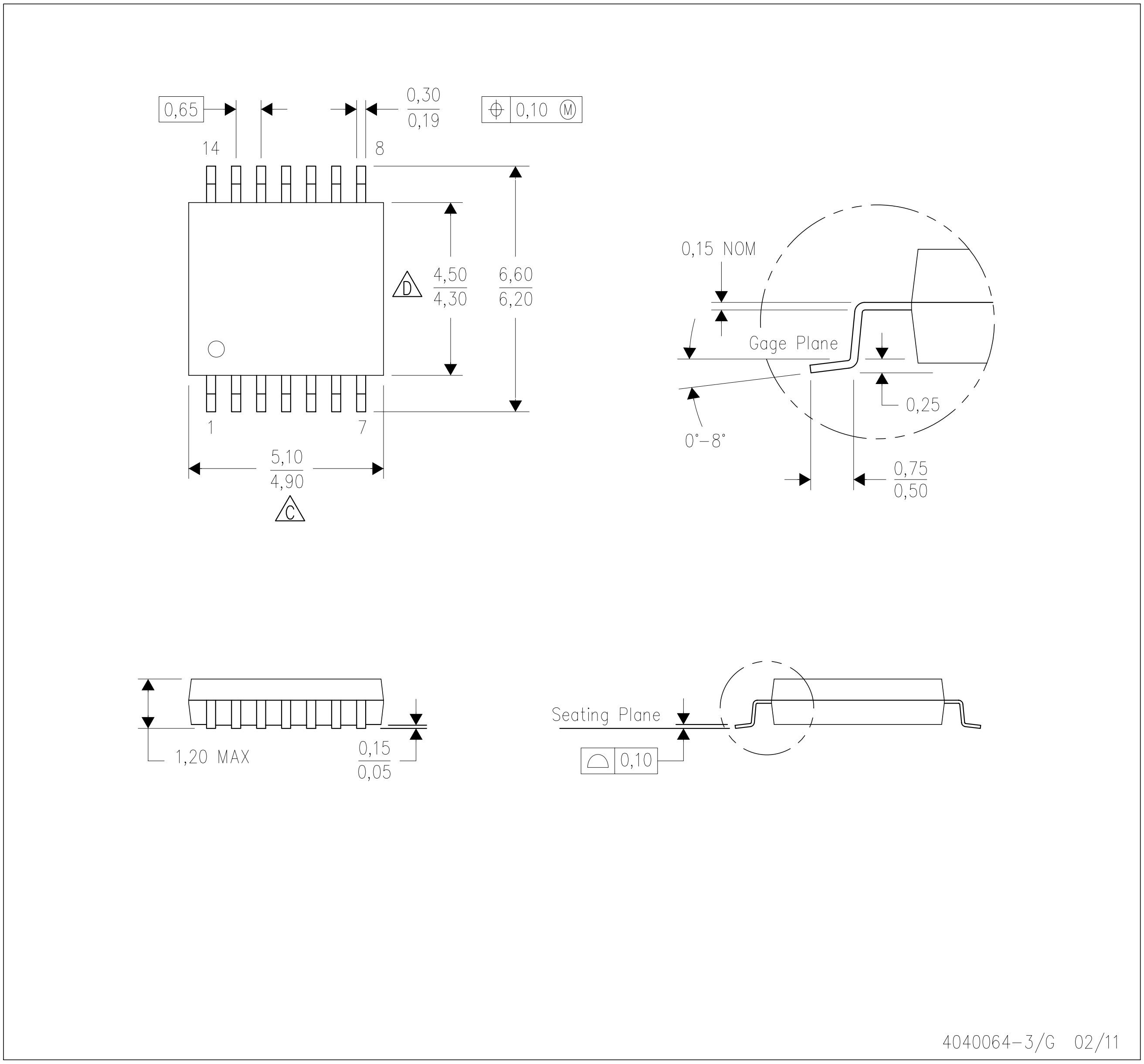
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



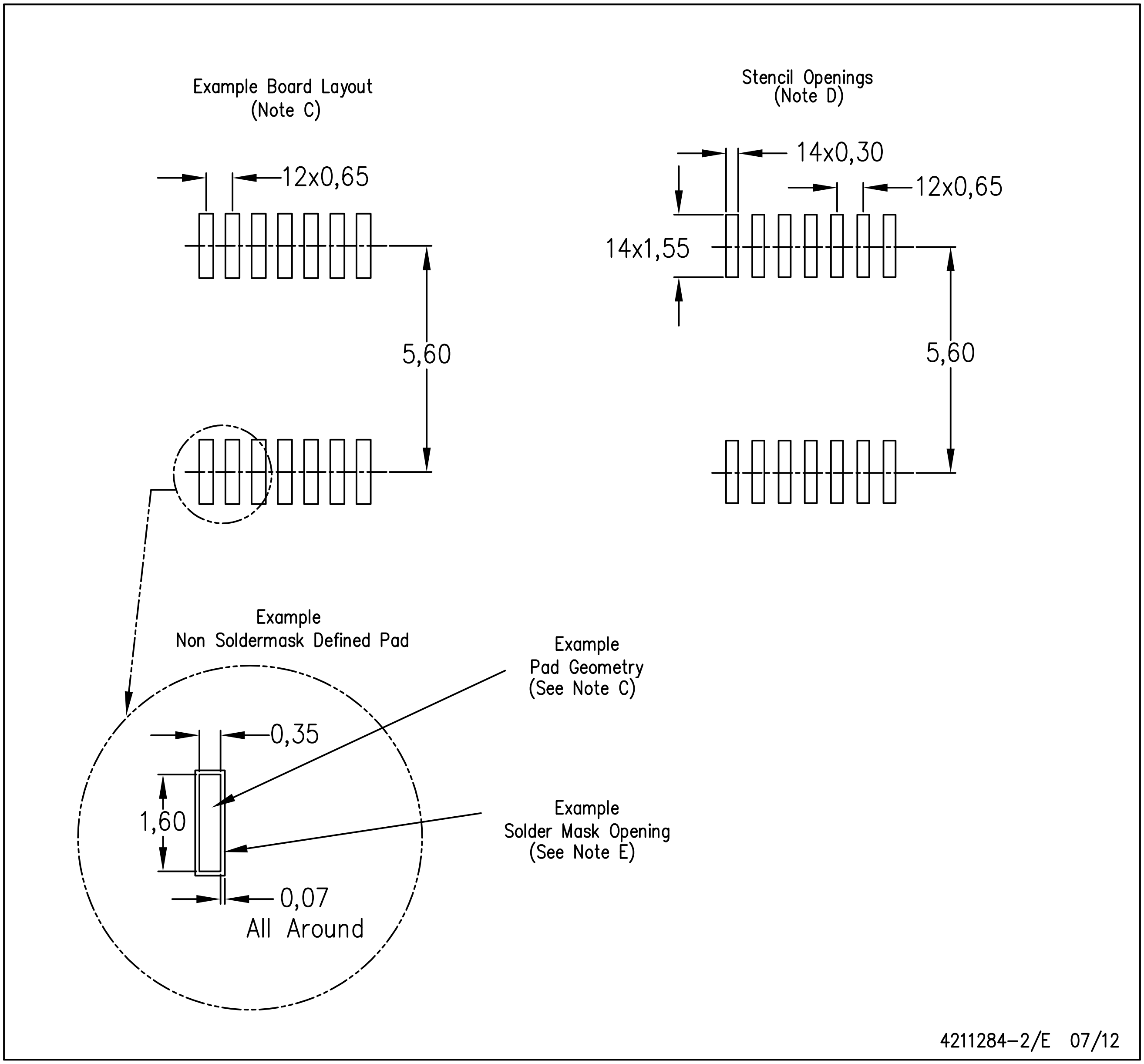
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



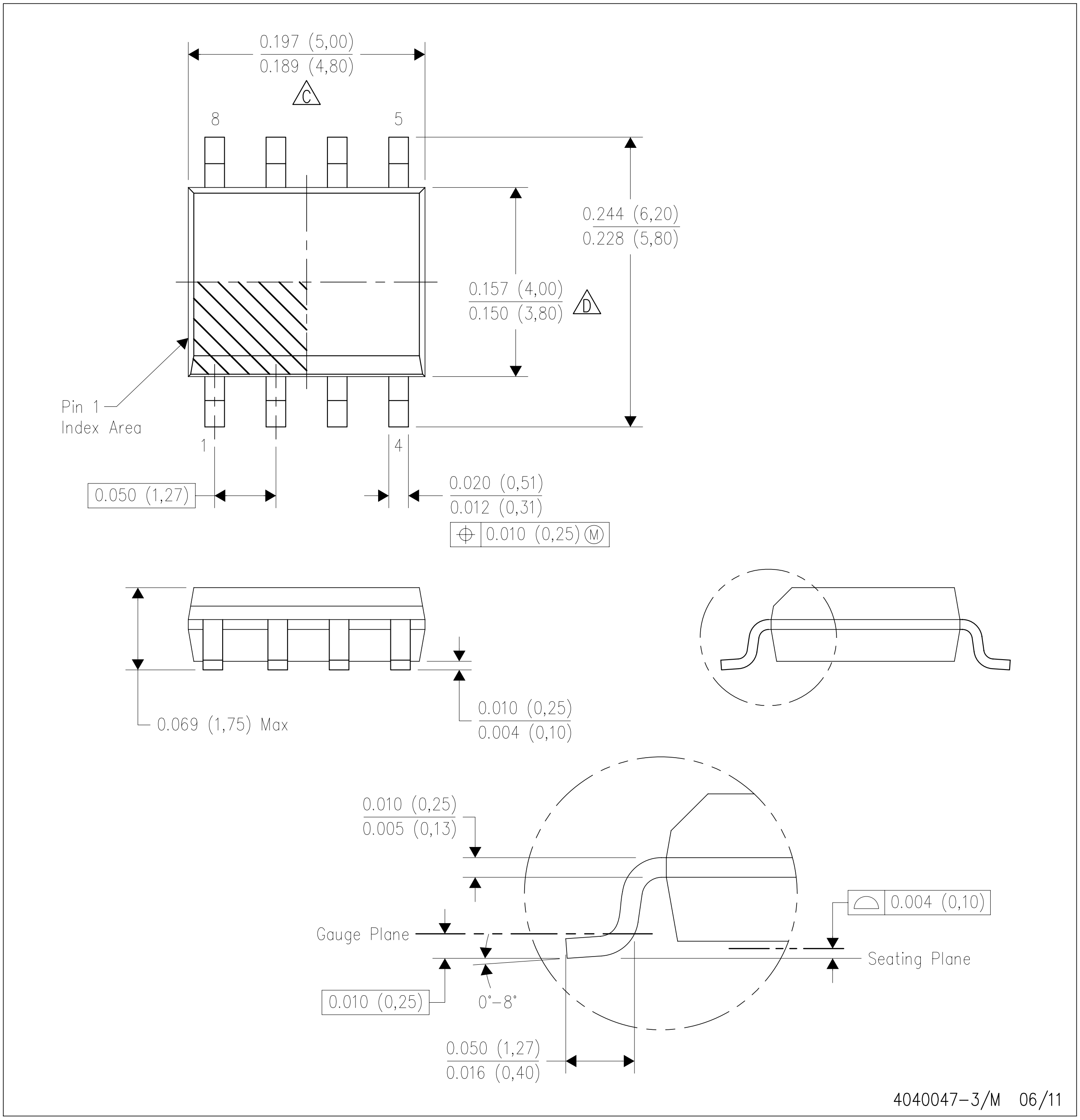
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



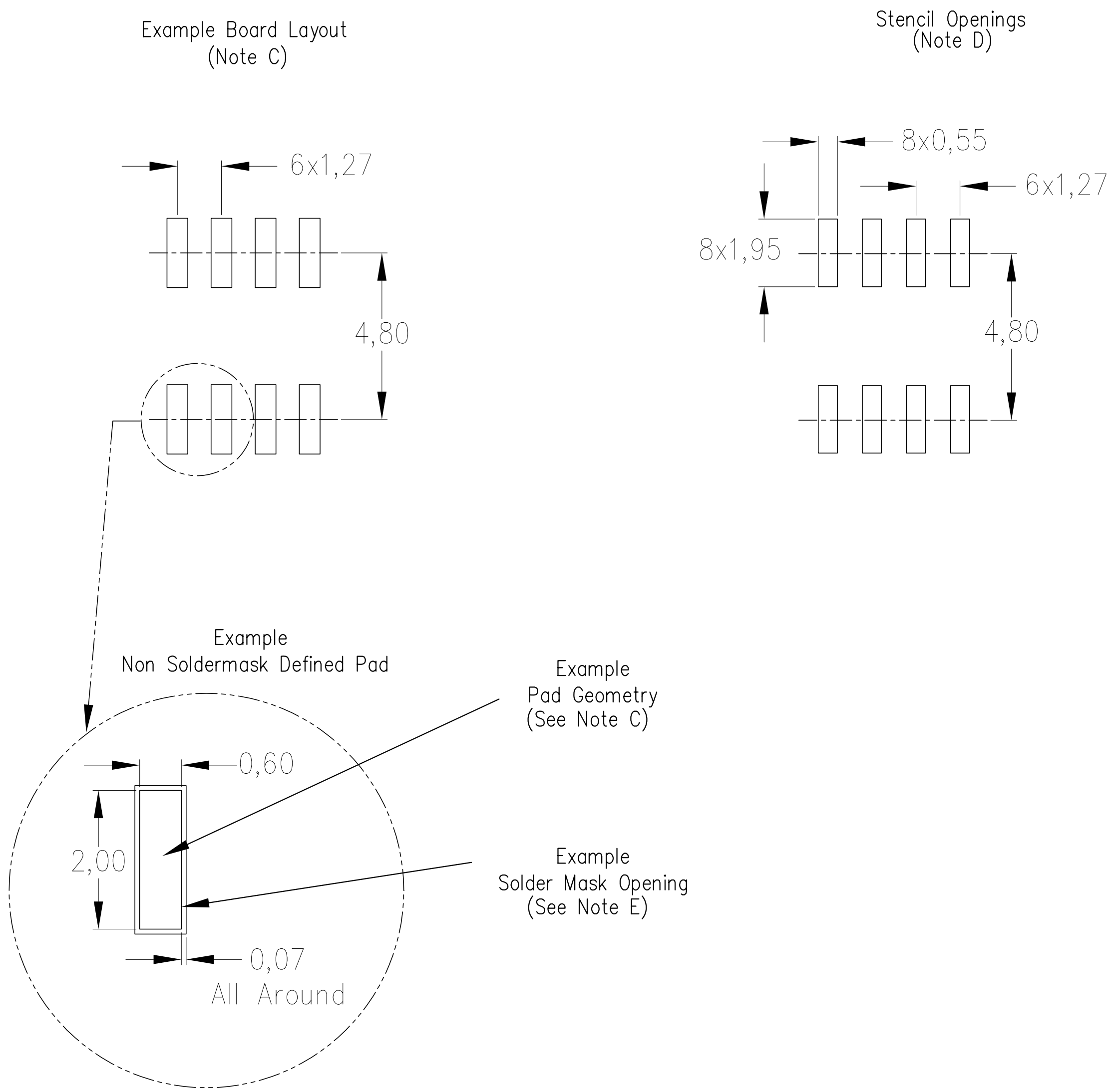
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.