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LOGIC GATES

Aim : To study logic gates ICs

Materials required :

Jumper wires, resistors, Jumper wires.

7404 (NOT GATE)

7400 (NAND GATE)

7408 (AND GATE)

7432 (OR GATE)

748C (XOR GATE)

} Same IC orientation.

7402 (NOR GATE)

Procedure.

- Connect the IC's to lower source
- Give high and low inputs accordingly to input part
- Through a resistor, connect the IC's to LEDs and record output

* **NOT GATE** ($\rightarrow\!\!\triangleright\!\!\circ\!\!-$)

$Y = \bar{A}$

TRUTH TABLE

A	Y
0	1
1	0

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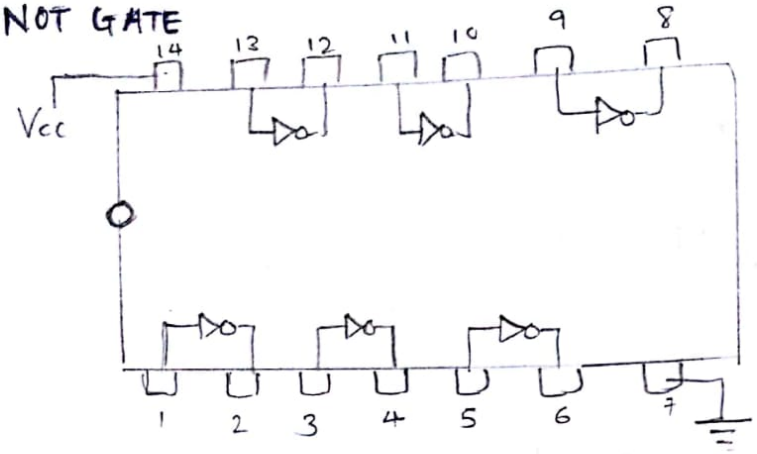
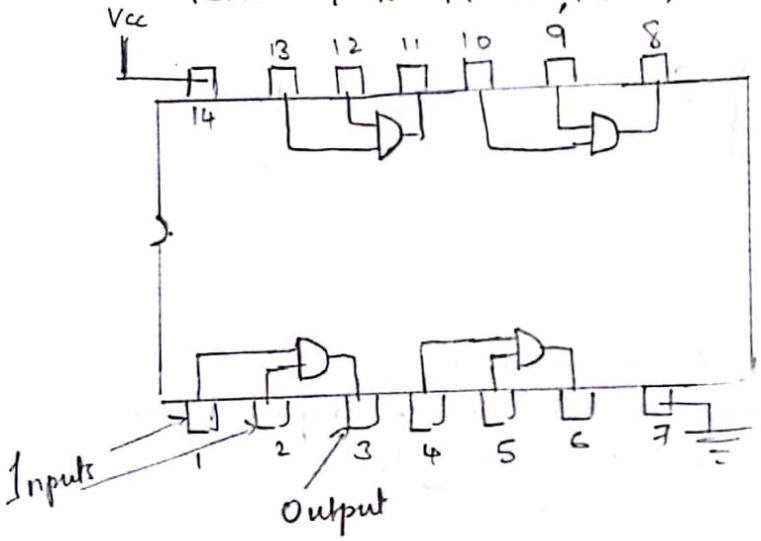
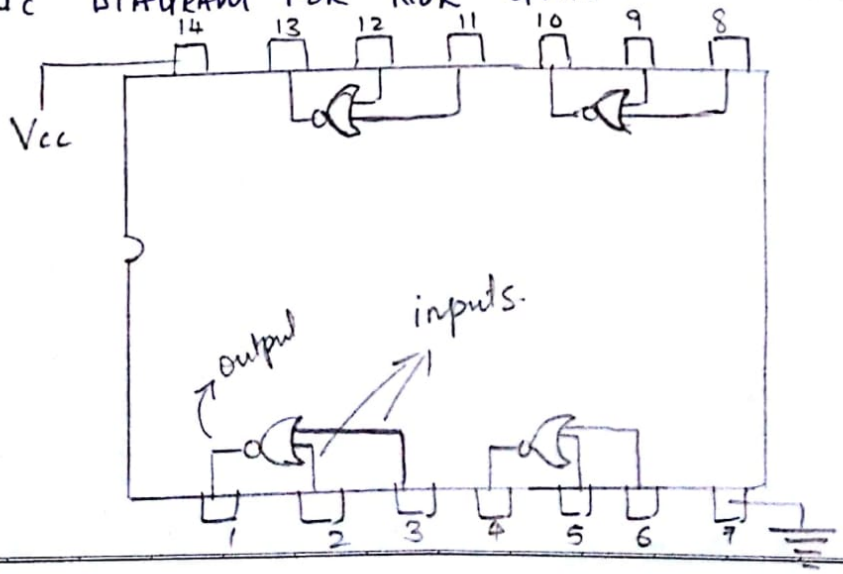
NOT GATE



Ic DIAGRAM FOR NAND, AND, OR & XOR :-



Ic DIAGRAM FOR NOR GATE.



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* NOR GATE (=D○-)

$Y = \overline{A+B}$

TRUTH TABLE

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

* XOR GATE (=)))

$Y = A\bar{B} + \bar{A}B$

TRUTH TABLE

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

* OR GATE (=)-)

$Y = A + B$

TRUTH TABLE

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

* AND GATE (=D-)

$Y = A \cdot B$

TRUTH TABLE

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

* NAND GATE

$Y = \overline{A \cdot B}$

A	B	Y
0	0	1
1	0	1
0	1	1
1	1	0

Conclusion:

The truths tables were made and verified for logic gates.

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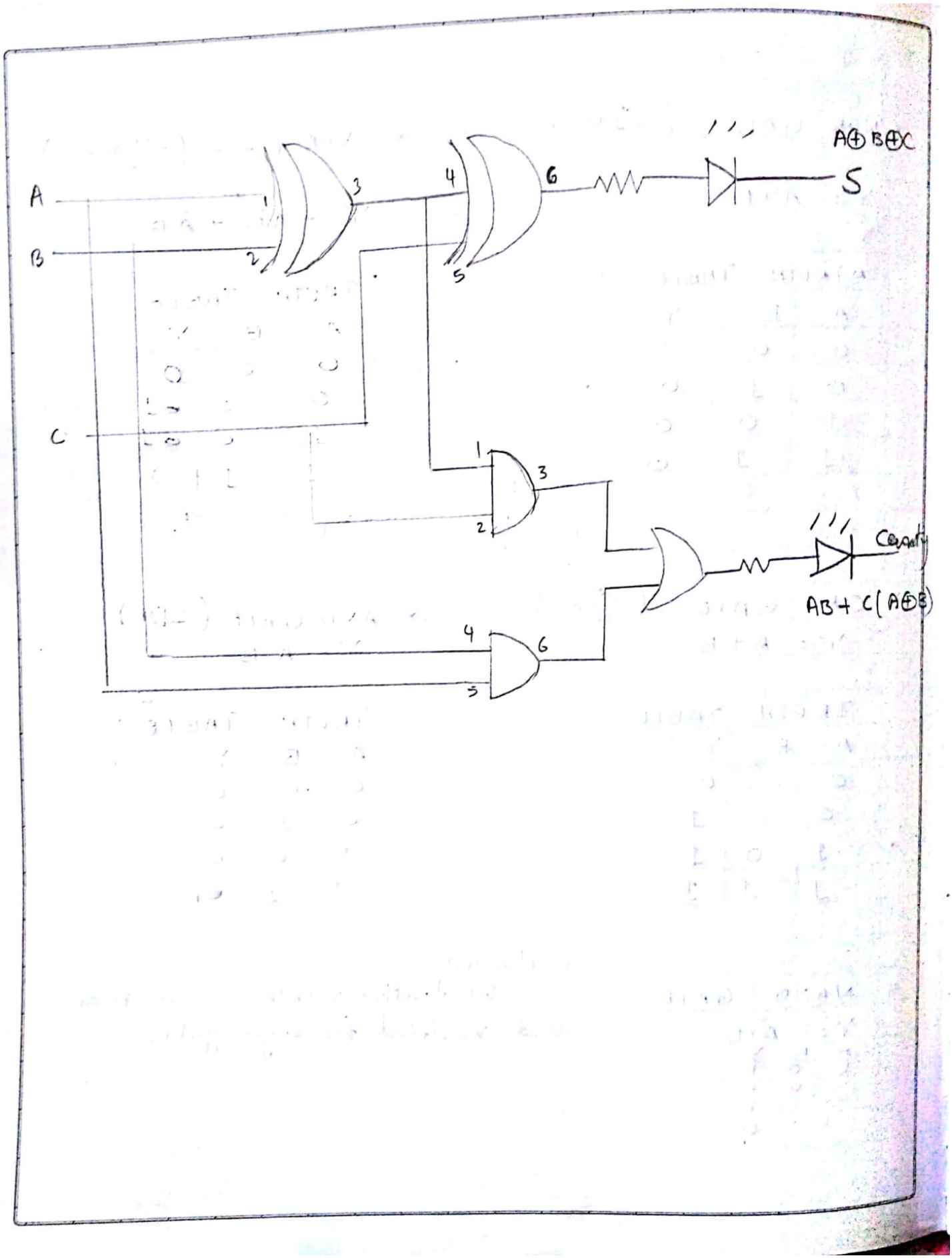

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FULL ADDER CIRCUIT

Aim: To make a full adder circuit.

Components Required:
- 7408 (AND GATE)
- 7432 (OR GATE)
- 7486 (XOR GATE)
- Resistor
- LEDS

A	B	C	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

output verified 01/8/17

$S = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

$= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC)$

$= A(B \oplus C) + A(\overline{B \oplus C})$

$=$ Taking $A = X$ and $B \oplus C = Y$

$= X\bar{Y} + X\bar{Y}$

$= X \oplus Y$

$\therefore S = A \oplus B \oplus C$

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$$C_{out} = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$
$$= C(\bar{A}B + A\bar{B}) + AB(\bar{C} + C)$$
$$= AB + C(A \oplus B)$$

Result: A full adder circuit was designed and verified.

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B_3

$\bar{G}_3\bar{G}_2$	$\bar{G}_1\bar{G}_0$	$\bar{G}_1G_0$	G_1G_0	$G_1\bar{G}_0$
$\bar{G}_3\bar{G}_2$	0 (0)	0 (1)	0 (3)	0 (2)
$\bar{G}_3G_2$	0 (4)	0 (5)	0 (7)	0 (6)
G_3G_2	1 (12)	1 (13)	1 (15)	1 (14)
$G_3\bar{G}_2$	1 (8)	1 (9)	1 (11)	1 (10)

$B_3 = G_3$

B_2

G_3G_2	$\bar{G}_1\bar{G}_0$	$\bar{G}_1G_0$	G_1G_0	$G_1\bar{G}_0$
$\bar{G}_3\bar{G}_2$	0 (0)	0 (1)	0 (3)	0 (2)
$\bar{G}_3G_2$	1 (4)	1 (5)	1 (7)	1 (6)
G_3G_2	0 (12)	0 (13)	0 (15)	0 (14)
$G_3\bar{G}_2$	1 (8)	1 (9)	1 (11)	1 (10)

$B_2 = \bar{G}_3G_2 + G_3\bar{G}_2$

$B_2 = G_3 \oplus G_2$

B_1

$\bar{G}_3\bar{G}_2$	$\bar{G}_1\bar{G}_0$	$\bar{G}_1G_0$	G_1G_0	$G_1\bar{G}_0$
$\bar{G}_3\bar{G}_2$	0 (0)	0 (1)	1 (3)	1 (2)
$\bar{G}_3G_2$	1 (4)	1 (5)	0 (7)	0 (6)
G_3G_2	0 (12)	0 (13)	1 (15)	1 (14)
$G_3\bar{G}_2$	1 (8)	1 (9)	0 (11)	0 (10)

$B_1 = \bar{G}_3\bar{G}_2 + \bar{G}_2G_2\bar{G}_1 + G_3G_2G_1 + G_3\bar{G}_2\bar{G}_1$

$B_1 = \bar{G}_3(G_2 \oplus G_1) + G_3(\overline{G_2 \oplus G_1})$

$B_1 = G_3 \oplus G_2 \oplus G_1$

B_0

$\bar{G}_3\bar{G}_2$	$\bar{G}_1\bar{G}_0$	$\bar{G}_1G_0$	G_1G_0	$G_1\bar{G}_0$
$\bar{G}_3\bar{G}_3$	0 (0)	1 (1)	0 (3)	1 (2)
$\bar{G}_3G_2$	1 (4)	0 (5)	1 (7)	0 (6)
G_3G_2	0 (12)	1 (13)	0 (15)	1 (14)
$G_3\bar{G}_2$	1 (8)	0 (9)	1 (11)	0 (10)

$B_0 = \bar{G}_3\bar{G}_2\bar{G}_1G_0 + \bar{G}_3\bar{G}_2G_1\bar{G}_0 + \bar{G}_3G_2\bar{G}_1\bar{G}_0 + \bar{G}_3G_2G_1G_0 + G_3G_2\bar{G}_1G_0 + G_3G_2G_1\bar{G}_0 + G_3\bar{G}_2\bar{G}_1\bar{G}_0 + G_3\bar{G}_2G_1G_0$

$B_0 = G_3 \oplus G_2 \oplus G_1 \oplus G_0$

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4- Bit Gray to Binary Converter

G_3	G_2	G_1	G_0	B_3	B_2	B_1	B_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

output verified
24/8/18

Procedure :

- Do the k mapping for all the values from Gray to Binary.
- Design and construct the appropriate circuit
- Verify the truth table.

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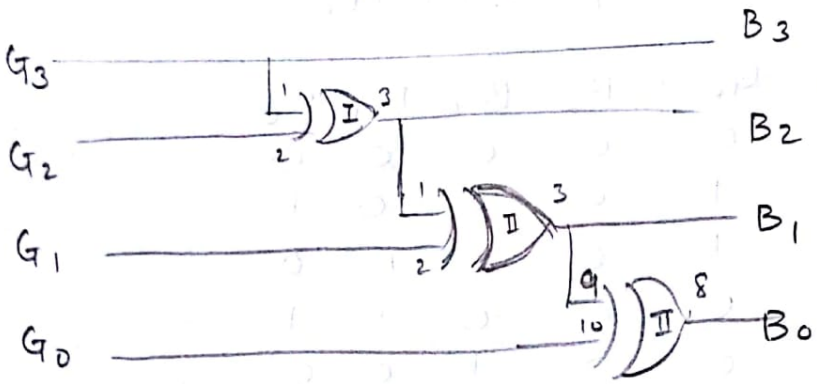
CIRCUIT DIAGRAM



4 - Bit Gray to Binary

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Result : The k-mapping from Gray to Binary and the truth table is verified.

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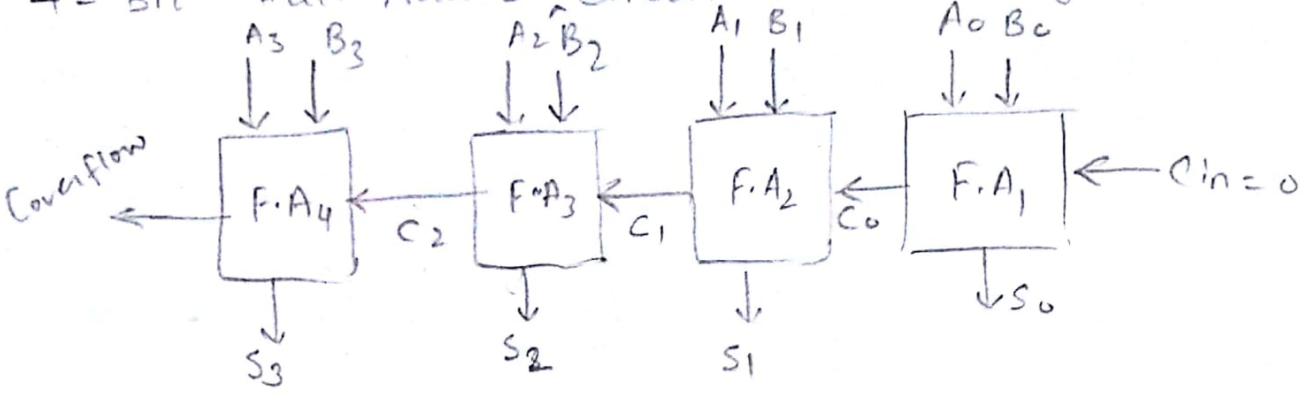
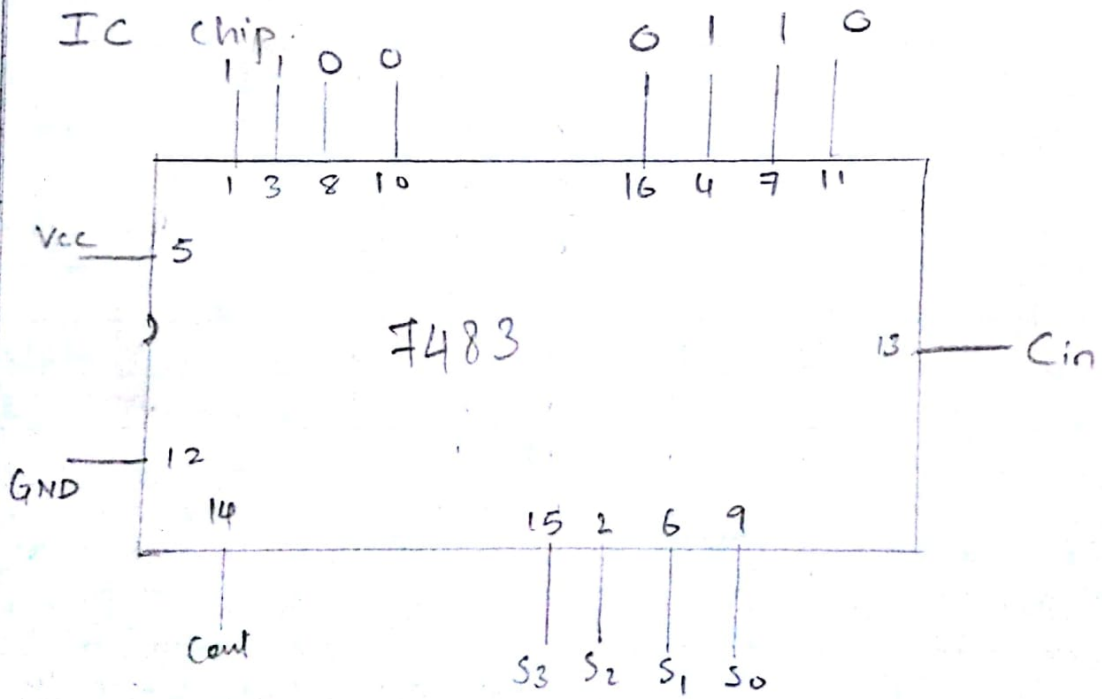
4 - Bit Full Adder Circuit (Block Diagram)



IC chip



output

12

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4-Bit Full Adder.

Aim : To make a 4-Bit Full Adder.

Components Required : 7483 IC Chip
Resistors
LEDs

Truth Table

Sum = $A \oplus B \oplus C$

Carry = $AB + C(A \oplus B)$

Result : A test was done and 2 4-bit binary numbers were fed and the output was verified.

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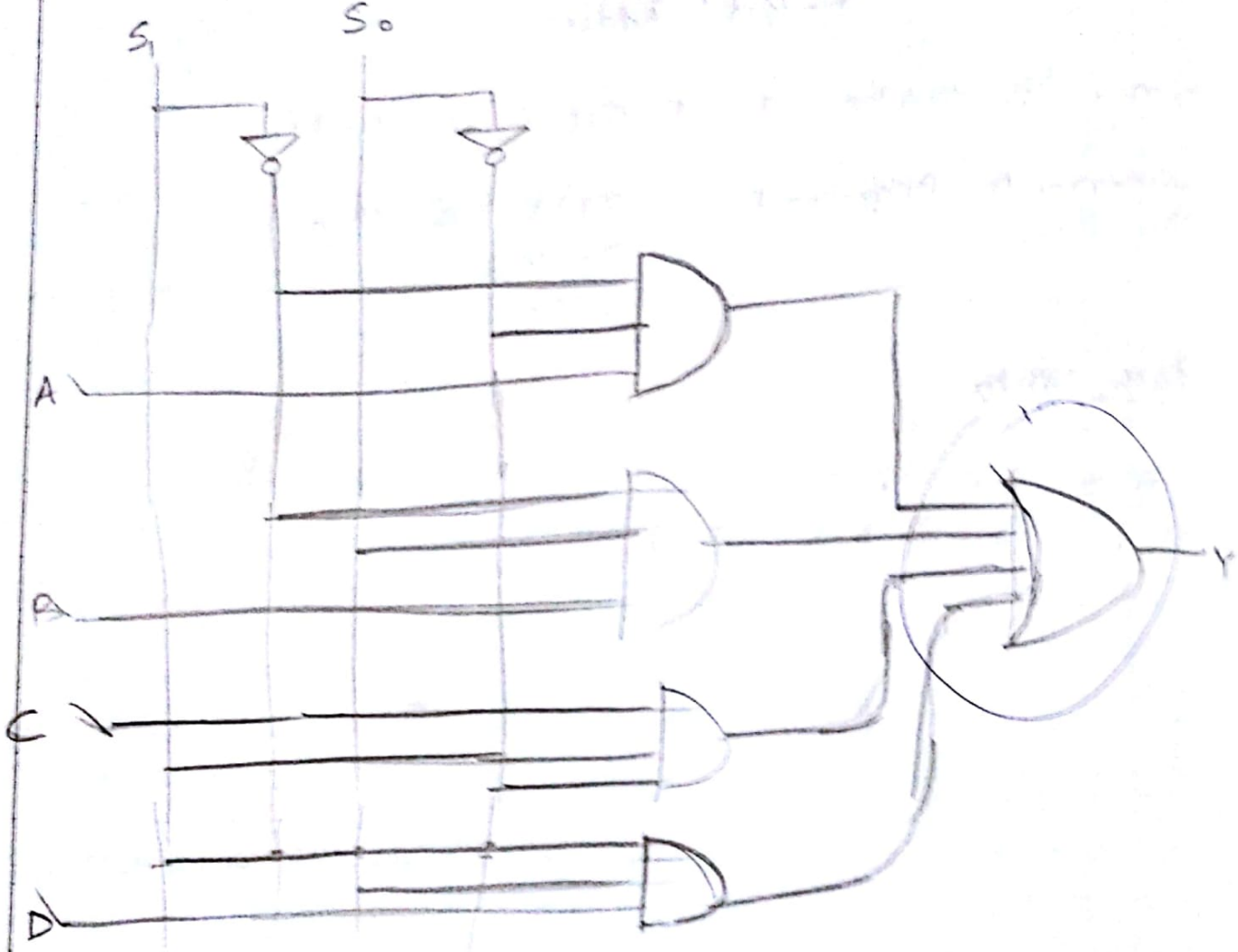
Circuit Diagram.



TRUTH TABLE

S_1	S_0	A	B	C	D	Y
0	0	1/0	0	0	0	A
0	1	0	1/0	0	0	B
1	0	0	0	1/0	0	C
1	1	0	0	0	1/0	D

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~~Parallel Adder~~ Multiplexer

Aim : To successfully make a multiplexer.

Component required : LEDs
Resistors
Gates (AND and OR)
AND (7408)
OR (7432)

By observing the Truth Table, the output is

$$Y = \bar{S}_0\bar{S}_1 A + S_0\bar{S}_1 B + \bar{S}_0 S_1 C + S_0 S_1 D$$

Result : The multiplexer circuit was successfully verified.

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FULL ADDER.

```
module FA(a, b, c, s, Co)
 input a, b, c;
 output s, Co;
 wire d, e, f;
 xor (sum, a, b, c);
 and (d, a, b);
 and (e, b, c);
 and (f, a, c);
 or (Co, d, e, f);
endmodule.

// Test Bench.
module fulladdt_b;
reg a, b, c;
wire sum;
wire carry;
FA uut (.a(a), .b(b), .c(c), .sum(s), .Co(Co));
initial
 begin
#10 a = 1'b0; b = 1'b0; c = 1'b0;
#10 a = 1'b0; b = 1'b0; c = 1'b1;
#10 a = 1'b0; b = 1'b1; c = 1'b0;
#10 a = 1'b0; b = 1'b1; c = 1'b1;
#10 a = 1'b1; b = 1'b0; c = 1'b0;
#10 a = 1'b1; b = 1'b0; c = 1'b1;
#10 a = 1'b1; b = 1'b1; c = 1'b0;
#10 a = 1'b1; b = 1'b1; c = 1'b1;
#10 $stop ; end
endmodule
```

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