CMOS Inverter Layout

Name: Sparsh Arya
Registration Number: 17BEC0656
Lab slot: L37 + L38

Aim

- To draw the schematic of inverter
- To draw the layout of inverter
- To remove any errors caused
- To the check its functionality
- To calculate Delay

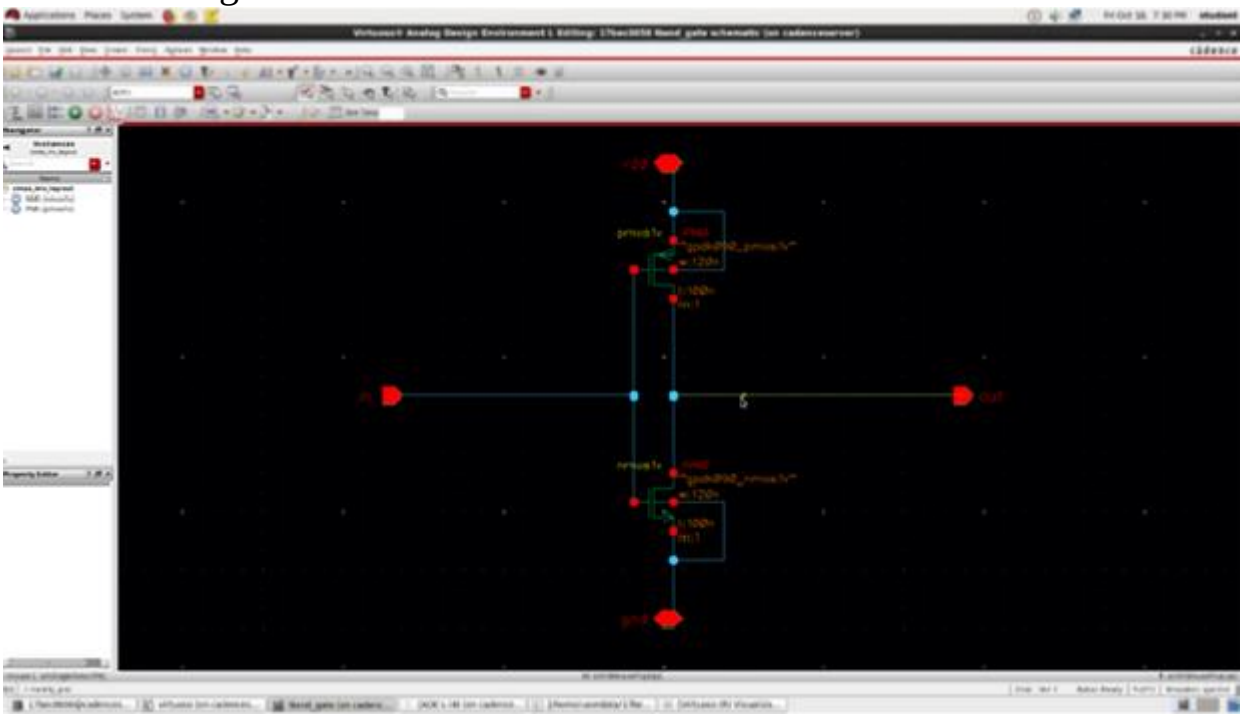
Materials required

Cadence Software

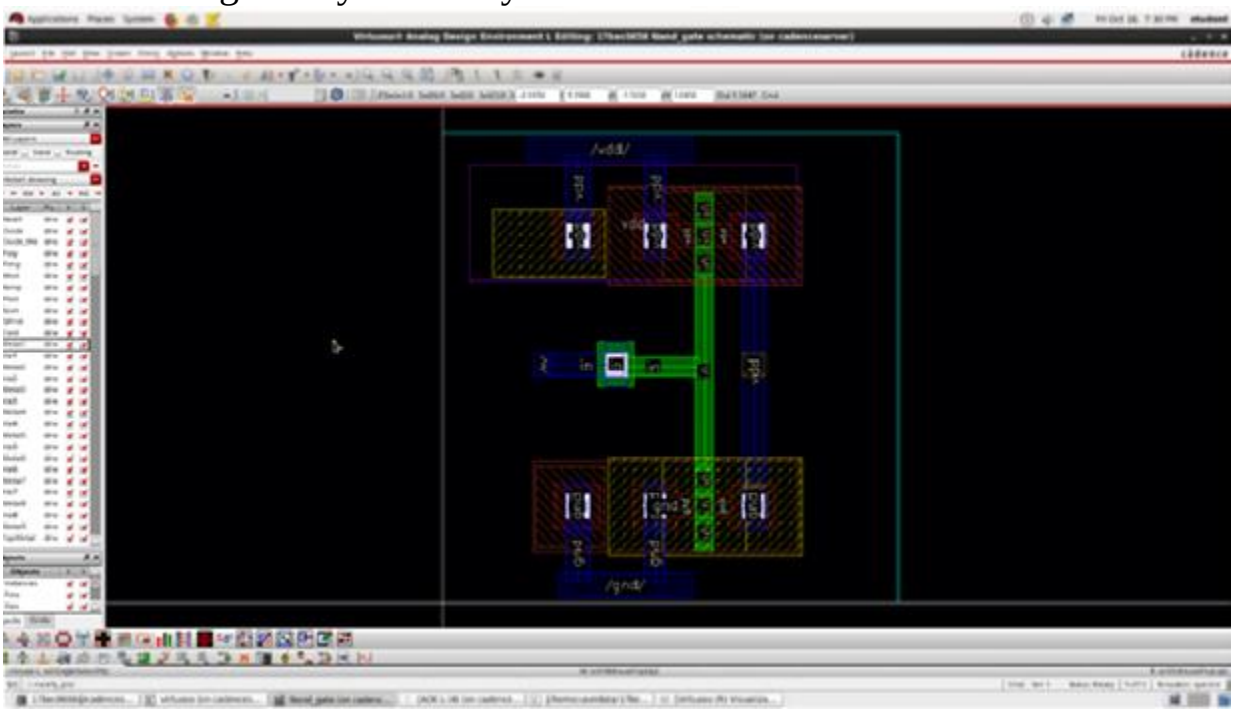
- Gnd
- Vdc
- NMOS
- PMOS
- Vdd
- Vpulse
- Input and Outputs

Observations

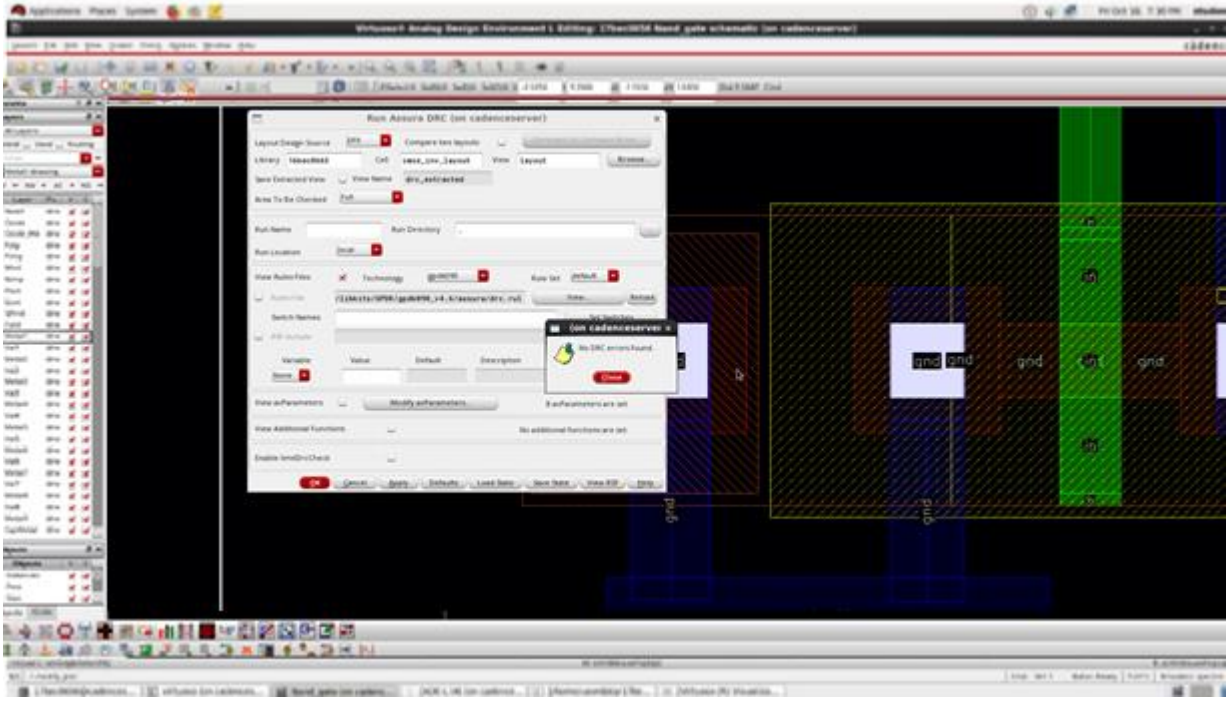
1. Drawing the Schematic in Virtuoso



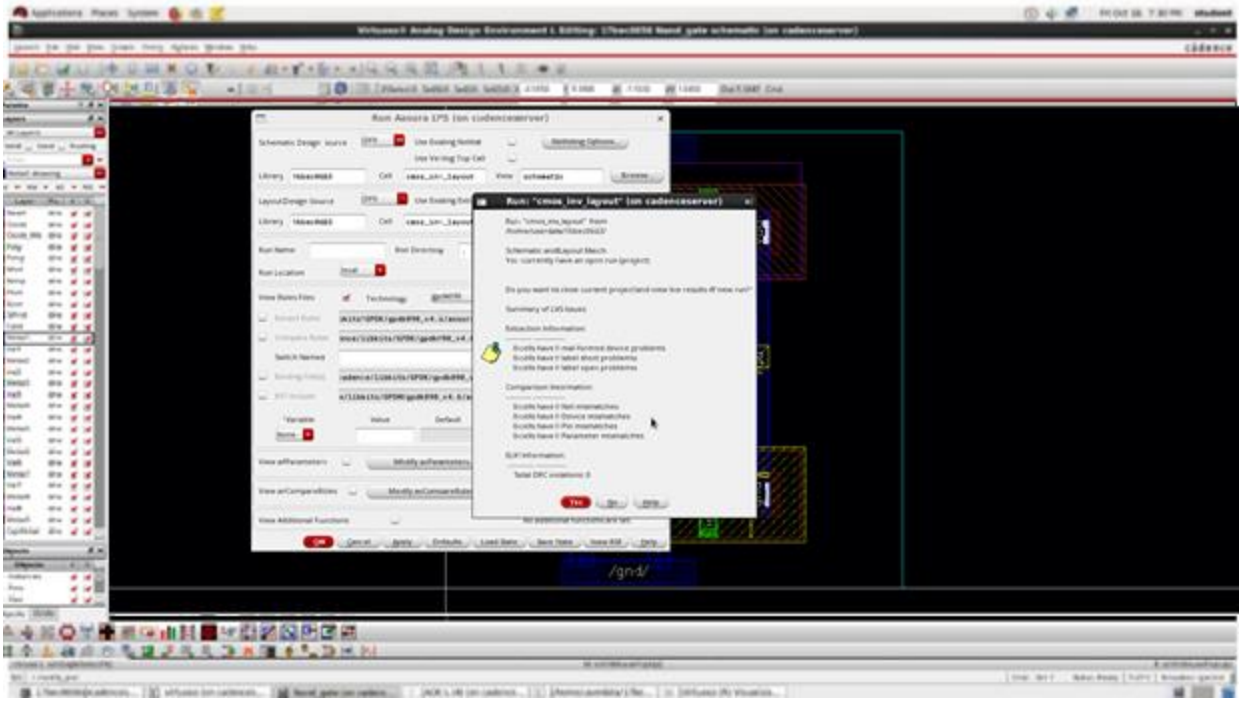
2. Drawing the layout in Layout XL



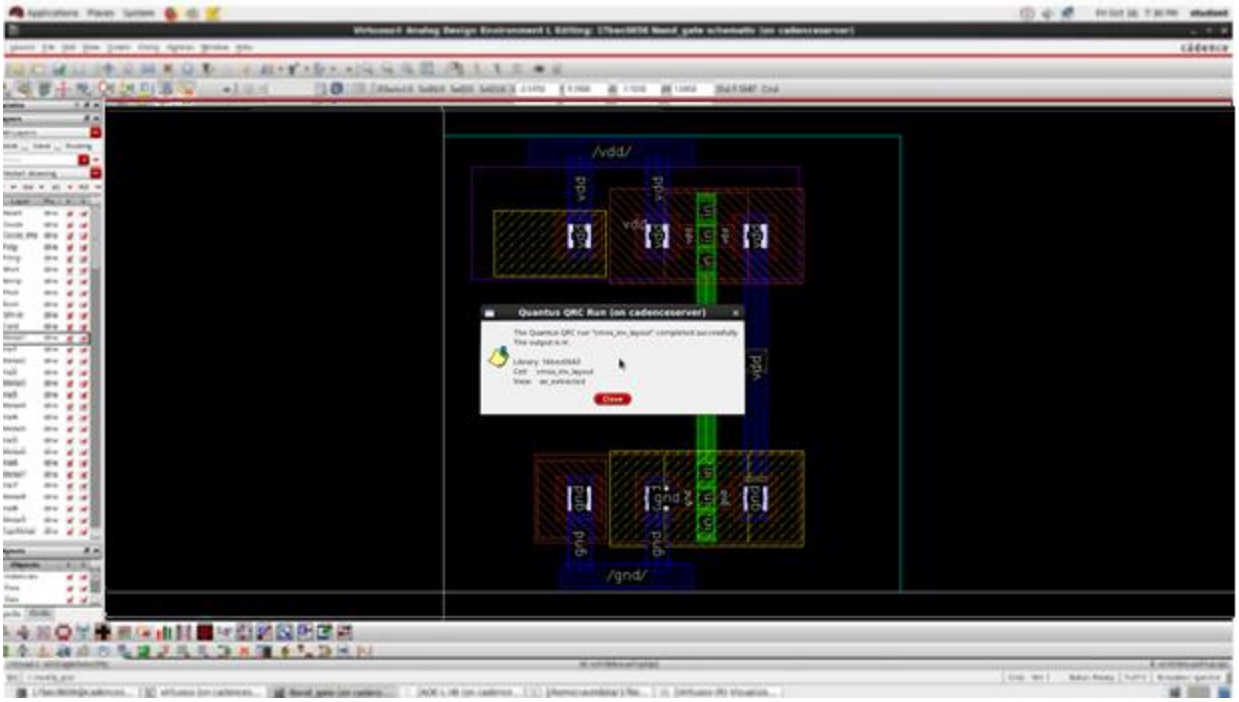
3. Removing DRC error



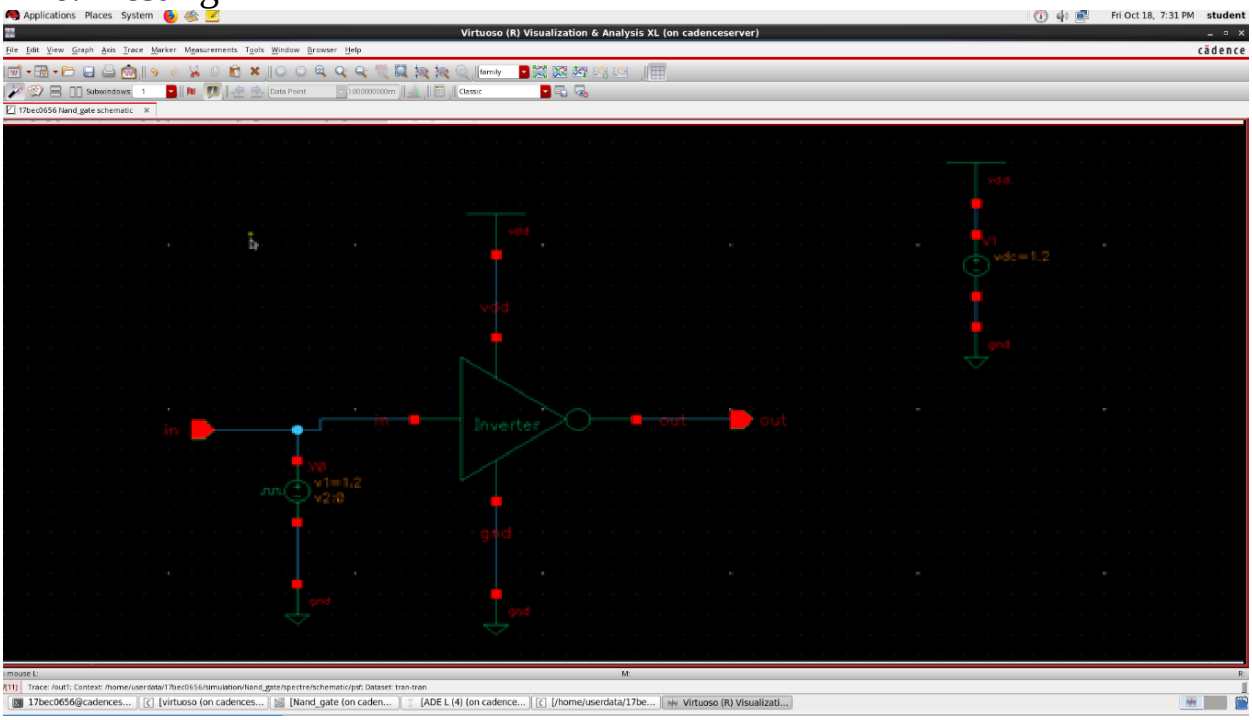
4. Removing LVS error



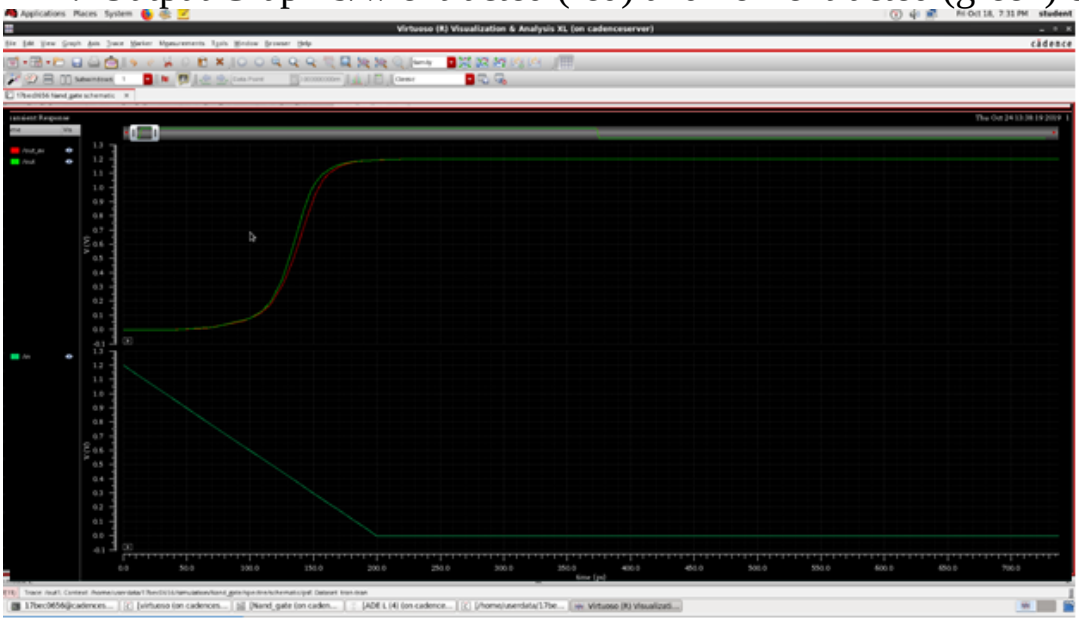
5. QRC check



6. Testing



7. Output Graph b/w extracted (red) and non-extracted (green) outputs



8. Delay (Rising)

9. Delay (Falling)

Calculations

Rising

With AV extracted = 132.86 ns
Without AV extracted = 129.32 ns

Rising Delay = 3.54 ns

Falling

With AV extracted =22.191 ns
Without AV extracted =22.028 ns

Falling Delay = 0.163 ns

Results and Inference

Schematic and Layout of CMOS Inverter were successfully created and tested without any errors.

Rising Delay = 3.54 ns
Falling Delay = 0.163 ns
