VLSI LAB

TASK 5

4 BIT FULL ADDER IMPLEMENTATION

Done by:

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Aim:

To design a 4-bit Full Adder circuit and plot its various characteristics using Virtuoso Cadence Tool Software.

Materials Required:

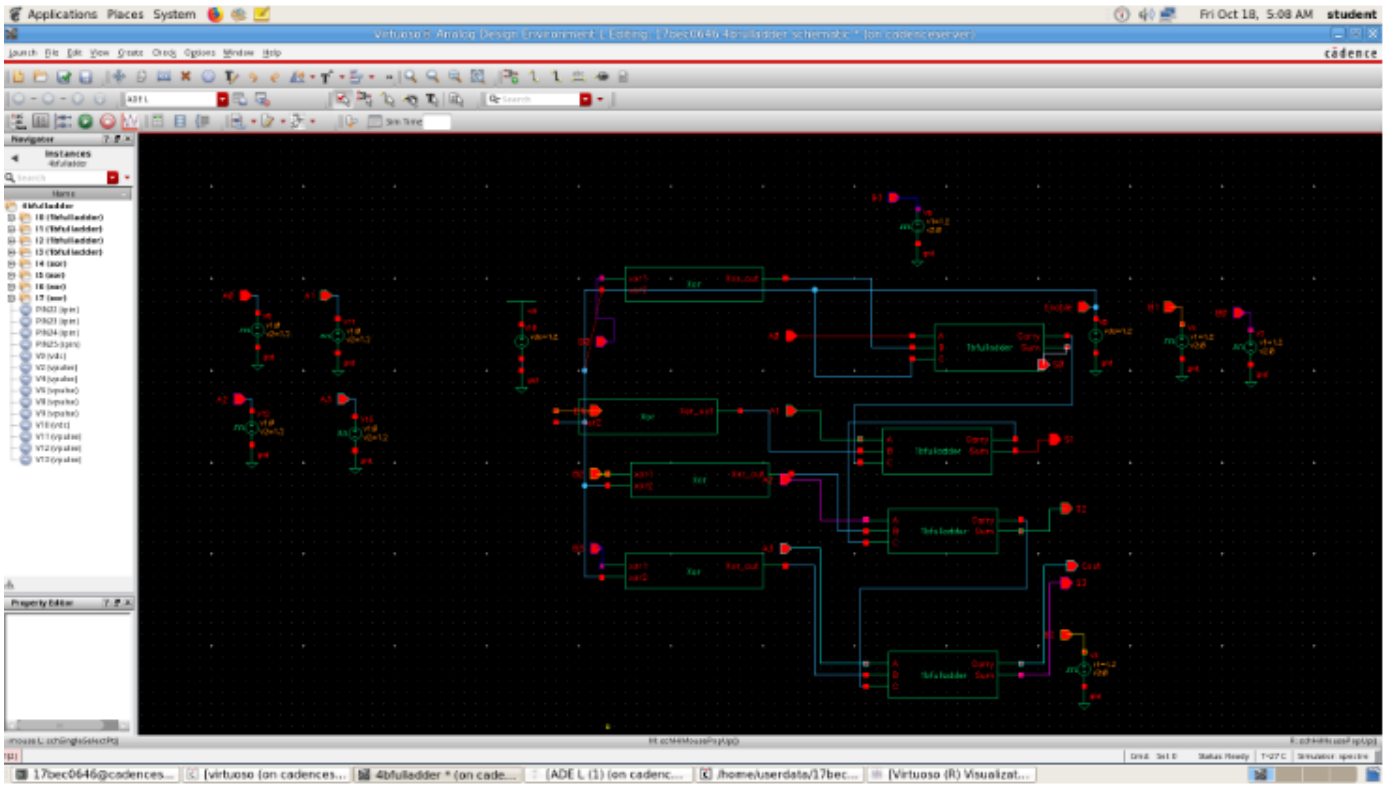
Virtuoso Cadence Tool Software

Procedure

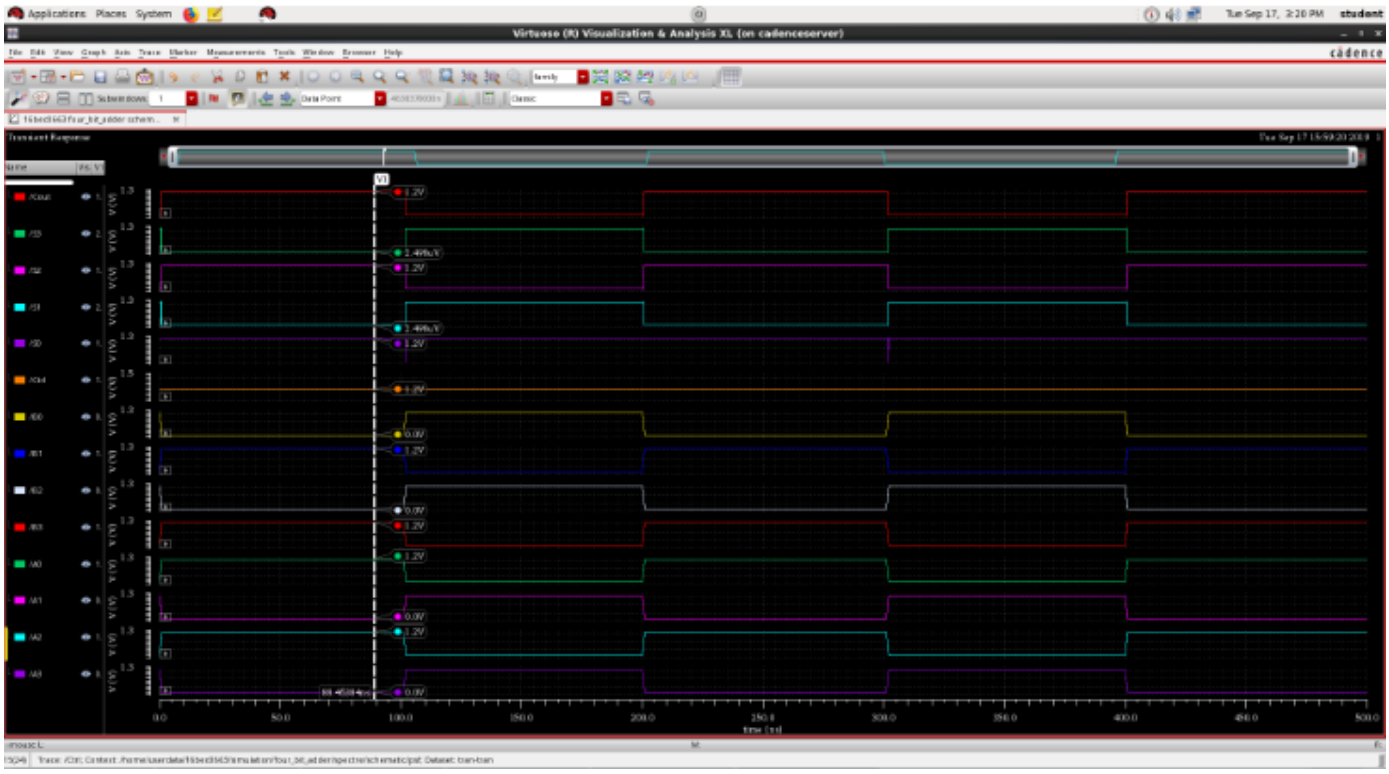
1. Create the basic symbols for AND GATE, NOT GATE & OR GATE.
2. Create a XOR GATE symbol.
3. Create a simple 1-bit full adder circuit with 3 inputs & sum and carry as the output.
4. Call 4 1-bit full adder circuits to obtain the sum and difference of 2 4-bit numbers.
5. The final output is obtained and the following waveforms are plotted against each input.
6. Delay is calculated for the following circuit.

Lab Output:

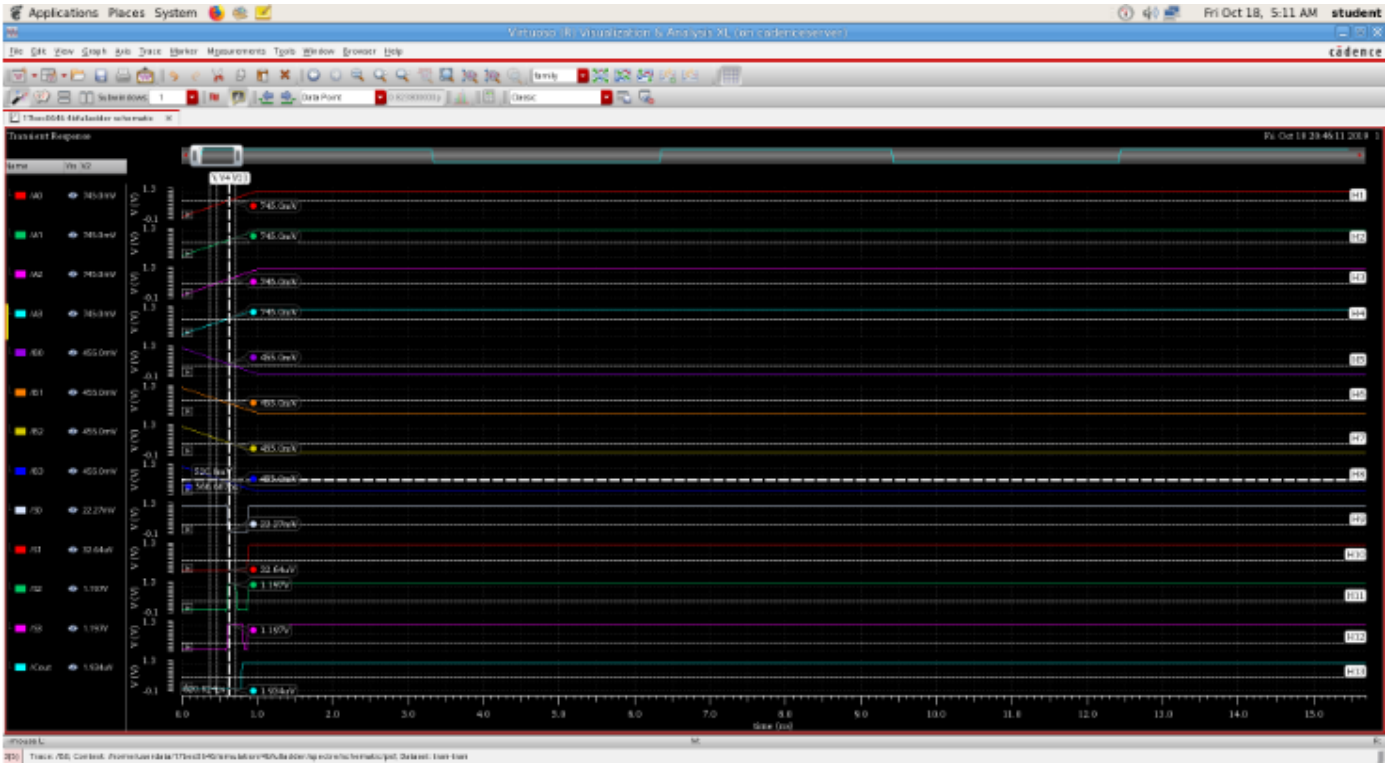
FULL ADDER Schematic



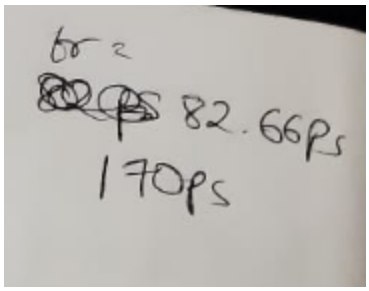
OUTPUT GRAPH



DELAY CALCULATION



Calculation



Inference

RISE TIME: 82.66pS
FALL TIME:170 ps
Propogation delay:126.33ns

Result

The full adder circuit has been successfully constructed and the output waveforms have been observed using the Virtuoso Cadence Tool Software

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