VLSI LAB

TASK 6

NAND GATE IMPLEMENTATION

Done by:

Name: Sparsh Arya
Registration Number: 17BEC0656
Slot: A1
Teacher: Sakthivel R

Aim:

To design a 2 input NAND Gate circuit and plot its various characteristics using Virtuoso Cadence Tool Software.

Materials Required:

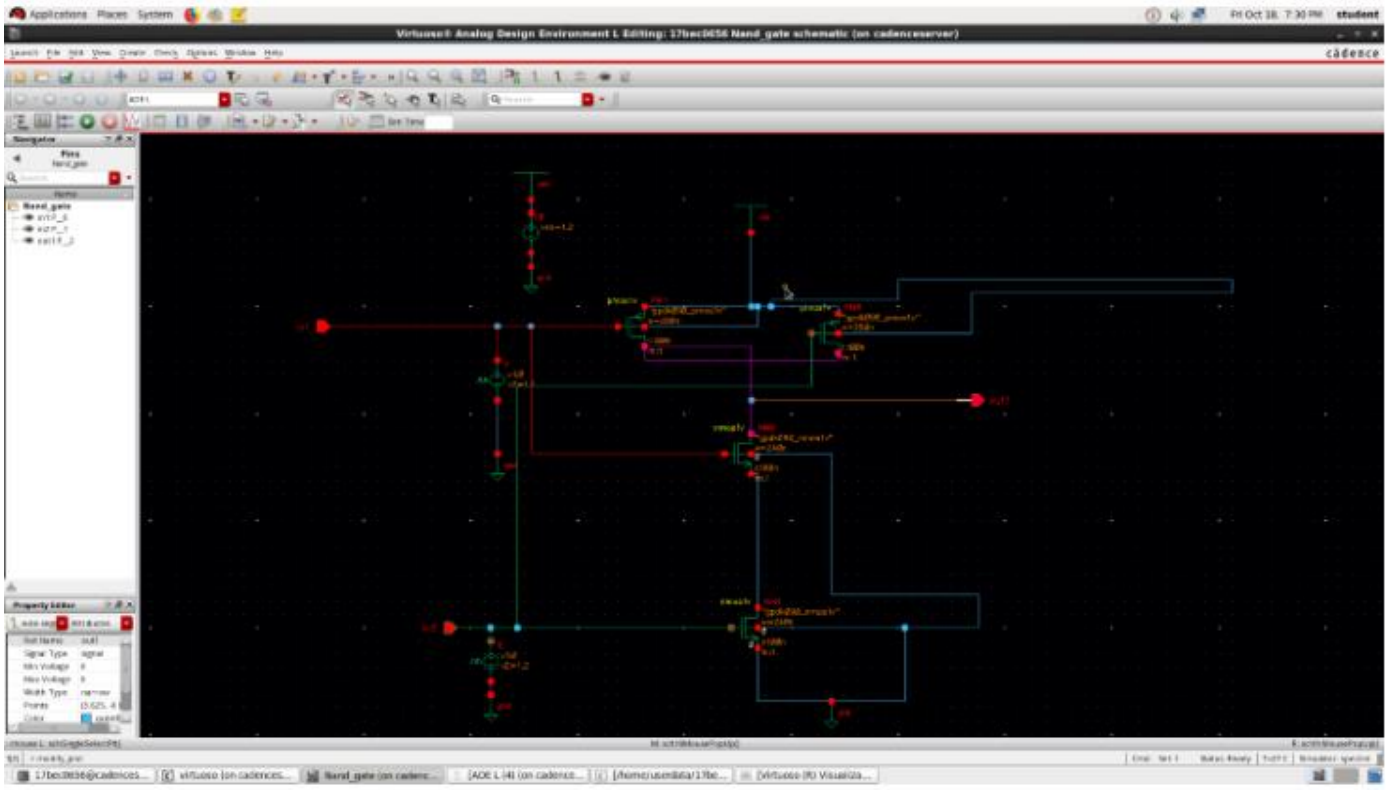
Virtuoso Cadence Tool Software

Procedure

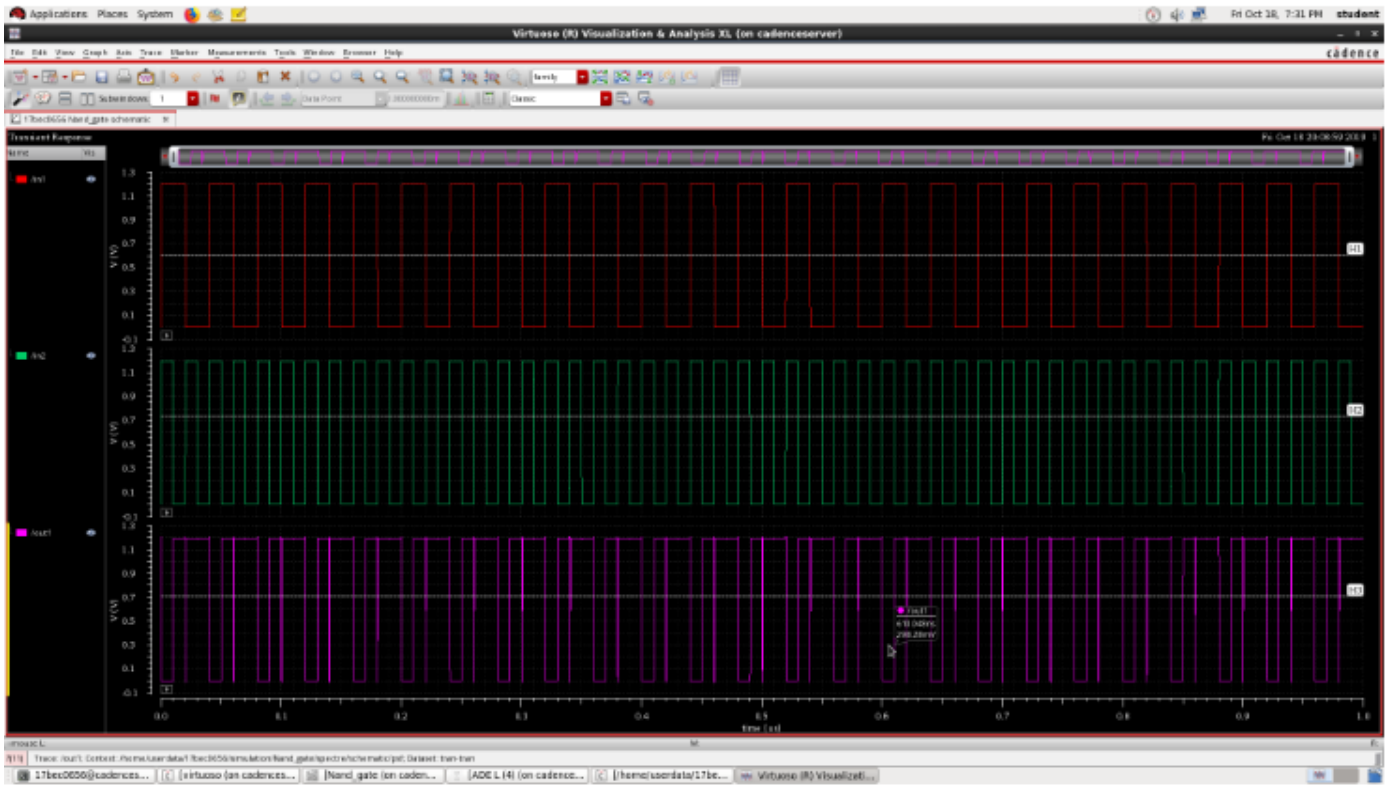
1. Make the 2 input NAND schematic by connecting various components using the virtuoso libraries.
2. Find the waveforms for 2 input and plot the output waveforms.
3. Calculate the power for the following circuit. Also calculate the rise time and the fall time along with propagation delay.

Lab Output:

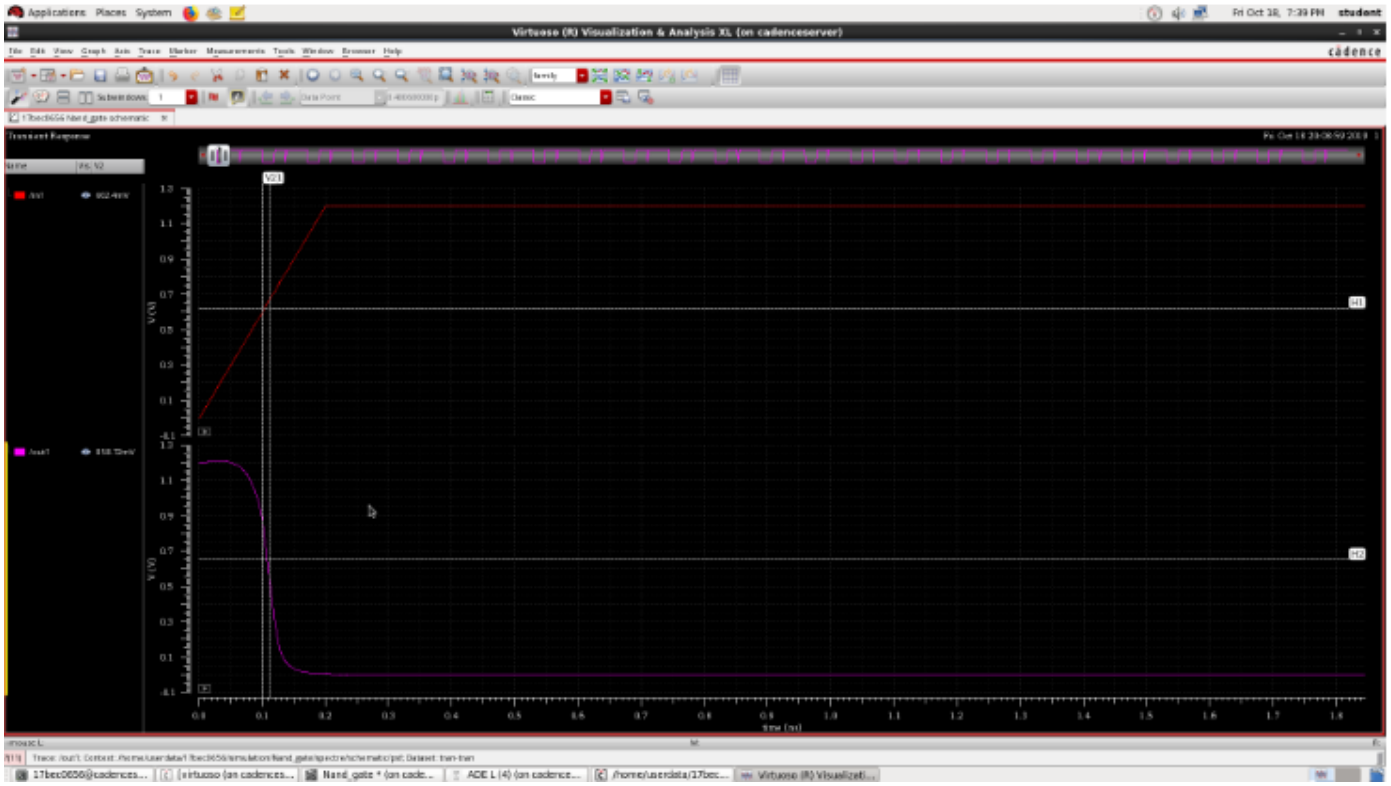
NAND Schematic



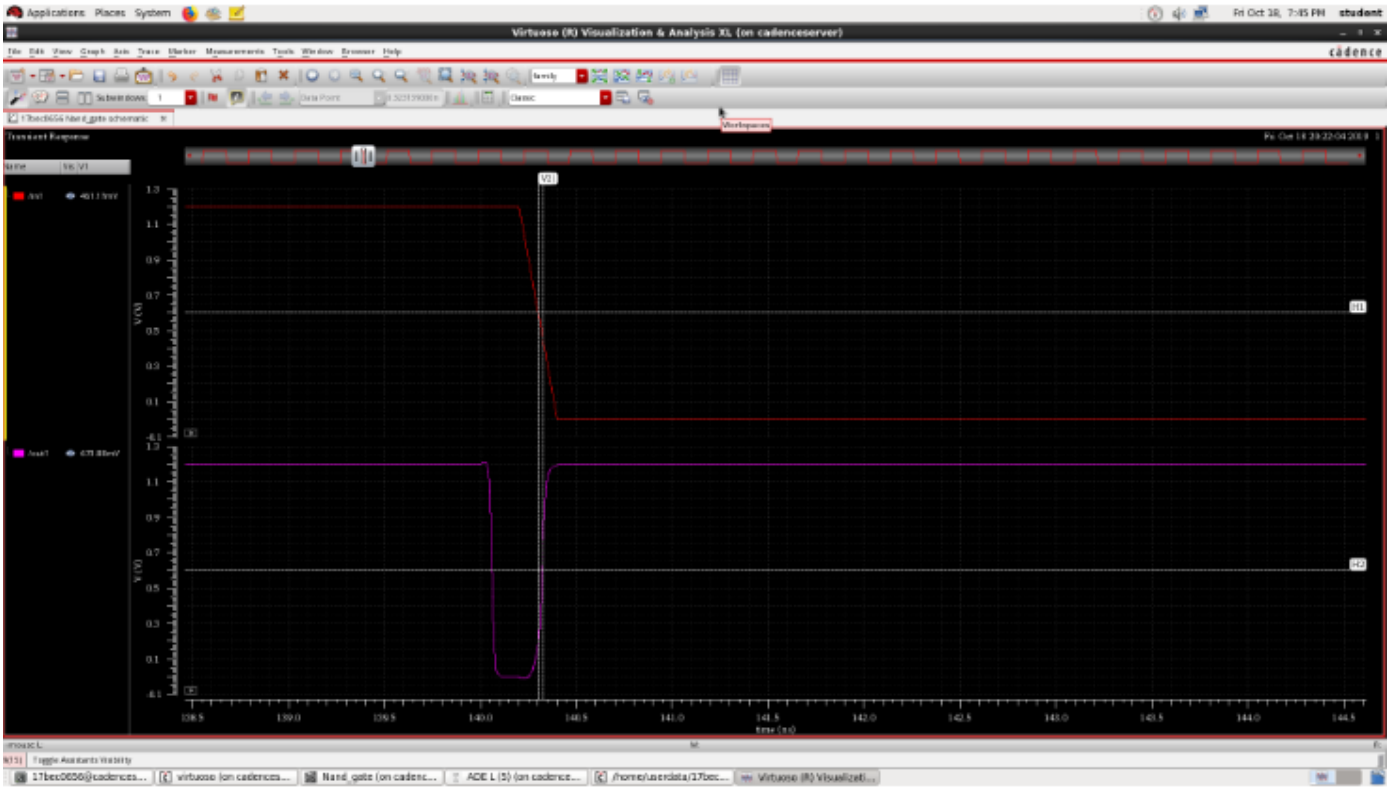
Characterstics of input and output



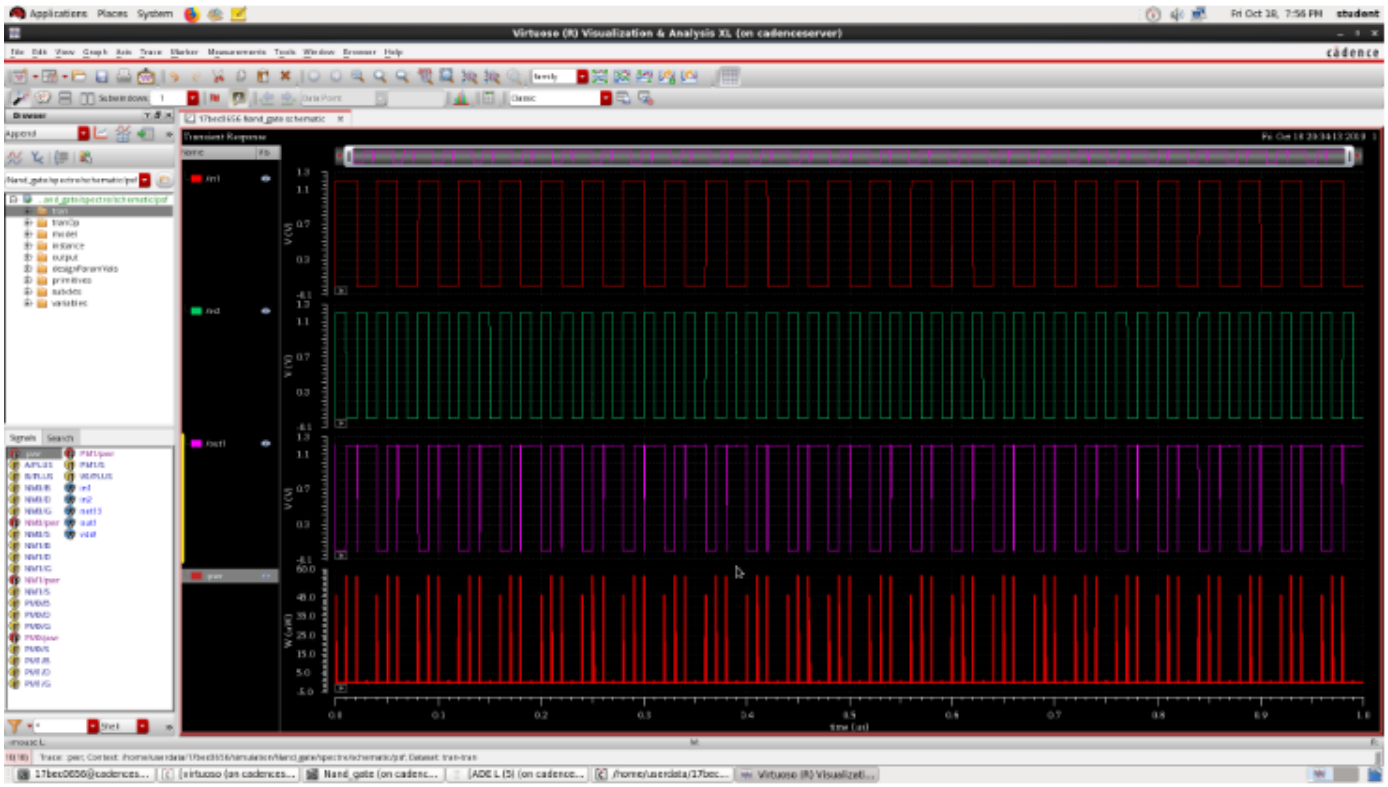
Delay calculation(rise time)



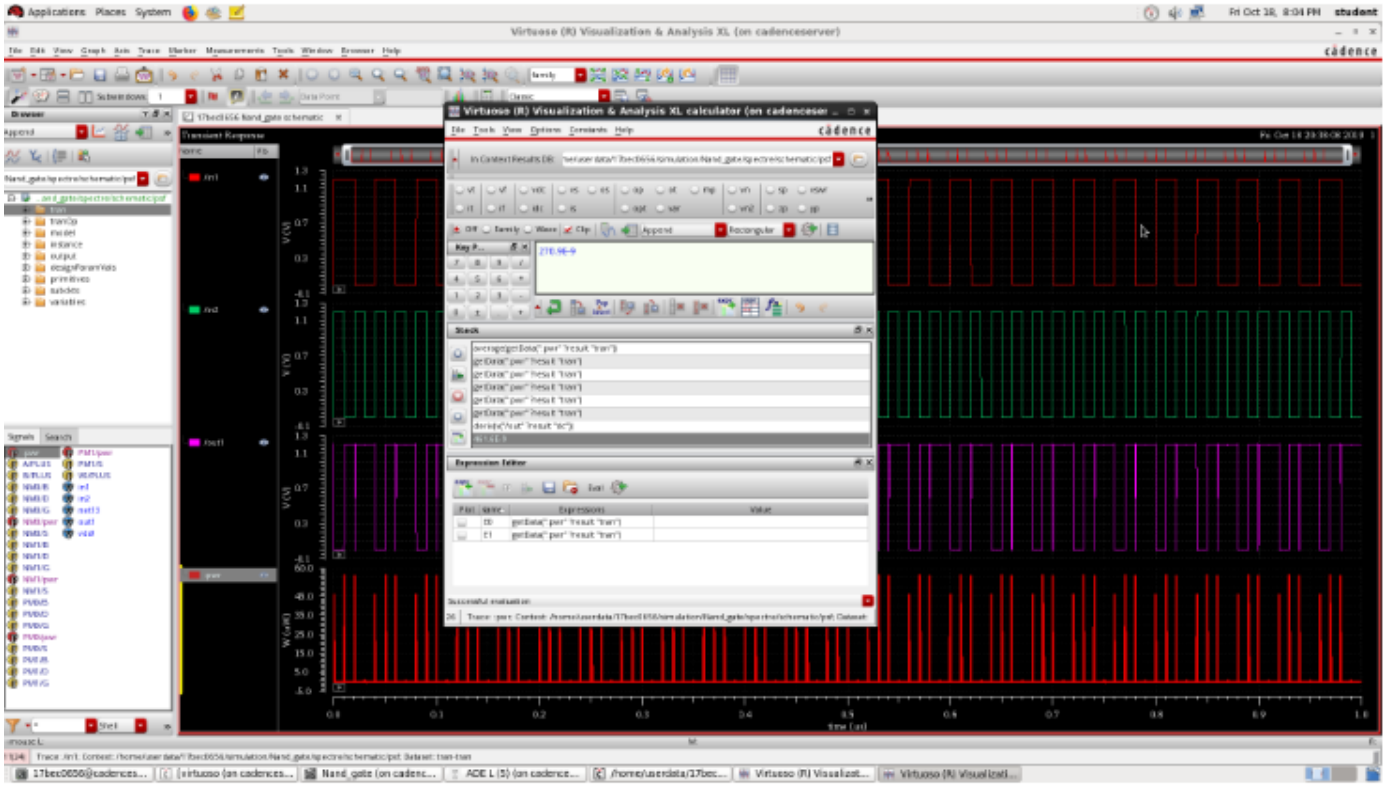
Delay calculation(fall time)



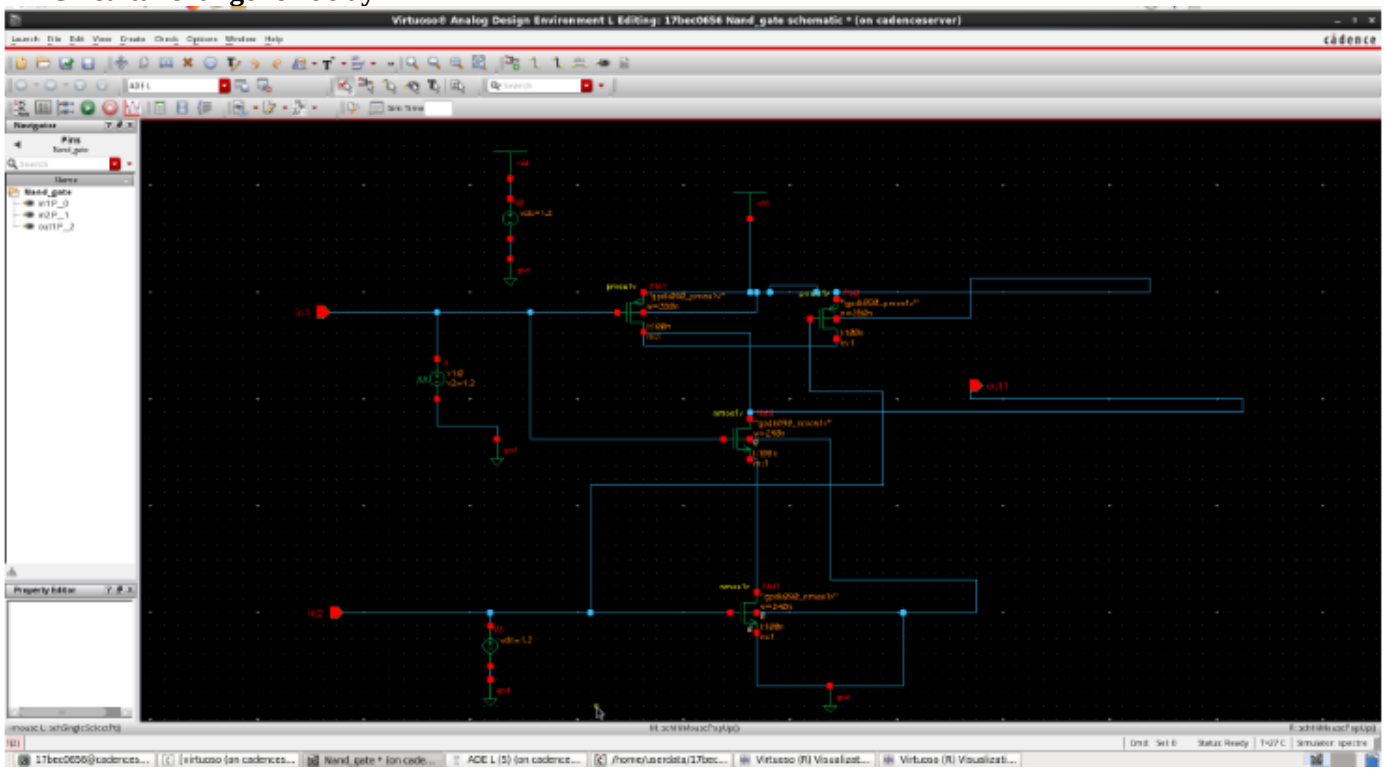
Power calculation



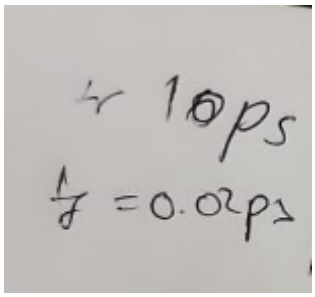
Average power value



Circuital change for delay



Calculation



Inference

Rise time=10 ps
Fall time= 0.02ns
Propagation delay= 15ps
Average power= 250* 10^(-9) watts

Result

The NAND circuit has been successfully constructed and the output waveforms have been observed using the Virtuoso Cadence Tool Software

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