Document Title

32Kx8 bit Low Power CMOS Static RAM

Revision History

Revision No	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
0.0	Advance information	February 12th 1993	Design target
0.1	Initial draft	November 2nd 1993	Preliminary
1.0	Finalize	September 24th 1994	Final
2.0	Revise - Add 45ns part with 30pF test load	August 12th 1995	Final
3.0	Revise - Change specification format and merge: Commercial, Extended, Industrial product in same datasheets.	April 15th 1996	Final
4.0	Revise - Change Speed bin Erase 45ns part from commercial product and 100ns from extended and industrial product Production change Erase Low power product from TSOP package	December 19 1997	Final

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32Kx8 bit Low Power CMOS Static RAM

FEATURES

• Process Technology : 0.7µm CMOS

• Organization: 32Kx8

Power Supply Voltage: Single 5V±10%
Low Data Retention Voltage: 2V(Min)
Three state output and TTL Compatible
Package Type: 28-DIP-600, 28-SOP-450, 28-TSOP1 -0813.4F/R

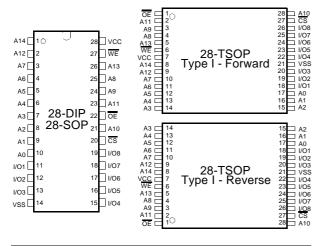
GENERAL DESCRIPTION

The KM62256C family is fabricated by SAMSUNG's advanced CMOS process technology. The family supports various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

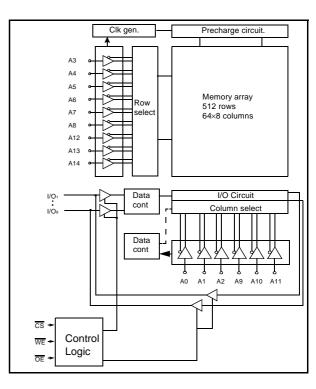
				Power Dissipation		
Product Family	Operating Temperature.	Speed(ns)	PKG Type	Standby (ISB1, Max)	Operating (Icc2)	
KM62256CL	Commercial (0~70°C)	55/70ns	28-DIP, 28-SOP	100μΑ		
KM62256CL-L	Commercial (0~70 C)	33/70118	28-TSOP I R/F	20μΑ		
KM62256CLE	Extended (-25~85°C)	70ns	28-SOP	100μΑ	70mA	
KM62256CLE-L	Exterided (-25~05 C)	70113	28-TSOP I R/F	50μΑ	7 OHIA	
KM62256CLI	Industrial (-40~85°C)	70ns	28-SOP	100μΑ		
KM62256CLI-L		70115	28-TSOP I R/F	50μΑ		

PIN DESCRIPTION



NameName	Function
A0~A14	Address Inputs
WE	Write Enable Input
CS	Chip Select Input
ŌĒ	Output Enable Input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power(5V)
Vss	Ground

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Commercial Temp Product (0~70°C)			Temp Products 5~85°C)	Industrial Temp Products (-40~85°C)			
Part Name	Part Name Function		Part Name Function		Function		
KM62256CLG-7L KM62256CLTG-5L KM62256CLTG-7L KM62256CLRG-5L	28-DIP, 55ns, L-pwr 28-DIP, 55ns, LL-pwr 28-DIP, 70ns, LL-pwr 28-DIP, 70ns, LL-pwr 28-SOP, 55ns, LL-pwr 28-SOP, 55ns, LL-pwr 28-SOP, 70ns, LL-pwr 28-TSOP F, 55ns, LL-pwr 28-TSOP F, 55ns, LL-pwr 28-TSOP R, 55ns, LL-pwr 28-TSOP R, 55ns, LL-pwr 28-TSOP R, 55ns, LL-pwr 28-TSOP R, 70ns, LL-pwr	•	28-SOP, 70ns, L-pwr 28-SOP, 70ns, LL-pwr 28-TSOP F, 70ns, LL-pwr 28-TSOP R, 70ns, LL-pwr	KM62256CLGI-7 KM62256CLGI-7L KM62256CLTGI-7L KM62256CLRGI-7L	28-SOP, 70ns, L-pwr 28-SOP, 70ns, LL-pwr 28-TSOP F, 70ns, LL-pwr 28-TSOP R, 70ns, LL-pwr		

Note: LL means Low Low standby current.

FUNCTIONAL DESCRIPTION

<u>cs</u>	ŌĒ	WE	I/O Pin	Mode	Power
Н	X	Х	High-Z	Deselected	Standby
L	Н	Н	High-Z	Output Disabled	Active
L	L	Н	Dout	Read	Active
L	Х	L	Din	Write	Active

^{1.} X means don't care

ABSOLUTE MAXIMUM RATINGS 1)

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	VIN,VOUT	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.5 to 7.0	V	-
Power Dissipation	PD	1.0	W	-
Storage temperature	Тѕтс	-65 to 150	°C	-
		0 to 70	°C	KM62256CL
Operating Temperature	TA	-25 to 85	°C	KM62256CLE
		-40 to 85	°C	KM62256CLI
Soldering temperature and time	TSOLDER	260°C, 10sec(Lead Only)	-	-

^{1.} Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional opeation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect evice reliability.



RECOMMENDED DC OPERATING CONDITIONS 1)

ltem	Symbol	Min	Тур	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	VIH	2.2	-	Vcc+0.5V ²⁾	V
Input low voltage	VIL	-0.5 ³⁾	-	0.8	V

Note

1. Commercial Product : Ta=0 to 70° C, unless otherwise specified Extended Product : Ta=-25 to 85°C, unless otherwise specified Industrial Product: TA=-40 to 85°C, unless otherwise specified

2. Overshoot : V_{CC}+3.0V in case of pulse width≤30ns

3. Undershoot : -3.0V in case of pulse width≤30ns
4. Overshoot and undershoot is sampled, not 100% tested

CAPACITANCE 1) (f=1MHz, TA=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	VIN=0V	-	6	pF
Input/Output capacitance	Сю	VIO=0V	-	8	pF

^{1.} Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Ite	m	Symbol	Test Conditions			Тур	Max	Unit
Input leakage cur	rent	lu	VIN=Vss to Vcc		-1	-	1	μΑ
Output leakage cu	urrent	ILO	CS=VIH or WE=VIL, VIO=Vss to Vcc		-1	-	1	μΑ
Operating power	supply current	Icc	IIO=0mA, CS=VIL, VIN=VIH or VIL		-	7	15 ¹⁾	mA
Average operating current		Icc1	Cycle time=1μs, 100% duty, Iιο=0mA CS≤0.2V, Vιν≤0.2V, Vιν≥Vcc -0.2V		-	-	7 ²⁾	mA
		ICC2	Cycle time=Min,100% duty, lio=0mA, CS=VIL, VIN=VIH or VIL		-	-	70	mA
Output low voltage	е	Vol	OL IOL=2.1mA		-	-	0.4	V
Output high voltage	је	Voн	IOH=-1.0mA		2.4	-	-	V
Standby Current(ΓTL)	IsB	CS=VIH, Other inputs=VIH or VIL		-	-	1 ³⁾	mA
	KM62256CL KM62256CL-L			L(Low Power) LL(L Low Power)	-	2 1	100 20	μА
Standby Current (CMOS)	KM62256CLE KM62256CLE-L	ISB1	CS≥Vcc-0.2V, Other inputs=0~Vcc	L(Low Power) LL(L Low Power)	-	-	100 50	μА
	KM62256CLI KM62256CLI-L			L(Low Power) LL(L Low Power)	-	-	100 50	μА

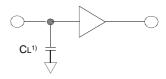
- 1. 20mA for Extended and Industrial Products
- 2. 10mA for Extended and Industrial Products
- 3. 2mA for Extended and Industrial Products



AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level: 0.8 to 2.4V Input rising and falingl time: 5ns input and output reference voltage: 1.5V Output load (See right): CL=100pF+1TTL



1. Including scope and jig capacitance

 $\label{eq:action} \textbf{AC CHARACTERISTICS} (Vcc=4.5~5.5V, KM62256C \ Family: TA=0 \ to \ 70°C, KM62256CE \ Family: TA=-25 \ to \ 85°C, KM62256CI \ Family: TA=-40 \ to \ 85°C)$

				Units			
Parameter List		Symbol	55ns		70ns		
			Min	Max	Min	Max	
	Read cycle time	trc	55	-	70	-	ns
	Address access time	taa	-	55	-	70	ns
	Chip select to output	tco	-	55	-	70	ns
	Output enable to valid output	toe	-	25	-	35	ns
Read	Chip select to low-Z output	tLZ	10	-	10	-	ns
	Output enable to low-Z output	toLz	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	20	0	30	ns
	Output disable to high-Z output	tonz	0	20	0	30	ns
	Output hold from address change	tон	5	-	5	-	ns
	Write cycle time	twc	55	-	70	-	ns
	Chip select to end of write	tcw	45	-	60	-	ns
	Address set-up time	tas	0	-	0	-	ns
	Address valid to end of write	taw	45	-	60	-	ns
Write	Write pulse width	twp	40	-	50	-	ns
vviile	Write recovery time	twr	0	-	0	-	ns
	Write to output high-Z	twnz	0	20	0	25	ns
	Data to write time overlap	tow	25	-	30	-	ns
	Data hold from write time	tDH	0	-	0	-	ns
	End write to output low-Z	tow	5	-	5	-	ns

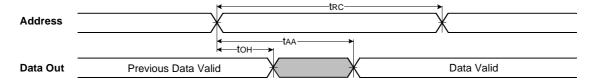
DATA RETENTION CHARACTERISTICS

Item		Symbol	Test Condition		Min	Тур	Max	Unit
Vcc for data retention	Vdr		CS≥Vcc-0.2V		2.0	-	5.5	٧
	IDR KN	KM62256CL KM62256CL-L	Vcc=3.0V CS ≥Vcc-0.2V	L-Ver LL-Ver	-	1 0.5	50 10	μΑ
Data retention current		KM62256CLE KM62256CLE-L		L-Ver LL-Ver	-	-	50 25	
		KM62256CLI KM62256CLI-L		L-Ver LL-Ver	-	-	50 25	
Data retention set-up time	tsdr		See data retention waveform		0	-	-	ms
Recovery time	trdr				5	-	-	1113

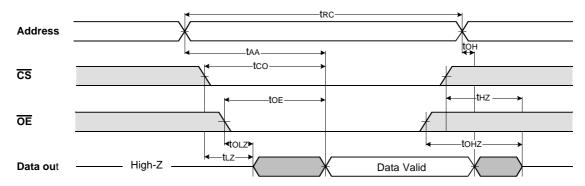


TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$)



TIMING WAVEFORM OF READ CYCLE(2) (WE=VIH)

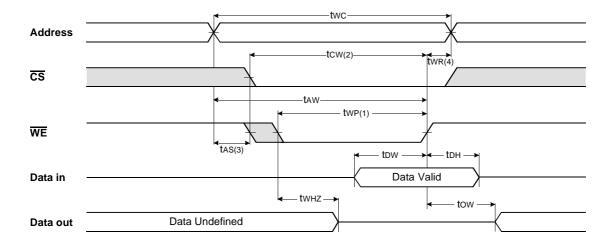


NOTES (READ CYCLE)

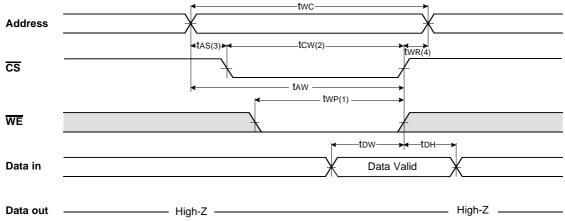
- 1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- 2. At any given temperature and voltage condition, tHZ(Max.) is less than tLZ(Min.) both for a given device and from device to device interconnection.



TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)



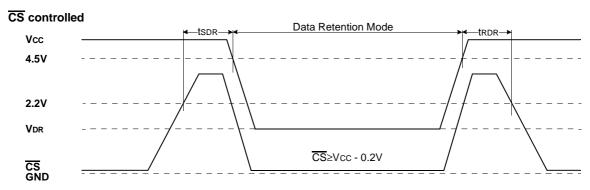
TIMING WAVEFORM OF WRITE CYCLE(2) (CS Controlled)



NOTES (WRITE CYCLE)

- 1. A write occurs during the overlap of a low \overline{CS} and a low \overline{WE} . A write begins at the latest transition among \overline{CS} going Low and \overline{WE} going low: A write end at the earliest transition among \overline{CS} going high and \overline{WE} going high, two is measured from the begining of write to the end of write.
- 2. tcw is measured from the $\overline{\text{CS}}$ going low to end of write.
- 3. tAS is measured from the address valid to the beginning of write.
- 4. two is measured from the end of write to the address change. two applied in case a write ends as CS or WE going high.

DATA RETENTION WAVE FORM



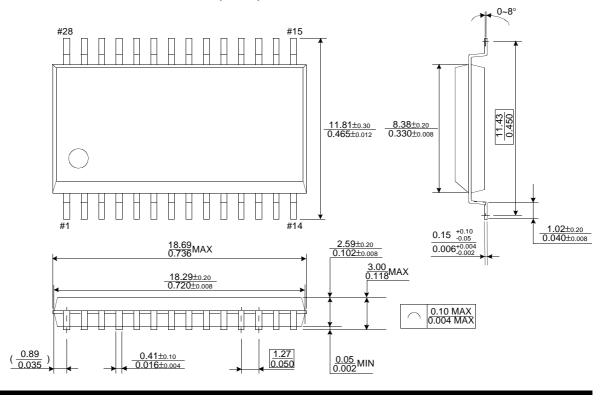


PACKAGE DIMENSIONS 28 PIN DUAL INLINE PACKAGE(600mil) 13.60±0.20 0.535±0.008 #10 36.72 14.446 MAX 36.32±0.20 1.430±0.008 36.32±0.20 1.430±0.008 36.32±0.20 1.430±0.008 36.32±0.20 1.430±0.008 36.32±0.20 1.430±0.008 36.32±0.20 1.430±0.008 36.32±0.20 1.430±0.008 36.32±0.20 1.430±0.008 36.32±0.20 1.430±0.008 36.32±0.20 1.430±0.008

28 PIN PLASTIC SMALL OUTLINE PACKAGE(450mil)

1.52±0.10 0.060±0.004

 $(\frac{1.65}{0.065}$

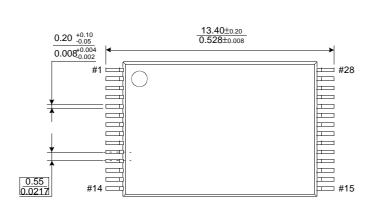


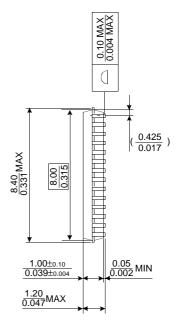
0.38 MIN

PACKAGE DIMENSIONS

Units:millimeters(inches)

28 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4F)





28 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4R)

