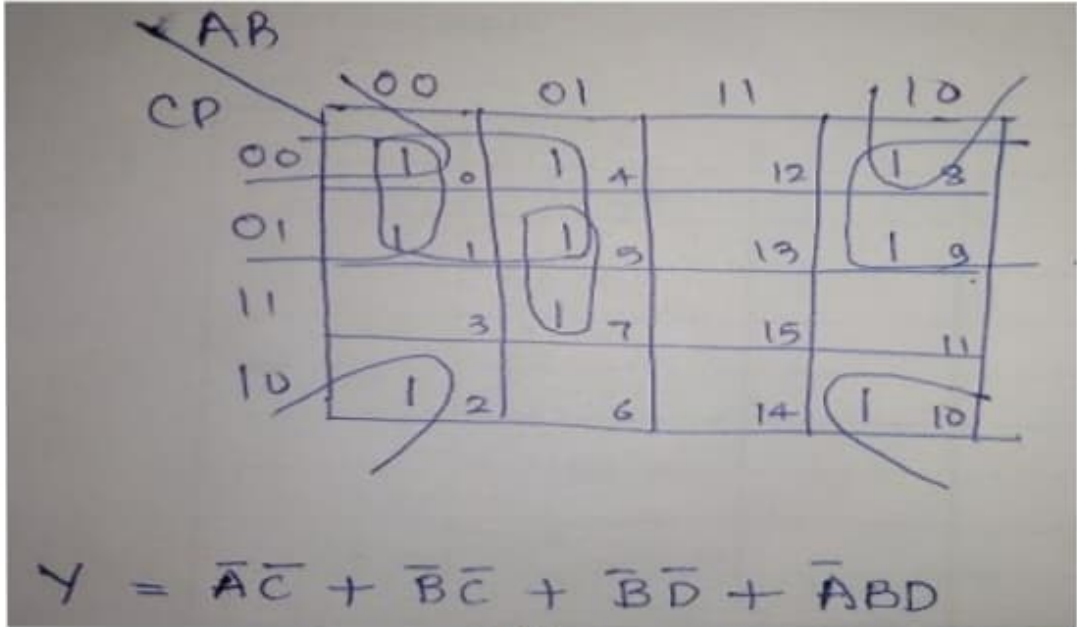
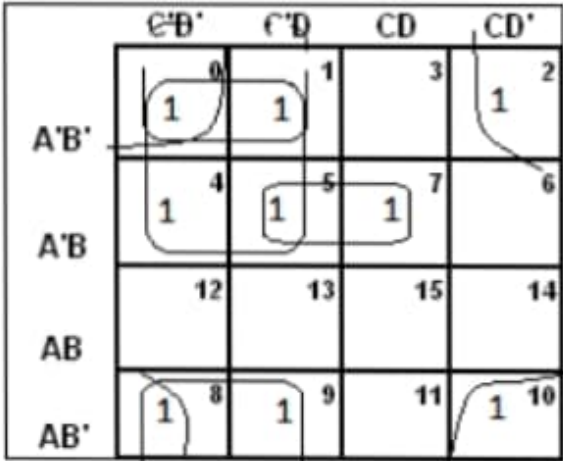
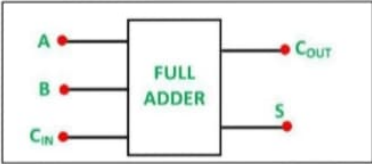


c)	Write simple example of Boolean expression for SOP and POS.
Ans:	<p><u>SOP form:</u></p> $Y = AB + BC + A\bar{C}$ <p><u>POS form:</u></p> $Y = (A + B)(B + C)(A + \bar{C})$
d)	State the necessity of multiplexer.
Ans:	<p><u>Necessity of Multiplexer:</u></p> <ul style="list-style-type: none"> • It reduces the number of wires required to pass data from source to destination. • For minimizing the hardware circuit. • For simplifying logic design. • In most digital circuits, many signals or channels are to be transmitted, and then it becomes necessary to send the data on a single line simultaneously. • Reduces the cost as sending many signals separately is expensive and requires more wires to send.

d)	Minimize the following expression using K-Map. $f(A, B, C, D) = \sum m(0, 1, 2, 4, 5, 7, 8, 9, 10)$	4M
----	--------------------------------------------------------------------------------------------------------	----

Ans:	 <p style="text-align: center;">OR</p>  <p style="text-align: center;">$\bar{A}\bar{C} + \bar{B}\bar{C} + \bar{B}\bar{D} + \bar{A}BD$</p>	<p>1 M – drawing k map</p> <p>1 M – Representing function in k map</p> <p>1 M – Grouping</p> <p>1M – Final expression</p>
------	---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------	---------------------------------------------------------------------------------------------------------------------------

b)	Describe the function of full Adder Circuit using its truth table, K-Map simplification and logic diagram.	4M
Ans:	<p>(Diagram- 1M, Truth table-1M, K-map- 1M, Logic diagram-1 M)</p> <p>A full adder is a combinational logic circuit that performs addition between three bits, the two input bits A and B, and carry C from the previous bit.</p> <p>Block diagram :</p> 	<p>1M</p> <p>1M</p>

Page



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Truth Table :

Input			Output	
A	B	C _{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

1M

K-Map :-

For Carry (C_{out})

For Sum

BC _{in}	00	01	11	10
A				
0	0	0	1	0
1	0	1	1	1

BC _{in}	00	01	11	10
A				
0	0	1	0	1
1	1	0	1	0

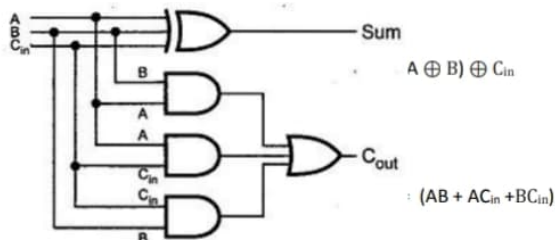
1M

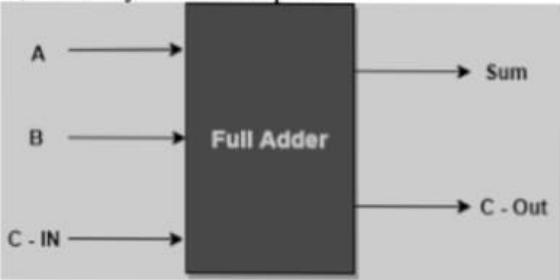
$$C_{out} = AB + A C_{in} + B C_{in}$$

$$Sum = \bar{A} \bar{B} C_{in} + \bar{A} B \bar{C}_{in} + A \bar{B} \bar{C}_{in} + A B C_{in}$$

Logic Diagram:

(Note: Logic Diagram using basic or universal gate also can be consider)



a)	Design a full Adder using Truth Table and K-map.	4M																																																		
Ans:	<p>A full adder is a combinational logic circuit that performs addition between three bits, the two input bits A and B, and carry C from the previous bit.</p> <div></div> <p>Truth Table:</p> <table><thead><tr><th colspan="3">Input</th><th colspan="2">Output</th></tr><tr><th>A</th><th>B</th><th>Cin</th><th>Sum</th><th>Carry</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr></tbody></table>	Input			Output		A	B	Cin	Sum	Carry	0	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	1	1	0	1	1	0	0	1	0	1	0	1	0	1	1	1	0	0	1	1	1	1	1	1	<p>Truth table 1½ M</p>
Input			Output																																																	
A	B	Cin	Sum	Carry																																																
0	0	0	0	0																																																
0	0	1	1	0																																																
0	1	0	1	0																																																
0	1	1	0	1																																																
1	0	0	1	0																																																
1	0	1	0	1																																																
1	1	0	0	1																																																
1	1	1	1	1																																																



K-map simplification for carry and sum

For Carry (C_{out})

BC_{in}	00	01	11	10
0	0	0	1	0
1	0	1	1	1

$$C_{out} = AB + A C_{in} + B C_{in}$$

For Sum

BC_{in}	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$$Sum = \bar{A} \bar{B} C_{in} + \bar{A} B \bar{C}_{in} + A \bar{B} \bar{C}_{in} + A B C_{in}$$

Logical diagram:

```

graph LR
    A --- AND1[AND]
    B --- AND1
    AND1 --- OR2[OR]
    A --- AND2[AND]
    Cin --- AND2
    AND2 --- OR1[OR]
    B --- AND3[AND]
    Cin --- AND3
    AND3 --- OR1
    OR1 --- Cout[C_out]
    OR2 --- Sum[Sum]
  
```

Fig. 3.17 Implementation of full-adder

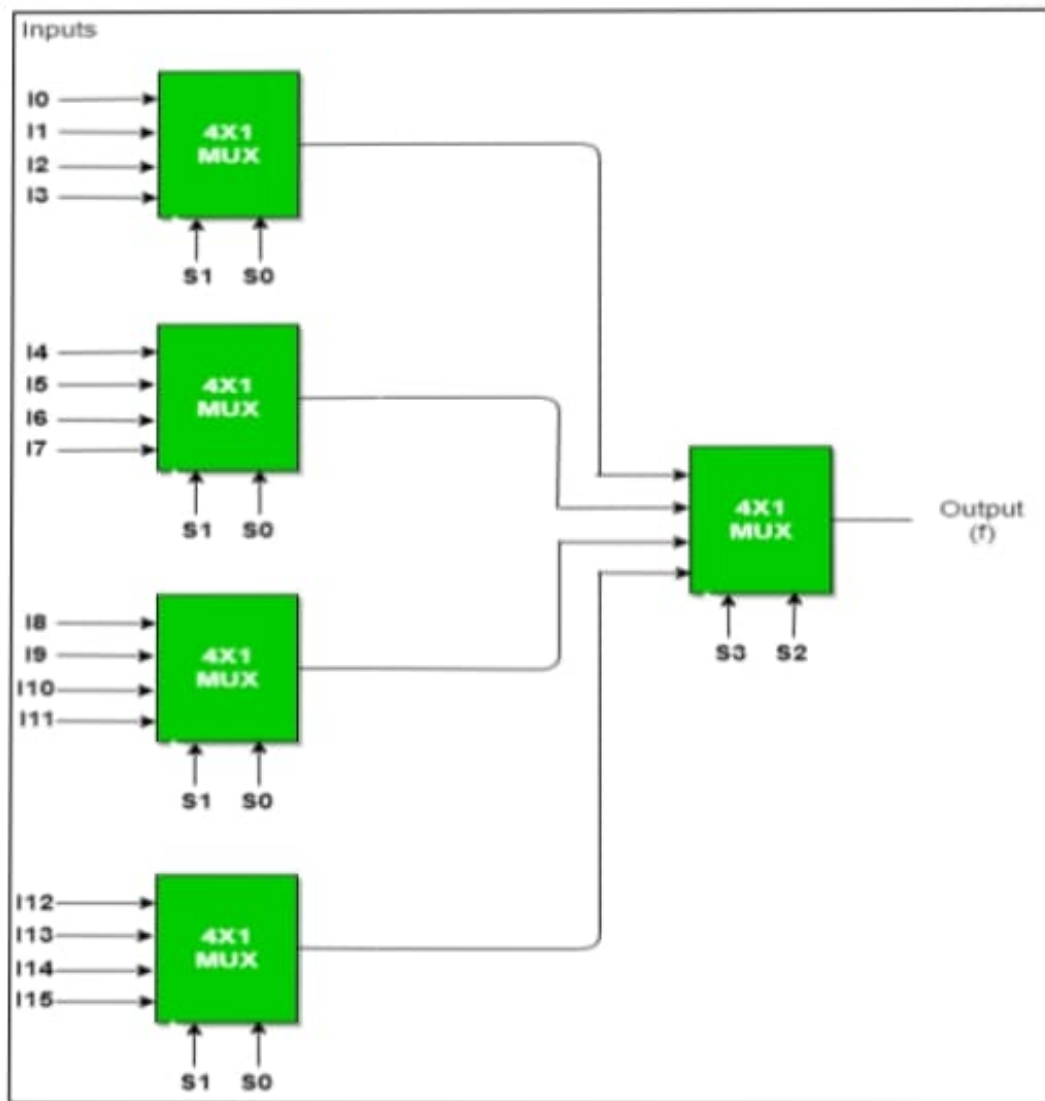
1M

1½ M

b) Draw 16:1 MUX tree using 4:1 MUX.

4M

Ans: Diagram :-



4M

a) Design 4 bit Binary to Gray code converter.

6M

Ans:

2M for truth table

1/2m for each output equation
2M for realization using gates

Truth Table for 4 bit Binary to Gray code converter

Binary Input				Gray output			
B ₃	B ₂	B ₁	B ₀	G ₃	G ₂	G ₁	G ₀
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

K-MAP FOR G₃:

B ₁ B ₀		00	01	11	10
B ₃ B ₂	00	0	0	0	0
	01	0	0	0	0
	11	1	1	1	1
	10	1	1	1	1

G₃=B₃

B ₁ B ₀		00	01	11	10
B ₃ B ₂	00	0	0	0	0
	01	1	1	1	1
	11	0	0	0	0
	10	1	1	1	1

K-MAP FOR G2:

$$G2 = \overline{B3} B2 + \overline{B2} B3$$

$$= B3 \text{ XOR } B2$$

K-MAP FOR G1:

B1B0 \ B3B2	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	1	1	0	0
10	0	0	1	1



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$$G1 = \overline{B2} B1 + B2 \overline{B1}$$

$$= B1 \text{ XOR } B2$$

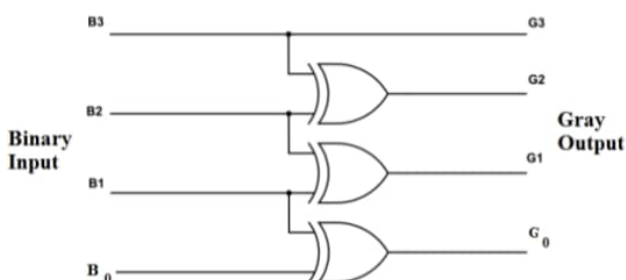
K-MAP FOR G0:

B1B0 \ B3B2	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	0	1	0	1
10	0	1	0	1

$$G0 = \overline{B1} B0 + B1 \overline{B0}$$

$$= B1 \text{ XOR } B0$$

Diagram for 4 bit Binary to Gray code converter:

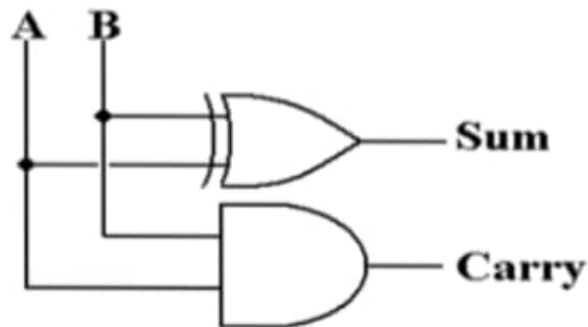


Note: Realization of output equations can be done using Basic or Universal gates

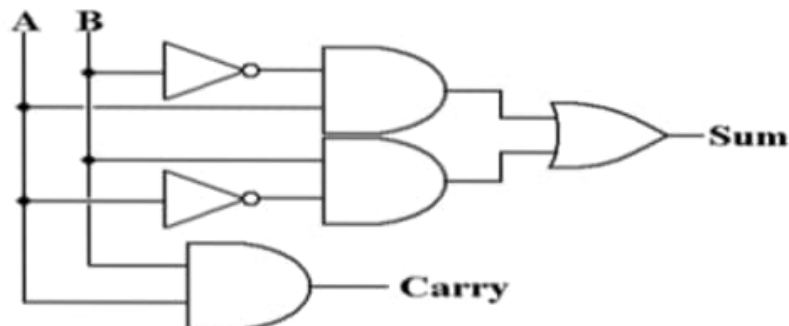
f)	Define encoder, write the IC number of IC used as decimal to BCD encoder.	2M
Ans:	<p>An encoder is a device or circuit that converts information from one format or code to another, for the purpose of standardization, speed or compression.</p> <p>Decimal to BCD encoder IC- 74147</p>	<p>Defination-1M</p> <p>IC-1M</p>

d)	Draw logic diagram of half adder circuit	4M
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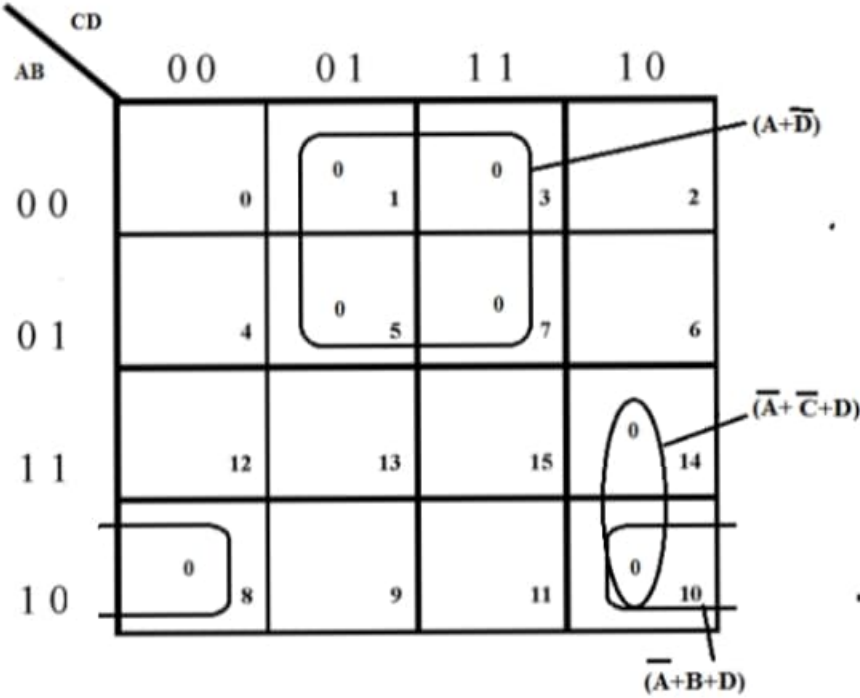
Ans:		4M
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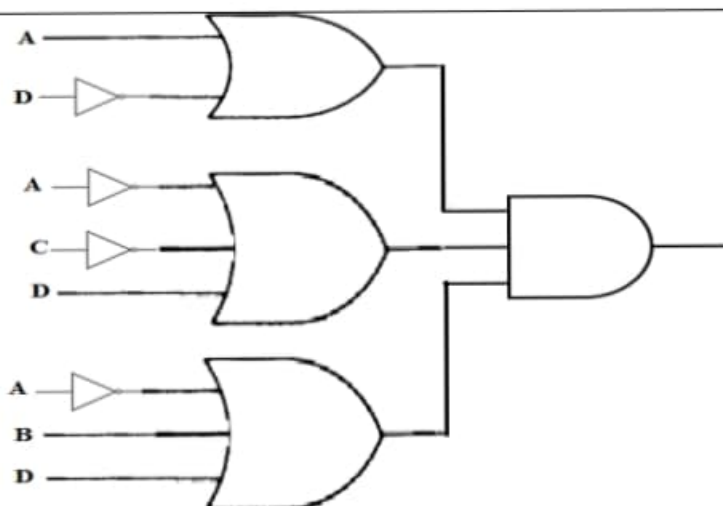


OR



Note: logic diagram using NAND/NOR also can be considered.

(d)	Reduce the following expression using K-map and implement it $F(A,B,C,D) = \prod M(1,3,5,7,8,10,14)$	4M
Ans:	 <p> $F(A,B,C,D) = (A + \bar{D})(\bar{A} + \bar{C} + D)(\bar{A} + B + \bar{D})$ </p>	Kmap-1M Pairs-1.5M Final Ans-1.5M

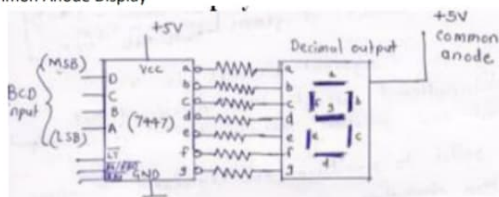




Ans: Note: Any one type of display shall be considered

1. BCD to 7 segment decoder is a combinational circuit that accepts 4 bit BCD input and generates appropriate 7 segment output.
2. In order to produce the required numbers from 0 to 9 on the display the correct combination of LED segments need to be illuminated.
3. A standard 7 segment LED display generally has 8 input connections, one from each LED segment & one that acts as a common terminal or connection for all the internal segments
4. Therefore there are 2 types of display 1. Common Anode Display 2. Common Cathode Display :

Common Anode Display



for normal functioning \overline{LT} , $\overline{BI}/\overline{RBO}$ & \overline{RBI} should be connected to logic 1

Truth Table

for seven segment decoder using common anode display

BCD Inputs				7 segment coded outputs							Display outputs
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	1	0	0	1	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0	0
0	0	1	1	0	0	0	0	1	1	0	0
0	1	0	0	1	0	0	1	1	0	0	0
0	1	0	1	0	1	0	0	1	0	0	0
0	1	1	0	1	1	0	0	0	0	0	0
0	1	1	1	0	0	0	1	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	1	1	0	0	0

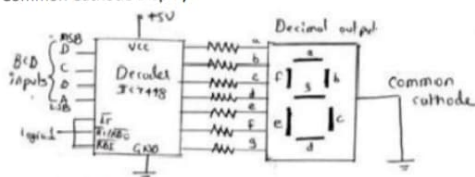
Explanation 2M

Circuit Diagram 2M

Truth Table 2M



Common Cathode Display:



Truth Table

BCD inputs				7 segment coded outputs							Display outputs
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	0	1	0
0	0	0	1	0	1	1	0	0	0	0	1
0	0	1	0	1	1	0	1	1	0	1	0
0	0	1	1	1	1	1	1	0	0	1	1
0	1	0	0	0	1	1	0	0	1	1	0
0	1	0	1	1	0	1	1	0	1	1	0
0	1	1	0	0	0	1	1	1	1	1	0
0	1	1	1	1	1	1	0	0	0	0	1
1	0	0	0	1	1	1	1	1	1	1	0
1	0	0	1	1	1	1	0	0	1	1	0

	d)	Convert the following expression into standard SOP form. $Y = AB + A\bar{C} + BC$	2M
	Ans:	$Y = AB + A\bar{C} + BC$ Total variable ABC 1 st Product term = AB (C is missing) 2 nd Product term = $A\bar{C}$ (B is missing) 3 rd Product term = BC (A is missing) $Y = AB \bullet 1 + A\bar{C} \bullet 1 + BC \bullet 1$ $Y = AB(C + \bar{C}) + A\bar{C}(B + \bar{B}) + BC(A + \bar{A})$ $Y = \underline{ABC} + \underline{AB\bar{C}} + \underline{A\bar{B}C} + \underline{A\bar{B}\bar{C}} + \underline{\bar{A}BC} + \bar{A}\bar{B}C$ $(\because A + \bar{A} = 1)$ $Y = ABC + AB\bar{C} + A\bar{B}C + \bar{A}BC$ Standard SOP Form	2M
			2M

c)	Minimize the four variable logic function using K map. $F(A,B,C,D) = \sum m(0,1,2,3,5,7,8,9,11,14)$	4M
Ans:		Kmap with place value-1M Pair-1M Answer- 2M
d)	Implement the following function using demultiplexer. $f_1 = \sum m(0,2,4,6)$ $f_2 = \sum m(1,3,5)$	4M



Ans:	$F_1 = \sum m(0,2,4,6)$ $f_2 = \sum m(1,3,5)$	(4 marks)	4M