UNIVERSITÀ DI PISA

Computer Engineering

Electronics and Communication Systems

CARTESIAN TO POLAR CONVERSION USING CORDIC ALGORITHM IN VECTORING MODE

VHDL decription and Xilinx Vivado Synthesis

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Abstract

This project has been developed during the course of Electronics and Communication Systems. The aim of this project is to demonstrate the knowledge of the VHDL language to design a digital circuit and the use of Xilinx Vivado Tool to synthesize this circuit, and analyze the results achieved.

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