16-February-2017

Custom Implementation FPGA Code Module

I/O pin mapping and driver configuration

I/O Module	IO397_50K
Simulink Real-Time Target Version	R2016b
Reference	speedgoat_IO397_50K_PMSM_DEMO

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real-time simulation and testing

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1 Introduction

This manual is an addendum to the User's Manual you have received with your Real-time target machine (with specific serial number).

Your Real-time target machine is equipped with at least one reconfigurable FPGA I/O module for which a default FPGA bitstream and Simulink Real-Time driver blockset has been provided. See the User's Manual for your Real-time target machine for more information on this.

This manual provides information on how to install, configure, and use the specific (custom) FPGA bitstream and Simulink Real-Time driver blockset you have additionally ordered at the time of your Real-time target machine purchase or also possible, at a later time.

2 Implemented Functionality

This custom FPGA bitstream and Simulink Real-Time driver blockset implements the following functionality:

FPGA Code Module	Transceiver Type	No. of modules / channels
Analog input	Analog	32
Analog output	Analog	8
Analog AD trigger	TTL	4
Analog DA trigger	TTL	1
Digital input/output	TTL	4
PWM with trigger	TTL	3
QAD with index	TTL	1
PWM capture	TTL	3

Table 1: Implemented functionality IO397_50K-ac Front I/O

3 Software Installation

The software installation for this custom FPGA bitstream and Simulink Real-Time driver blockset must be installed after the MathWorks software standard installation and the Speedgoat library (speedgoatlib). Therefore, the steps are as follows:

1. Download the custom implementation for your I/O module and Matlab R2016b : http://www.speedgoat.ch/downloads/ci/speedgoat_IO397_50K_PMSM_DEMO.zip
2. The archive contains both, the test model (*.slx) and the bitstream (*.mat) of the custom implementation.
3. The content of this archive can be extracted in your current MATLAB workspace. To make the bitstream accessible for all projects and folders, we recommend to add the bitstream in the following directory:

   For Speedgoatlib 8.x.x:
   [matlabroot]\toolbox\rtw\targets\xpc\target\build\xpcblocks\thirdpartydrivers\sg_bitstream

Note: After placing the bitstream file into the *thirdpartydrivers*-folder, please do not forget to type **rehash toolbox** in your MATLAB Command Window!

4 I/O Pin mapping

The I/O pin mapping for this custom FPGA bitstream implementation is shown below. This I/O pin mapping is specific to the reconfigurable FPGA module for which it has been designed and is the reference on how you connect the pins to your hardware under test.

Attention: Speedgoat delivers real-time target machines together with terminal boards pre-wired for the default FPGA bitstream implementation (see User's Manual of your target machine). Therefore, the wires of the terminal board for the reconfigurable FPGA I/O module have to be wired as described in section 7.2 of this document to execute the test model for this specific implementation.

Note: Current sense inputs are captured in synchronization with the PWM signals. This is handled via an internal FPGA connection that interconnects ADC trigger lines with the PWM trigger of Leg A. The PWM trigger is issued at half of the PWM period. PWM and ADC trigger lines, are not accessible from the IO397 pins.

4.1 Front I/O

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Proposed FPGA pin mapping for IO397 I/O module

Terminal board 1: digital I/O

Pin	Code Module Channel	Functionality	Direction	Transceiver	Port	Pull Resistors
13	1	GND		TTL		
14	1	GND		TTL		
15	1	GPIO	IN/OUT	TTL		
16	1	PWM - A	OUT	TTL		
17	1	PWM - Trigger		TTL		
18	2	PWM - A	OUT	TTL		
19	3	PWM - A	OUT	TTL		
20	2	GPIO	IN/OUT	TTL		
21	3	GPIO	IN/OUT	TTL		
22	4	GPIO	IN/OUT	TTL		
23	1	QAD - A	OUT	TTL		
24		QAD - B		TTL		
25		QAD - C/Index		TTL		
26	1	CAP	IN	TTL		
27	2	CAP	IN	TTL		
28	3	CAP	IN	TTL		
29	1	GND		TTL		
30	1	GND		TTL		pull-up 3.3 VDC

Terminal board 2: analog I/O

Pin	Single-ended	Differential	Analog
1	Analog input 01	Analog input 01 (+)	
2	GND	Analog input 01 (-)	
3	Analog input 02	Analog input 02 (+)	
4	GND	Analog input 02 (-)	
5	Analog input 03	Analog input 03 (+)	ADC
6	GND	Analog input 03 (-)	
7	Analog input 04	Analog input 04 (+)	
8	GND	Analog input 04 (-)	
9	Analog Output 01	(-)	
10	Analog output 02	(-)	
11	Analog Output 03	(-)	DAC
12	Analog Output 04	(-)	

Figure 1: Pinout front plug-in IO397_50K-ac

5 Simulink Driver Library

To open the library blocks for the custom FPGA bitstream, type
» `speedgoatlib_IO397_50K_PMSM_DEMO`

at the MATLAB command line prompt. The blockset looks as follows:

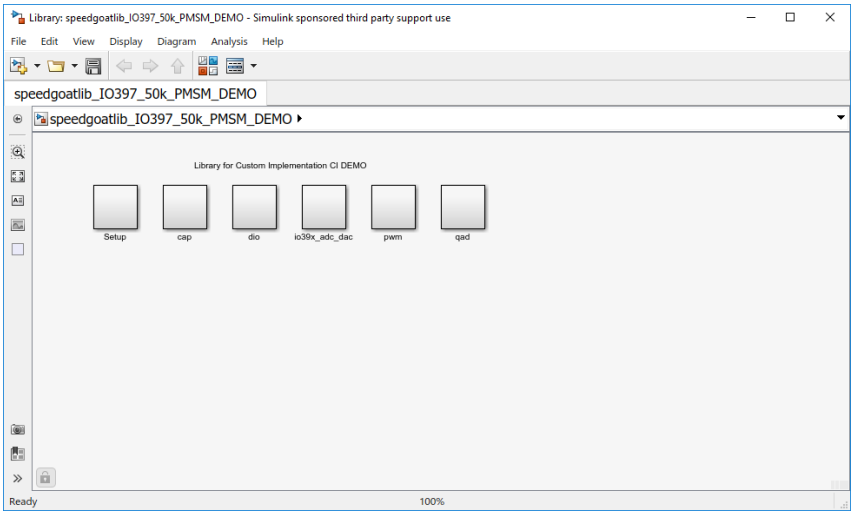

Figure 2: Library for Custom Implementation DEMO

6 Bitstream

Using this custom Speedgoat FPGA bitstream and driver blocks is basically identical to using the default FPGA bitstream, as described in the speedgoatlib_fpga User's Manual. The only difference is the configuration of the Setup driver block:

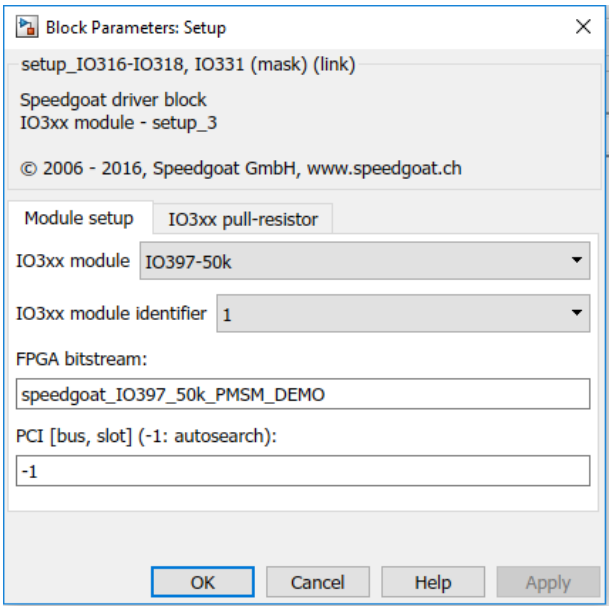

Figure 3: IO397_50K, select I/O module, front I/O plug-in module, rear I/O conditioning module and Custom Implementation Bitstream

7 Test Model

7.1 Test Model description

To test the custom set of FPGA Code Modules, a dedicated test model is included. Note that this test model only tests I/O channels for which the loopback test method is possible. It is required to pre-wire the provided terminal board as described in chapter 7.2 of this manual. The test model doesn't exercise I/O channels requiring additional external hardware. Nevertheless executing this test model will confirm the correct set-up of this implementation.

To open the test model type:
» `speedgoat_IO397_50K_PMSM_DEMO`

at the MATLAB command line prompt. The model looks as follows:

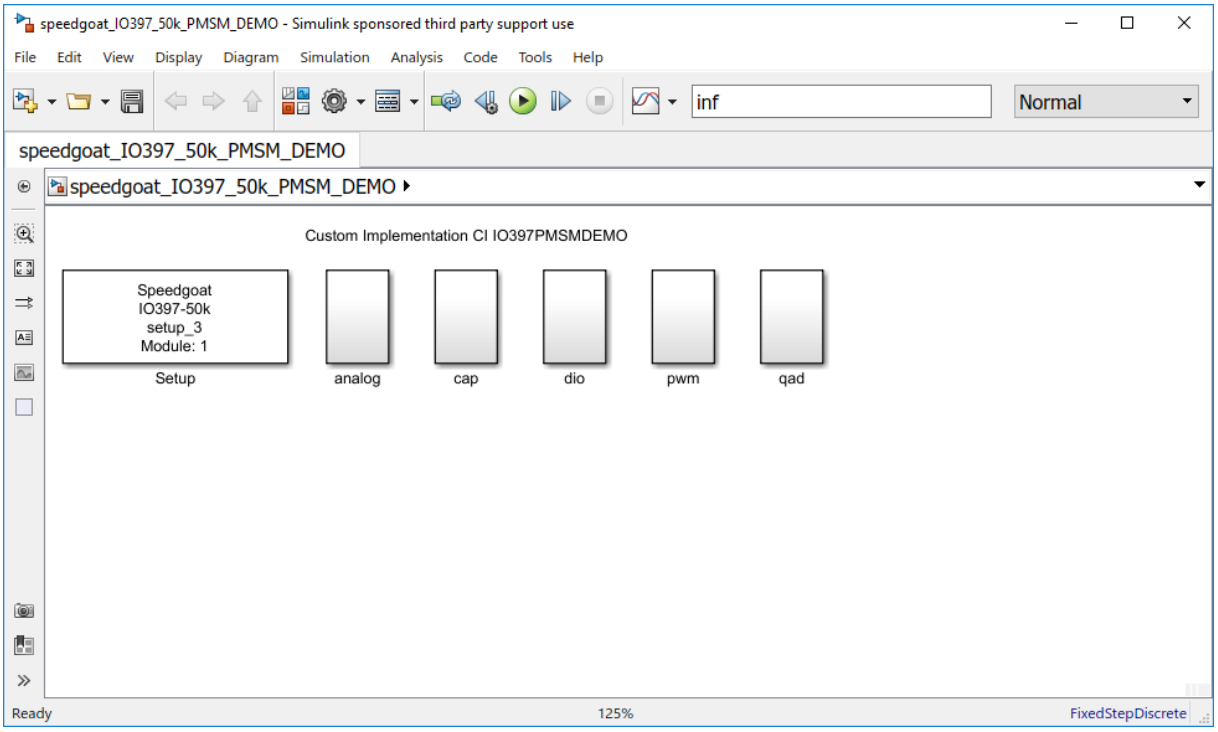

Figure 4: speedgoat_IO397_50K_PMSM_DEMO

7.2 Required test wiring of the terminal board

Front I/O (Analog):

From Pin	To Pin	Tested functionality
9	1	VOUT01 - VIN01 (+) ADC01
10	3	VOUT02 - VIN02 (+) ADC01
11	5	VOUT03 - VIN03 (+) ADC02
12	7	VOUT04 - VIN04 (+) ADC03
30	2	Ground - VIN01 (-) ADC01
30	4	Ground - VIN02 (-) ADC02
30	6	Ground - VIN03 (-) ADC03
30	8	Ground - VIN04 (-) ADC04

Table 2: Front I/O Terminal Board wiring Analog

Front I/O (Digital):

From Pin	To Pin	Tested functionality
15	21	DO channel 1 - DI channel 3
20	22	DO channel 2 - DI channel 4
16	26	PWM A channel 1 - CAP channel 1
18	27	PWM A channel 2 - CAP channel 2

Table 3: Front I/O Terminal Board wiring

8 Target Screen

If you start the test model (speedgoat_IO397_50K_PMSM_DEMO.slx) with the wired board (according to section 7.2) you see the following target screen.

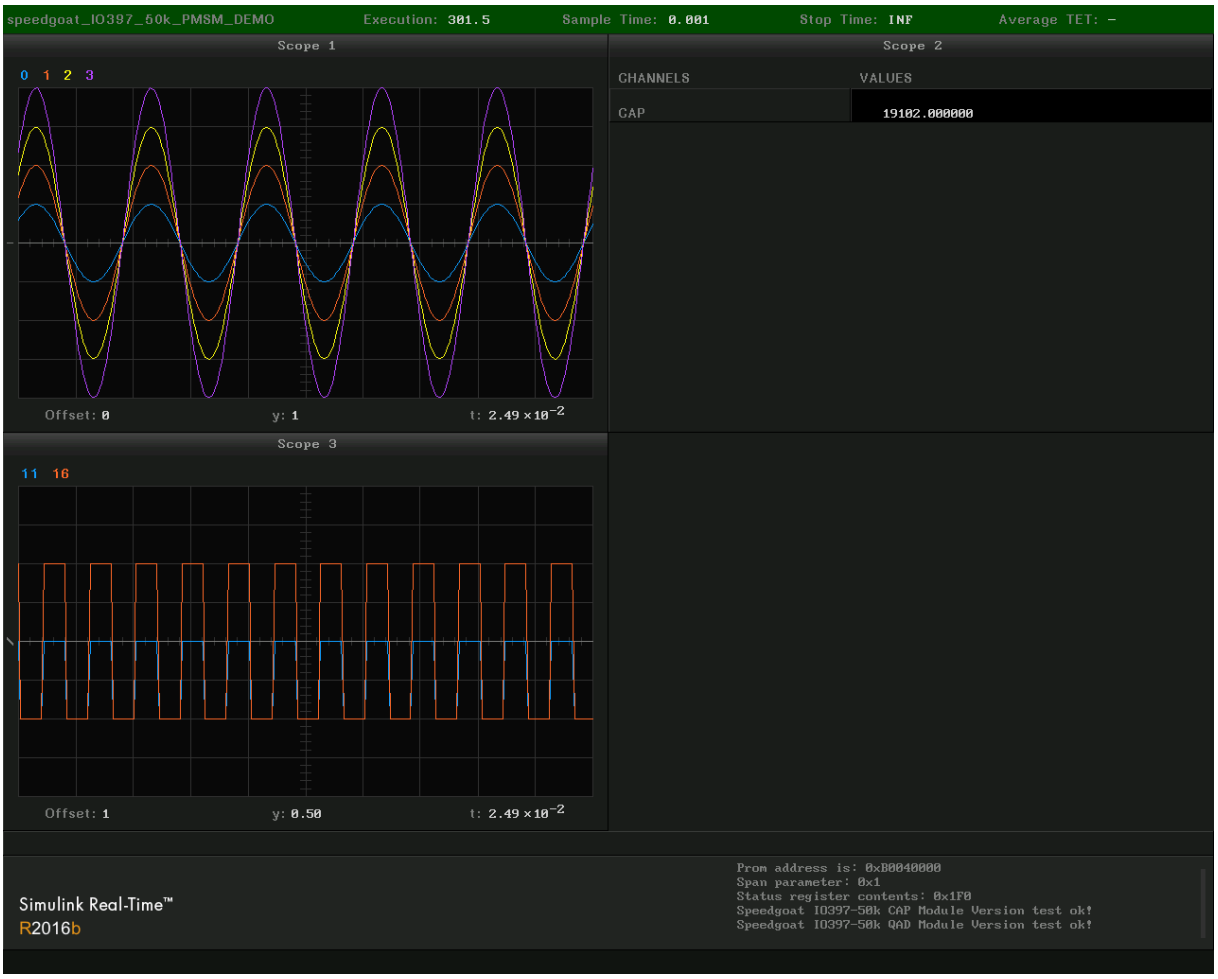

Figure 5: Target Screen with Test Signals