18 August 2020

Custom Implementation Package Manual

I/O pin mapping and driver configuration

I/O Module	IO397_50K
Simulink Real-Time Target Version	R2020a
Minimum Required Speedgoat Library	8.28.2.3
Reference	speedgoat_IO397_50K_CI_02171

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Document Version History

Rev.	Description	Date
1.0	initial version of Custom Implementation Package Manual	18 August 2020

1 Introduction

This manual supplements the User Manual you received with your real-time target machine.

Your real-time target machine is equipped with at least one FPGA I/O module for which a default FPGA bitstream and Simulink Real-Time ™ driver blockset have been provided. Refer to your real-time target machine user manual for more information.

This manual explains how to install, configure, and use the specific (custom) FPGA bitstream and Simulink Real-Time driver blockset you ordered upon purchase of your real-time target machine. Note that the bitstream and driver blockset can also be purchased at a later date.

2 Implemented Functionality

This custom FPGA bitstream and Simulink Real-Time driver blockset implements the following functionality:

FPGA Code Module	Transceiver Type	No.of Modules/Channels	Version
Analog Input	Analog	4	1.0
Analog Output	Analog	4	1.0
Digital Input/Output	TTL	3	1.0
PWM - AB only	TTL	3	5.8
QAD with Index	TTL	1	3.1

Table 1: IO397_50K front I/O implemented functionality

Note 1:

PWM channel 1 trigger signal is internally used for ADC triggering.

3 Software Installation

Install the custom FPGA bitstream and Simulink Real-Time driver blockset after installing the MathWorks software and the Speedgoat library (speedgoatlib). The steps are as follows:

1. Download the custom implementation for your I/O module and Matlab R2020a from the Speedgoat Customer Portal. The custom implementation is listed in the downloads/software section. If it is not available, please contact Speedgoat support.
2. The archive contains the custom implementation test model (*.slx) and bitstream (*.mat).
3. The content of this archive can be extracted to your current MATLAB workspace. The bitstream (MAT-file) must be part of the MATLAB path. For your convenience, you can copy the bitstream to the following directory, which is part of the MATLAB path. To obtain the predefined bitstream directory, in MATLAB type:
   `» fullfile(speedgoatroot,'sg_bitstream')`
4. After copying the MAT-file, type:
   `» rehash toolbox`

4 I/O Pin mapping

The I/O pin mapping for this custom FPGA bitstream implementation is shown below. This I/O pin mapping is specific to the FPGA I/O module for which it has been designed and shows how to connect the pins to your hardware under test.

Note: Speedgoat delivers real-time target machines together with terminal boards (re-fer to your target machine user manual). The terminal board for the FPGA I/O module must therefore be wired as described in section 7.2 of this document in order to execute the test model for this specific implementation.

Note: Current sense LEG A, B and C are captured in synchronization with the PWM signals. This is handled via an internal FPGA connection that interconnects ADC trigger lines, of current sense Leg A, B and C, with the PWM trigger of Leg A. The PWM trigger is issued at half of the PWM period. PWM and ADC trigger lines, are not accessible from the IO397 pins.

4.1 Front I/O

FPGA pin mapping for the IO397 I/O module

Terminal board B: digital I/O

Pin	Code Module Channel	Functionality	Direction	Transceiver	Port	Pull Resistors
1b		0 V		TTL		pull-up 3.3 VDC
2b		5V		TTL		
3b	1	PWM-A, LEG A	OUT	TTL	PWM Output LEG A, high-side	
4b	-	***Reserved***	-	-	*Reserved*	
5b	1	PWM-B, LEG A	OUT	TTL	PWM Output LEG A, low-side	
6b	1	QAD-A	IN	TTL	Quadrature A input	
7b	2	PWM-A, LEG B	OUT	TTL	PWM Output LEG B, high-side	
8b	1	GPIO, nFLT	IN	TTL	Power Module Fault Input	
9b	2	PWM-B, LEG B	OUT	TTL	PWM Output LEG B, low-side	
10b	1	QAD-B	IN	TTL	Quadrature B input	
11b	3	PWM-A, LEG C	OUT	TTL	PWM Output LEG C, high-side	
12b	-	***Reserved***	-	-	*Reserved*	
13b	3	PWM-B, LEG C	OUT	TTL	PWM Output LEG C, low-side	
14b	1	QAD-C / Index	IN	TTL	Quadrature Index input	
15b	2	GPIO, Enable	OUT	TTL	Enable output	
16b	3	GPIO, nEnable	OUT	TTL	nEnable output	
17b		GND		TTL		

Terminal board A: analog I/O

Pin	Single-ended	Differential	Analog
1a		Current sense LEG A (+)	ADC
2a		Current sense LEG A (-)	
3a		Current sense LEG B (+)	
4a		Current sense LEG B (-)	
5a		Current sense LEG C (+)	
6a		Current sense LEG C (-)	
7a		DC Bus voltage (+)	
8a		DC Bus voltage (-)	
9a	n.a.	(-)	DAC
10a	n.a.	(-)	
11a	n.a.	(-)	
12a	n.a.	(-)	
13a	GND	(-)	
14a	GND	(-)	
15a	0V	(-)	
16a	5 VDC	(-)	
17a	GND	(-)	

Figure 1: IO397_50K front plug-in pin mapping

5 Simulink Driver Library

To open the library blocks for the custom FPGA bitstream, type:
» `speedgoatlib_IO397_50K_CI_02171`

at the MATLAB command line prompt. The blockset appears as follows:

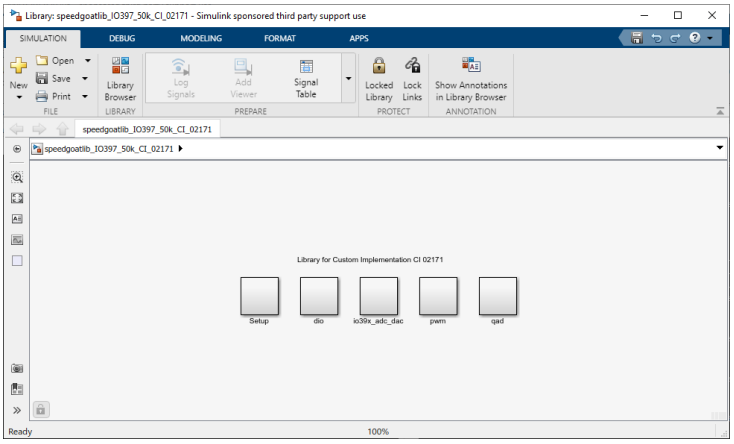

Figure 2: Library for Custom Implementation 02171

The custom FPGA bitstream library contains a subset of the Speedgoat FPGA library blocks implemented in this specific bitstream.

The Speedgoat Library may contain different versions of the driver blocks which are not compatible with your bitstream. We therefore highly recommend that you use this custom library whenever you start to build a new Simulink model.

Alternatively, ensure you select the right version of the respective driver blocks. The version of your implemented Code Module functionality is listed in Section 2, where the major version number signifies the driver block version.

6 Bitstream

The custom Speedgoat FPGA bitstream is configured in the setup driver block.

Figure 3: IO397_50K, select I/O module, front- / rear- I/O plug-in and Custom Implementation bitstream

The FPGA frequency and the resulting tick time (see figure above) is used for time measurements and configuration in several FPGA code modules (like PWM, CAP) and for defining transmission frequencies for protocols (such as SPI, I2C).

7 Test Model

7.1 Test Model Description

A dedicated test model is included to test the custom set of FPGA Code Modules.

Note that this test model only tests I/O channels for which the loop-back test method is possible. The terminal board provided must be wired as indicated in chapter 7.2 of this manual.

To open the test model type:
» `speedgoat_IO397_50K_CI_02171`

at the MATLAB command line prompt. The model appears as follows:

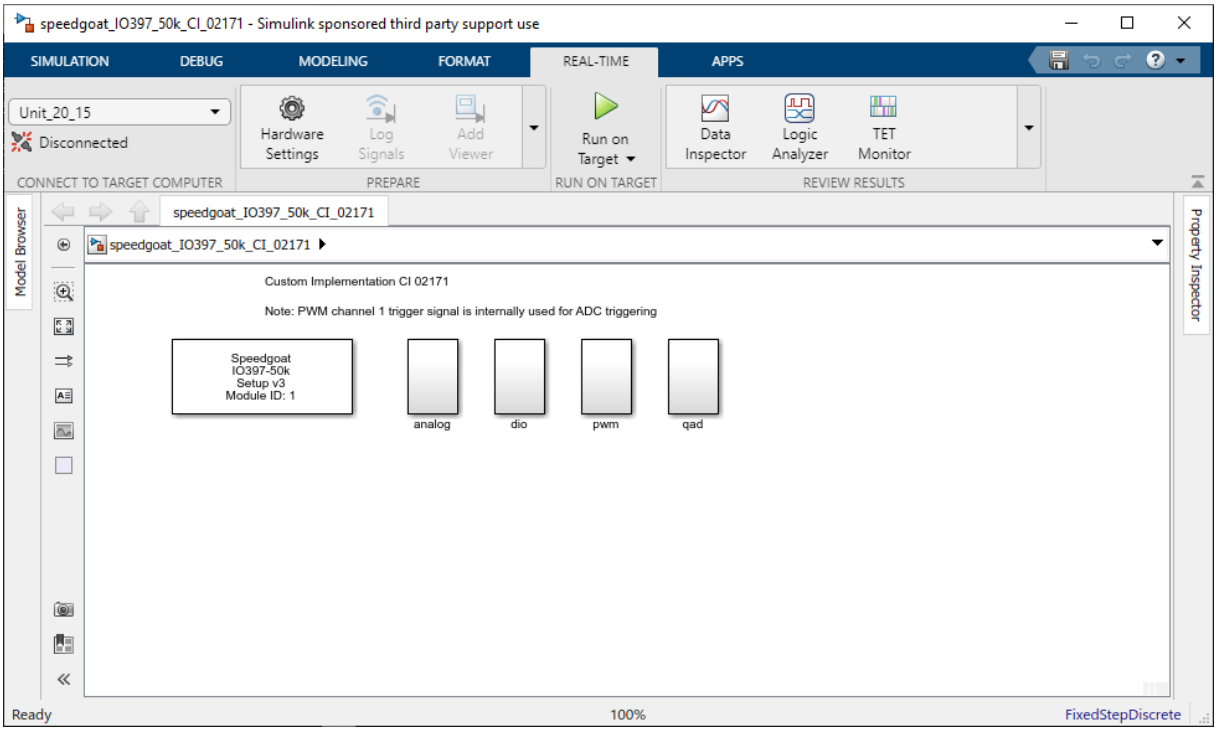

Figure 4: Test model speedgoat_IO397_50K_CI_02171

7.2 Required Test Wiring of the Terminal Board

Front I/O (Analog):

From Pin	To Pin	Tested Functionality
1a	9a	VOUT01 - VIN01 (+) ADC01
3a	10a	VOUT02 - VIN02 (+) ADC01
5a	11a	VOUT03 - VIN03 (+) ADC02
7a	12a	VOUT04 - VIN04 (+) ADC03
13a	2a	Ground - VIN01 (-) ADC01
13a	4a	Ground - VIN02 (-) ADC02
13a	6a	Ground - VIN03 (-) ADC03
13a	8a	Ground - VIN04 (-) ADC04

Table 2: IO397_50K- Front I/O analog terminal board wiring

Front I/O (Digital):

From Pin	To Pin	Tested Functionality
16b	10b	DO channel 3 to QAD - B channel 1
15b	6b	DO channel 2 to QAD - A channel 1
13b	8b	PWM - B channel 3 to DI channel 1

Table 3: IO397_50K- Front I/O digital terminal board wiring

8 Target Screen

If you start the test model (speedgoat_IO397_50K_CI_02171.slx) with the wired board (according to section 7.2), you will obtain the following target screen.

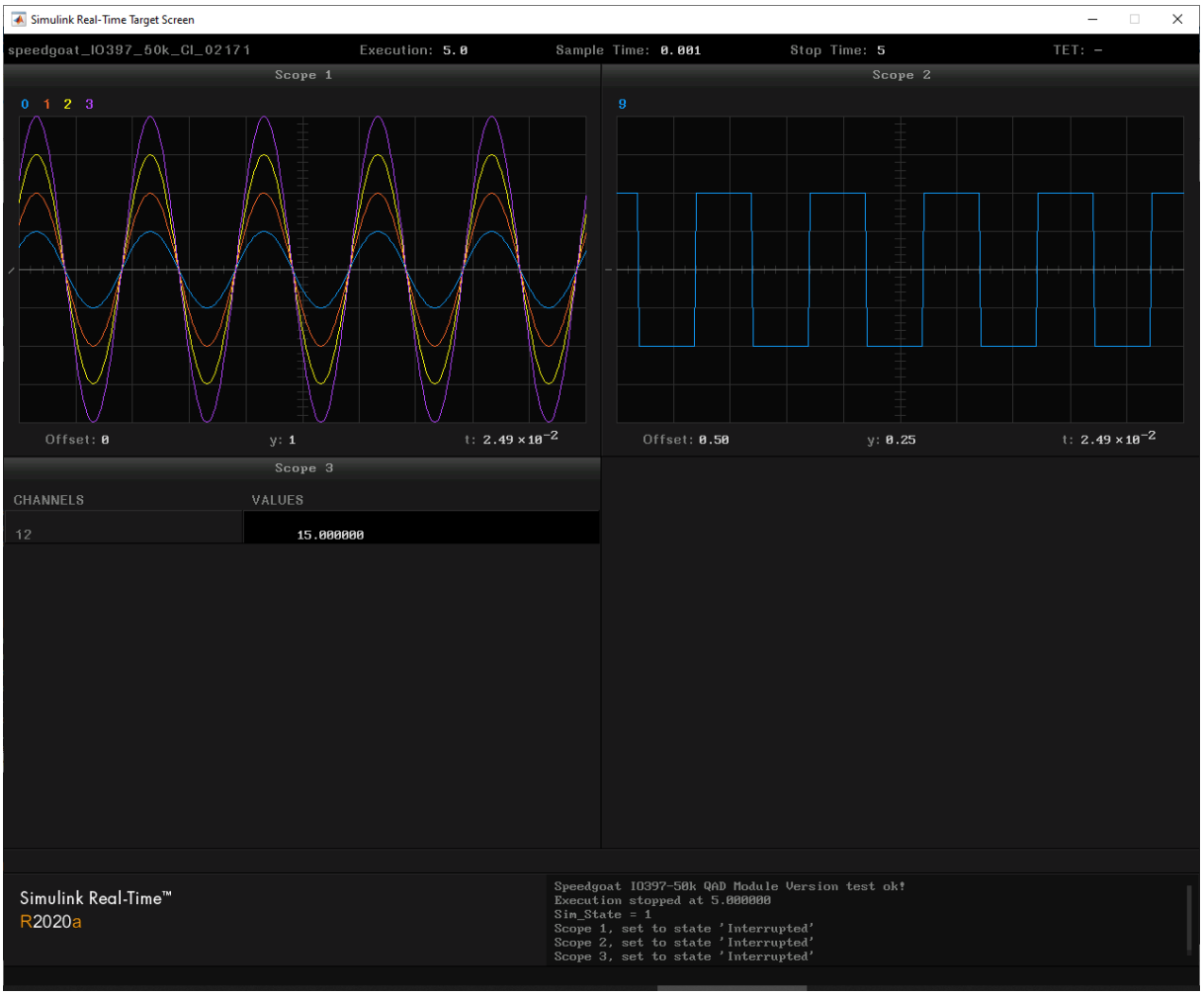

Figure 5: Target Screen with Test Signals