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RCP bitstream for Electric Motor Control Kit (CI-02009)

IO397 pin mapping

Terminal board B: digital I/O

Pin	Code Module Channel	Functionality	Direction	Transceiver	Port	Pull Resistors
1b		0 V		TTL		pull-up 3.3 VDC
2b		5V		TTL		
3b	1	PWM-A, LEG A	OUT	TTL	PWM Output LEG A, high-side	
4b	1	GPIO, FLT CLR	OUT	TTL	Fault clear output	
5b	1	PWM-B, LEG A	OUT	TTL	PWM Output LEG A, low-side	
6b	1	QAD-A	IN	TTL	Quadrature A input	
7b	2	PWM-A, LEG B	OUT	TTL	PWM Output LEG B, high-side	
8b	2	GPIO, nFLT_V	IN	TTL	Overvoltage input	
9b	2	PWM-B, LEG B	OUT	TTL	PWM Output LEG B, low-side	
10b	1	QAD-B	IN	TTL	Quadrature B input	
11b	3	PWM-A, LEG C	OUT	TTL	PWM Output LEG C, high-side	
12b	3	GPIO. nFLT_I	IN	TTL	Overcurrent input	
13b	3	PWM-B, LEG C	OUT	TTL	PWM Output LEG C, low-side	
14b	1	QAD-C / Index	IN	TTL	Quadrature Index input	
15b	4	GPIO, Enable	OUT	TTL	Enable output	
16b	5	GPIO, nEnable	OUT	TTL	nEnable output	
17b		GND		TTL		

Terminal board A: analog I/O

Pin	Single-ended	Differential	Analog
1a		Current sense LEG A (+)	ADC
2a		Current sense LEG A (-)	
3a		Current sense LEG B (+)	
4a		Current sense LEG B (-)	
5a		Current sense LEG C (+)	
6a		Current sense LEG C (-)	
7a		DC Bus voltage (+)	
8a		DC Bus voltage (-)	
9a	n.a.	(-)	DAC
10a	n.a.	(-)	
11a	n.a.	(-)	
12a	n.a.	(-)	
13a	GND	(-)	
14a	GND	(-)	
15a	0V	(-)	
16a	5 VDC	(-)	
17a	GND	(-)	

Note: Field Oriented Control requires that the motor phase currents (analog signals gathered by current sense lines Leg A, B and C) to be captured in synchronization with the PWM signals that control the MOSFET of the two-level three-phase inverter. This is handled via an internal FPGA connection that interconnects ADC trigger lines, of current sense Leg A, B and C, with the PWM trigger of Leg A, which is issued at half of the PWM period. Neither the PWM or the ADC trigger lines, are phiysically accessible from the IO397 IO module pins.