27-November-2017

Custom Implementation FPGA Code Module

I/O pin mapping and driver configuration

I/O Module	IO397_50K
Simulink Real-Time Target Version	R2017b
Minimum Required Speedgoat Library	8.21.0
Reference	speedgoat_IO397_50K_CI_IO397_DUT_DEMO

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Contents

List of Tables

List of Figures

1 Introduction

This manual is an addendum to the User's Manual you have received with your Real-time target machine (with specific serial number).

Your Real-time target machine is equipped with at least one FPGA I/O module for which a default FPGA bitstream and Simulink Real-Time driver blockset has been provided. See the User's Manual for your Real-time target machine for more information on this.

This manual provides information on how to install, configure, and use the specific (custom) FPGA bitstream and Simulink Real-Time driver blockset you have additionally ordered at the time of your Real-time target machine purchase or also possible, at a later time.

2 Implemented Functionality

This custom FPGA bitstream and Simulink Real-Time driver blockset implements the following functionality:

FPGA Code Module	Transceiver Type	No. of modules / channels
Analog input	Analog	4
Analog output	Analog	4
Digital input/output	TTL	8
PWM with trigger	TTL	1
I2C Master	TTL	1
I2C Slave	TTL	1

Table 1: Implemented functionality IO397_50KFront I/O

3 Software Installation

The software installation for this custom FPGA bitstream and Simulink Real-Time driver blockset must be installed after the MathWorks software standard installation and the Speedgoat library (speedgoatlib). Therefore, the steps are as follows:

1. Download the custom implementation for your I/O module and Matlab R2017b from Speedgoat customer login. It is listed in the downloads/software section. If it is not available please contact Speedgoat support.
2. The archive contains both, the test model (*.slx) and the bitstream (*.mat) of the custom implementation.
3. The content of this archive can be extracted in your current MATLAB workspace. The bitstream (MAT-file) must be part of the MATLAB path. For your convenience, you can copy the bitstream in the following directory, which is part of the MATLAB path. To get the predefined bitstream directory, in MATLAB type:
   » `fullfile(speedgoatroot,'sg_bitstream')`
4. After copying the MAT-file, type:
   » `rehash toolbox`

4 I/O Pin mapping

The I/O pin mapping for this custom FPGA bitstream implementation is shown below. This I/O pin mapping is specific to the reconfigurable FPGA module for which it has been designed and is the reference on how you connect the pins to your hardware under test.

Attention: Speedgoat delivers real-time target machines together with terminal boards (see User's Manual of your target machine). Therefore, the wires of the terminal board for the reconfigurable FPGA I/O module have to be wired as described in section 7.2 of this document to execute the test model for this specific implementation.

4.1 Front I/O

Terminal board B: digital I/O

Pin	Code Module Channel	Functionality	Direction	Transceiver	Port	Pull Resistors
1b		0 V		TTL		pull-up 3.3 VDC
2b		5V		TTL		
3b	1	GPIO	IN/OUT	TTL		
4b	2	GPIO	IN/OUT	TTL		
5b	3	GPIO	IN/OUT	TTL		
6b	4	GPIO	IN/OUT	TTL		
7b	5	GPIO	IN/OUT	TTL		
8b	6	GPIO	IN/OUT	TTL		
9b	7	GPIO	IN/OUT	TTL		
10b	8	GPIO	IN/OUT	TTL		
11b	3	PWM - A	OUT	TTL		
12b		PWM - B		TTL		
13b	1	I2C Master CLK	OUT	TTL		
14b		I2C Master Data	IN/OUT	TTL		
15b	1	I2C Slave CLK	IN	TTL		
16b		I2C Slave Data	IN/OUT	TTL		
17b	1	GND		TTL		

Terminal board A: analog I/O

Pin	Single-ended	Differential	Analog
1a	Analog Input 01	Analog Input 01 (+)	ADC
2a	GND	Analog Input 01 (-)	
3a	Analog Input 02	Analog Input 02 (+)	
4a	GND	Analog Input 02 (-)	
5a	Analog Input 03	Analog Input 03 (+)	
6a	GND	Analog Input 03 (-)	
7a	Analog Input 04	Analog Input 04 (+)	
8a	GND	Analog Input 04 (-)	
9a	Analog Output 01	(-)	DAC
10a	Analog Output 02	(-)	
11a	Analog Output 03	(-)	
12a	Analog Output 04	(-)	
13a	GND	(-)	
14a	GND	(-)	
15a	0V	(-)	
16a	5 VDC	(-)	
17a	GND	(-)	

Figure 1: Pinout front plug-in IO397_50K

5 Simulink Driver Library

To open the library blocks for the custom FPGA bitstream, type
» `speedgoatlib_IO397_50K_CI_IO397_DUT_DEMO`

at the MATLAB command line prompt. The blockset looks as follows:

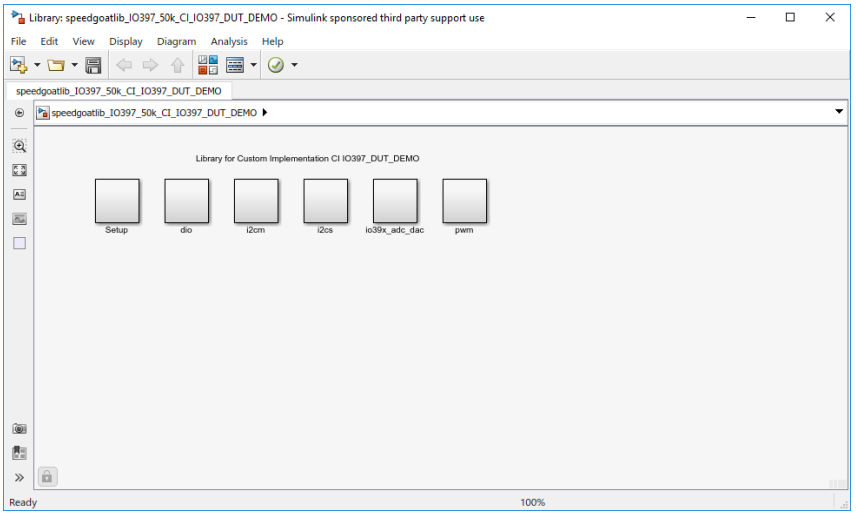

Figure 2: Library for Custom Implementation IO397_DUT_DEMO

The custom FPGA bitstream library contains a subset of the Speedgoat FPGA library blocks. The driver blocks are included in other libraries which come with the standard Speedgoat driver library. When using this FPGA bitstream, only the blocks included in its specific library are supported.

6 Bitstream

Using this custom Speedgoat FPGA bitstream and driver blocks is basically identical to using the default FPGA bitstream, as described in the speedgoatlib_fpga User's Manual. The only difference is the configuration of the Setup driver block:

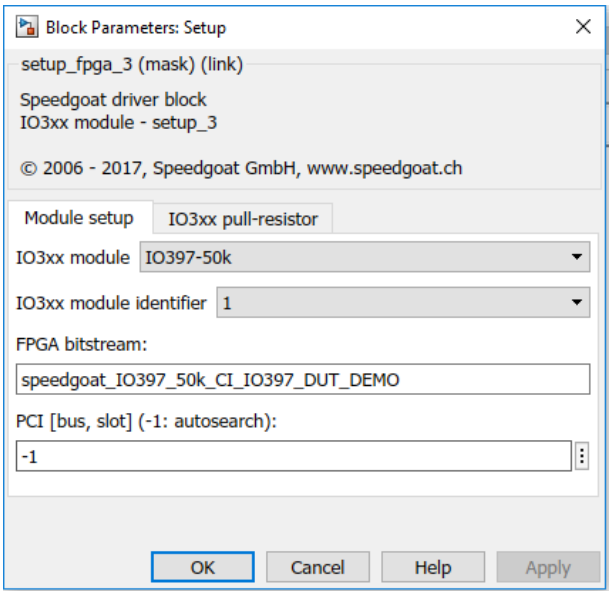

Figure 3: IO397_50K, select I/O module, front- / rear- I/O plug-in and Custom Implementation Bitstream

7 Test Model

7.1 Test Model description

To test the custom set of FPGA Code Modules, a dedicated test model is included. Note that this test model only tests I/O channels for which the loopback test method is possible. It is required to pre-wire the provided terminal board as described in chapter 7.2 of this manual. The test model doesn't exercise I/O channels requiring additional external hardware. Nevertheless executing this test model will confirm the correct set-up of this implementation.

To open the test model type:
» `speedgoat_IO397_50K_CI_IO397_DUT_DEMO`

at the MATLAB command line prompt. The model looks as follows:

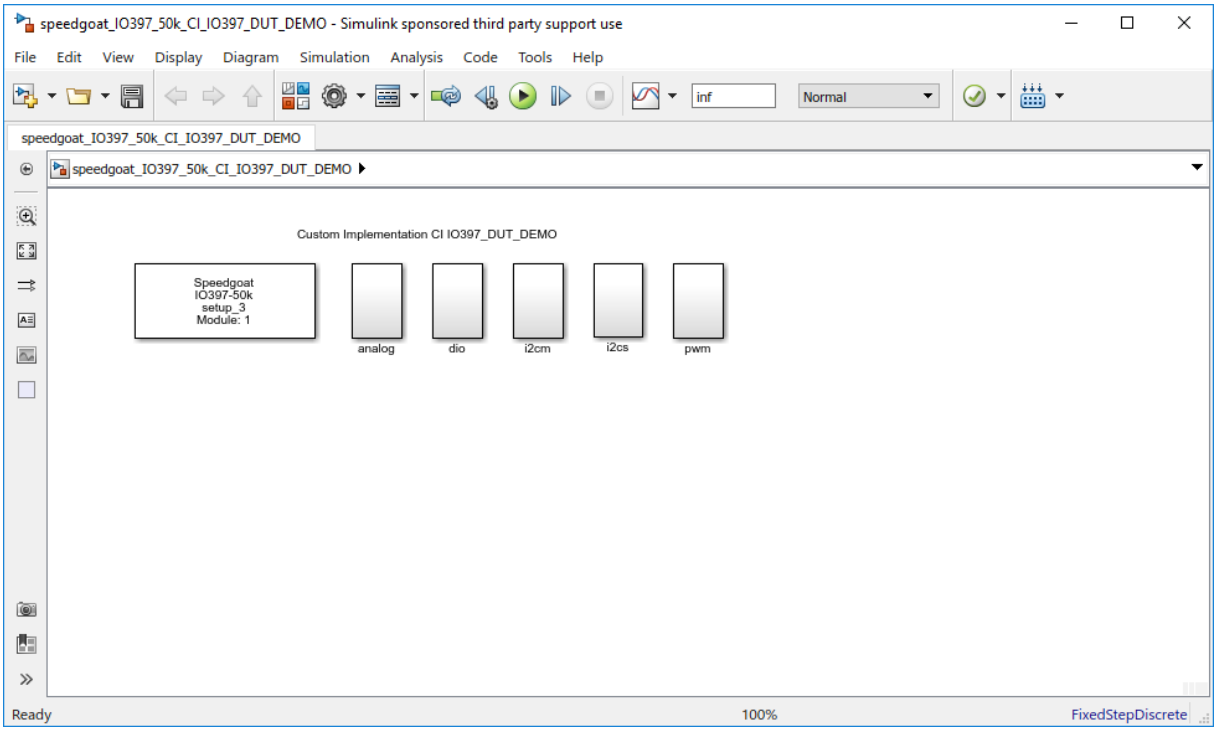

Figure 4: speedgoat_IO397_50K_CI_IO397_DUT_DEMO

7.2 Required test wiring of the terminal board

Front I/O (Analog):

From Pin	To Pin	Tested functionality
9a	1a	VOUT01 - VIN01 (+) ADC01
10a	3a	VOUT02 - VIN02 (+) ADC01
11a	5a	VOUT03 - VIN03 (+) ADC02
12a	7a	VOUT04 - VIN04 (+) ADC03
13a	2a	Ground - VIN01 (-) ADC01
13a	4a	Ground - VIN02 (-) ADC02
13a	6a	Ground - VIN03 (-) ADC03
13a	8a	Ground - VIN04 (-) ADC04

Table 2: Front I/O Terminal Board wiring Analog

Front I/O (Digital):

From Pin	To Pin	Tested functionality
3b	4b	DO channel 1 - DI channel 2
5b	6b	DO channel 3 - DI channel 4
7b	8b	DO channel 5 - DI channel 6
9b	10b	DO channel 7 - DI channel 8
13b	15b	I2C Master CLK - I2C Slave CLK
14b	16b	I2C Master DATA -I2C Slave Data

Table 3: Front I/O Terminal Board wiring

8 Target Screen

If you start the test model (speedgoat_IO397_50K_CI_IO397_DUT_DEMO.slx) with the wired board (according to section 7.2) you see the following target screen.

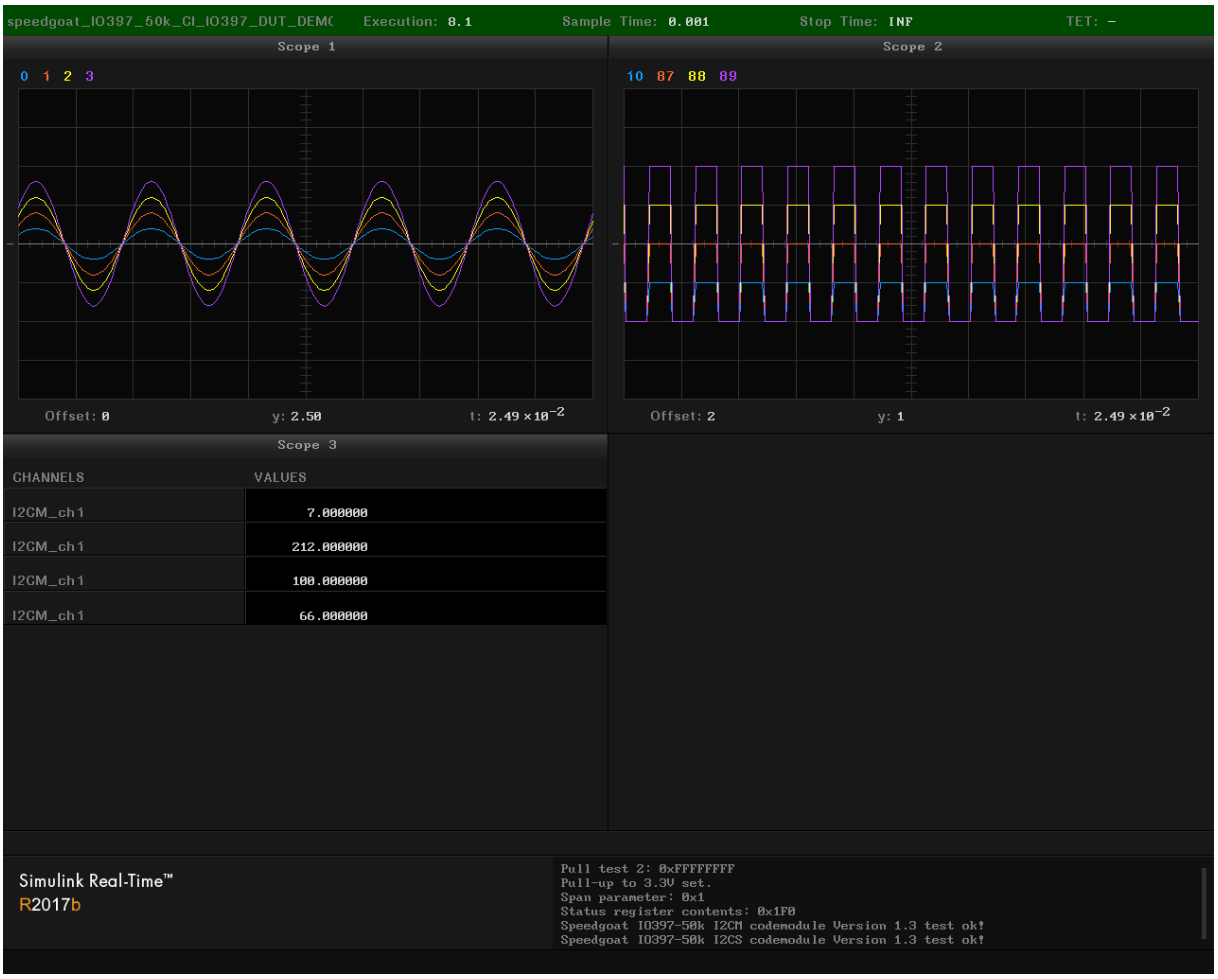

Figure 5: Target Screen with Test Signals