IL2239 Course Project

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Introduction

The goal of this project is to design a SAR-ADC (Successive Approximation Register Analog to Digital Converter) that meets the following specifications:

- Comparator clock: 100 MHz
- SNDR > 28 dB, SFDR > 37 dB
- Technology: 150 nm CMOS
- Supply voltage: 1.8 V
- Input amplitude $V_{\text{in}} = 0.5\,\text{V}_{\text{pp}}$
- A common-mode input voltage in the range $0 \geq V_{\text{in,cm}} \geq 1.8$ V
- Voltage reference value: $V_{\text{ref}} < 1.8$ V
- Switching energy for a full conversion cycle: <30 pJ for $V_{\text{in}} = 300$ mV (DC)
- Resolution: 5 bits

The circuit topology for the SAR-ADC is given in Figure 1.

The project will be carried out in several steps (milestones).

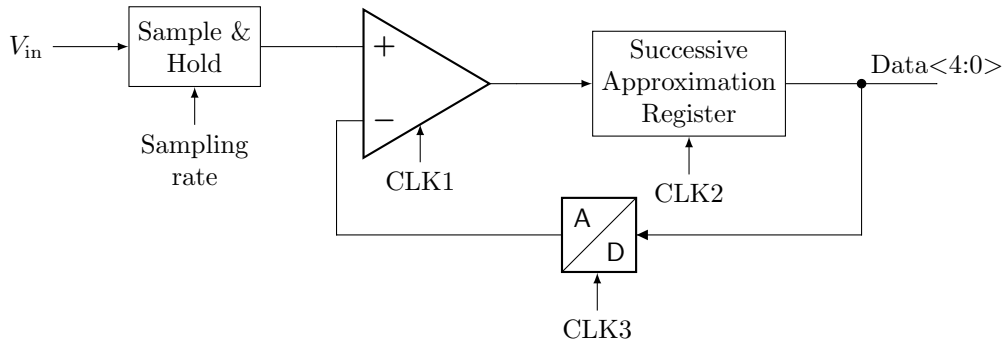


Figure 1: Block diagram of the SAR-ADC

Milestone 1

For this milestone the goals are:

- Design a comparator for the given clock frequency.
- Choose a common-mode input voltage for the comparator, taking into account the properties of the sample & hold circuit.

The comparator used will be of the StrongARM latch topology. To assist us with the design, template projects in Cadence Virtuoso were provided to us.

The schematic for the StrongARM latch comparator is given in Figure 2. In addition to the comparator schematic, two different testbenches (shown in Figures 3-4) were provided.

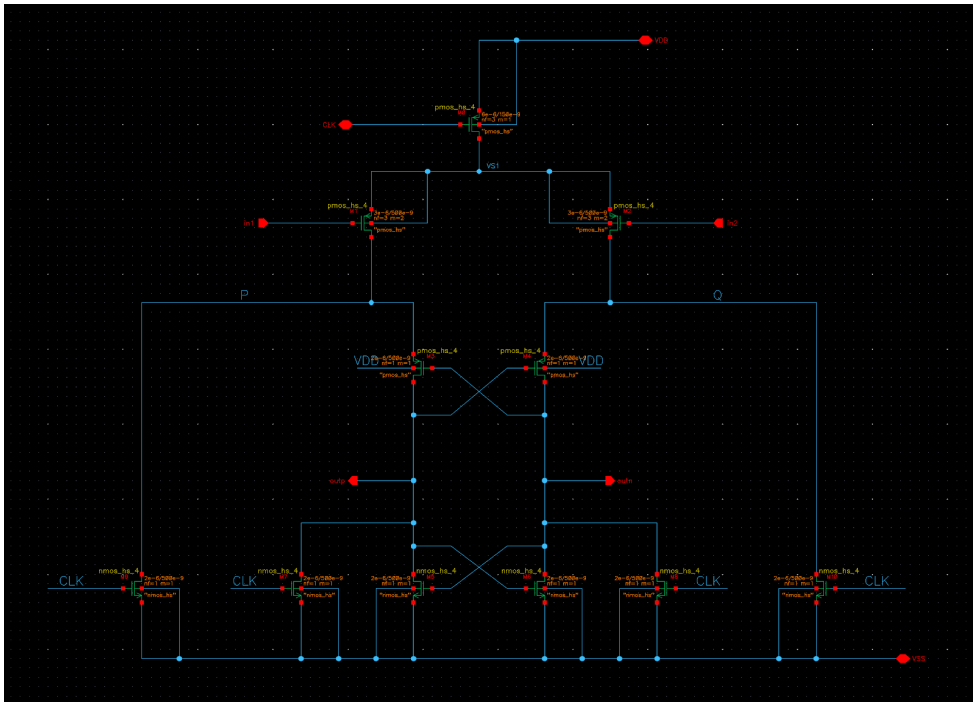


Figure 2: Schematic of the SAR comparator

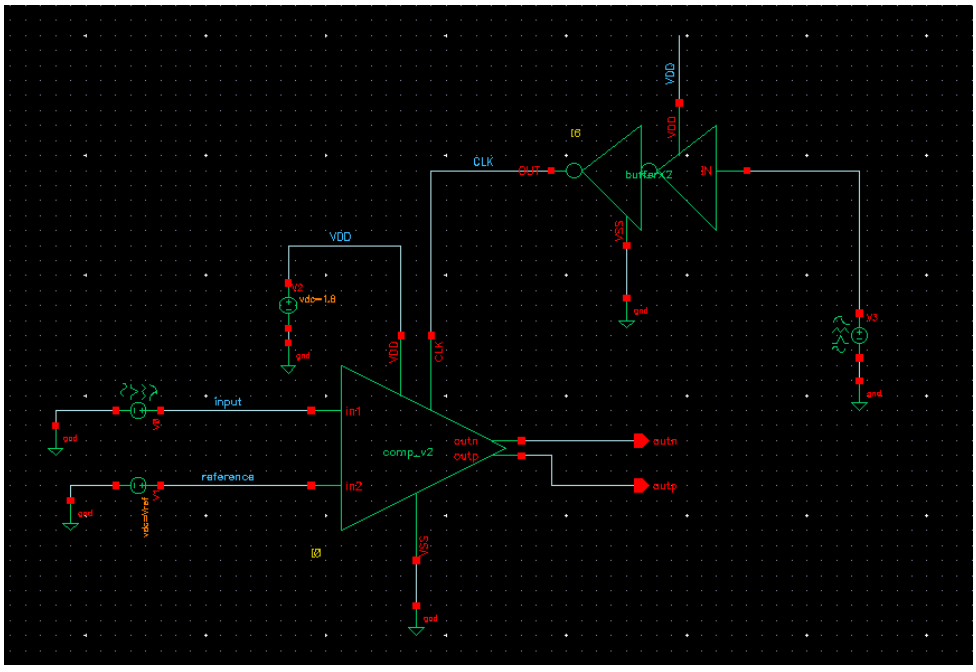


Figure 3: Testbench of the SAR comparator

The purpose of the first testbench in Figure 3 is to verify the basic functionality of the comparator. That is, that $V_{\text{out}}^{-} = V_{\text{DD}}$ and $V_{\text{out}}^{+} = 0$ when $V_{\text{in}}^{-} > V_{\text{in}}^{+}$, and viceversa. The outputs are changed on the negative edge of the input clock and will retain their values during the entire negative half of the clock

cycle. On the positive edge of the clock cycle, both outputs will be changed 0 and these values will be retained during the entire positive half of the clock cycle.

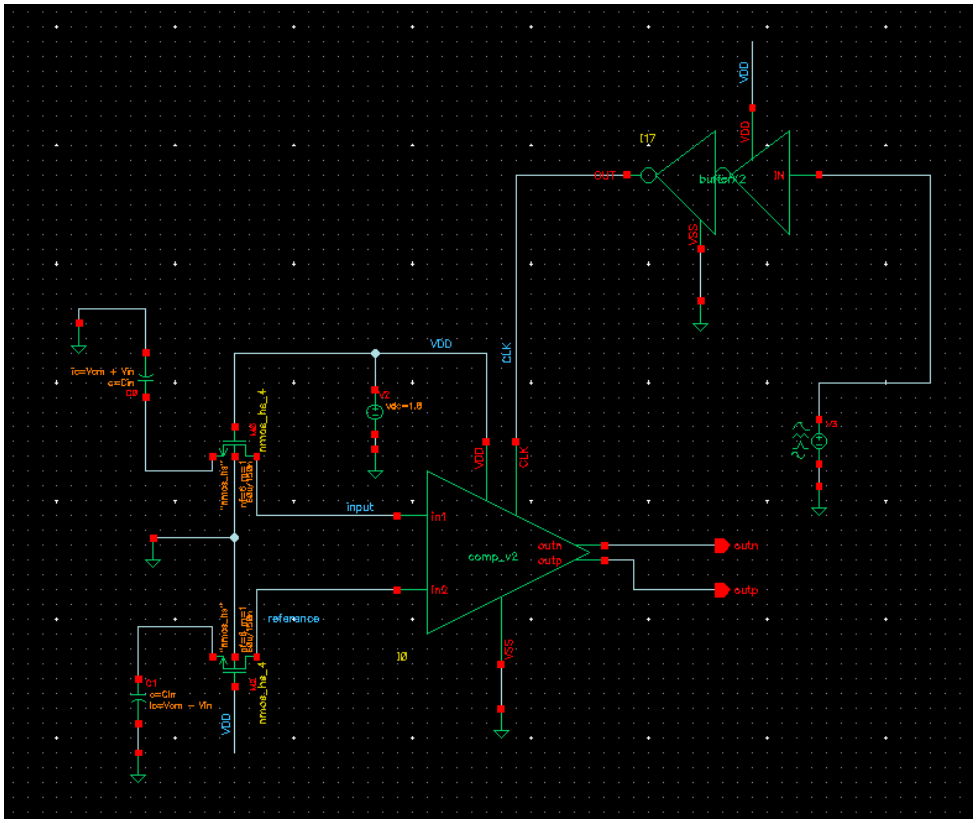


Figure 4: Testbench of the SAR comparator

The second testbench in Figure 4 is mainly useful for determining the amount of kickback noise. Kickback noise is a seen as a voltage drop or spike on the inputs as a result of capacitive coupling between the gate-drain and gate-source of transistors M1 and M2 in Fig. 1. This is an undesirable effect and can cause incorrect comparison results. For a comparator used in a SAR-ADC, the kickback noise must be less than $0.5/2^n$V, where n is the desired amounts of bits of resolution that the ADC must be able to handle, in our case 5.

In order to determine the common mode input voltage, we have to look at the sample-and-hold circuit which connects to in1 of the comparator.

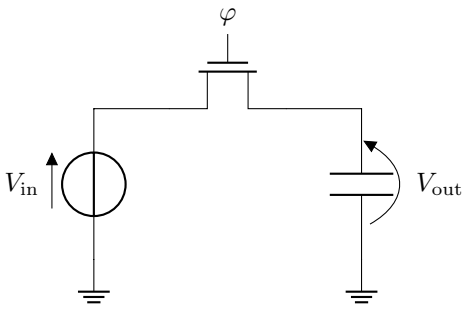


Figure 5: Simple sample & hold circuit

In Figure 5 a simple sample-and-hold circuit is shown. In our case V_{in} will be equal to $V_{\text{cm}} + V_{\text{sample}}$, that is, a common-mode voltage plus the voltage we are interested in sampling. in1 of the comparator is connected to the capacitor. The transistor used as a switch can be considered to be an n-channel MOSFET.

The gate of the transistor will be driven by VDD=1.8, and in order for it conduct, the Vgs voltage must be equal to or greater than the threshold voltage. We can make the assumption that Vth=0.7 V. Further, we can make the assumption that the voltage drop between the drain and source is negligible.

It's easy to see that the voltage across the capacitor can't be higher than 1.1 V, or else the transistor won't conduct. Since Vsample will have a swing of $0.5\,V_{pp}$, the maximum voltage present at the drain of the transistor will be $V_{cm} + 0.25$ V.

Thus, to determine a suitable value for the common mode voltage, we use the following relation:

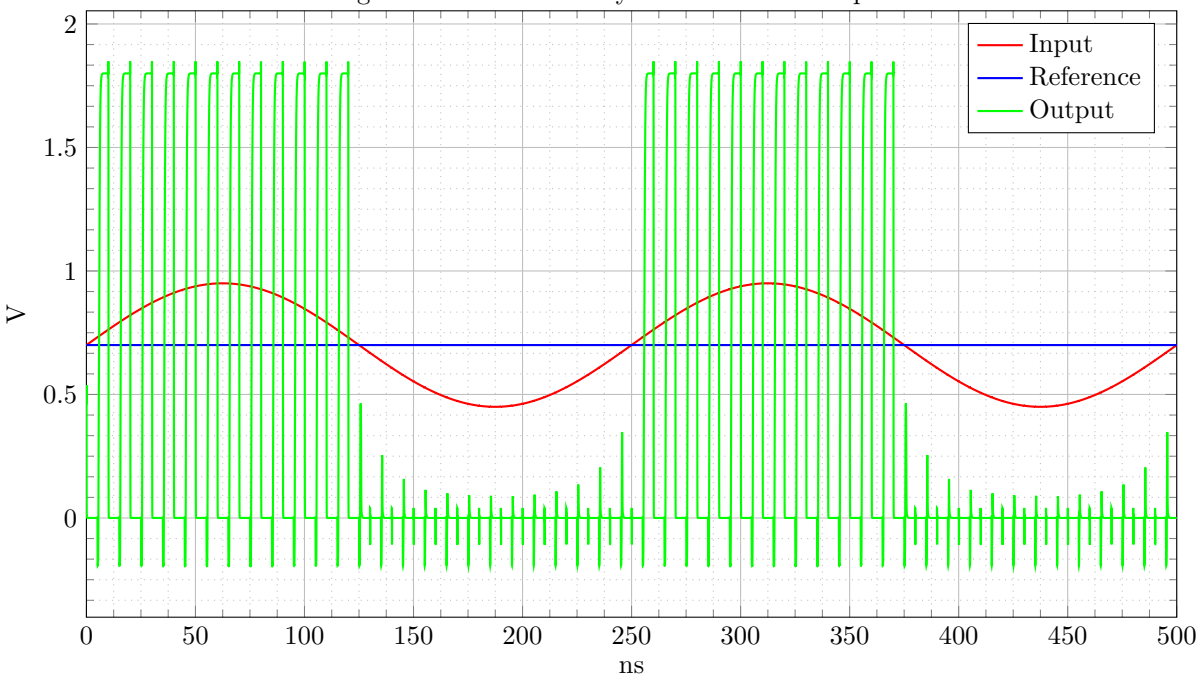
$$V_{cm} + 0.25 = 1.1 \tag{1}$$

Which gives a maximum common mode voltage of Vcm=0.85 V. In order to have a little more margin, we choose $V_{cm} = 0.7$ V.

1.1 Transient analysis

To verify the functionality of our circuit we perform a transient simulation where we expect to see the ouput of the comparator changing to high according to the relation $V_{in}^{+} \lessgtr V_{in}^{-}$.

Figure 6: Transient analysis of the SAR comparator



In Figure 6 we can see the results of the transient simulation for two periods of a 4 MHz input sine wave. It is easy to check that the functionality of the comparatoris as expected.

1.2 Kickback simulation

Untill this point, the effects of the capacitive coupling between the input and intermediate nodes of the comaprator has been ignored. In reality this effect can lead into significant errors due to the effect of the kickback.

Figure 7 shows the effect of the so called kickback. As we can see the inputs, which are not supposed to change, present a significant variation due to the capacitive coupling through the parasitic capacitances of the transistors. To quantize this effec we use the following expression.

```
(ymax((vtime('tran "/input") - vtime('tran "/reference"))) - (2 * VAR("Vin")))
```

This effect can be visualized in Figure 8. With the current sizes and biasing we obtain a kickback of only 7.1 mV.

Figure 7: Close-up on the kickback noise effects

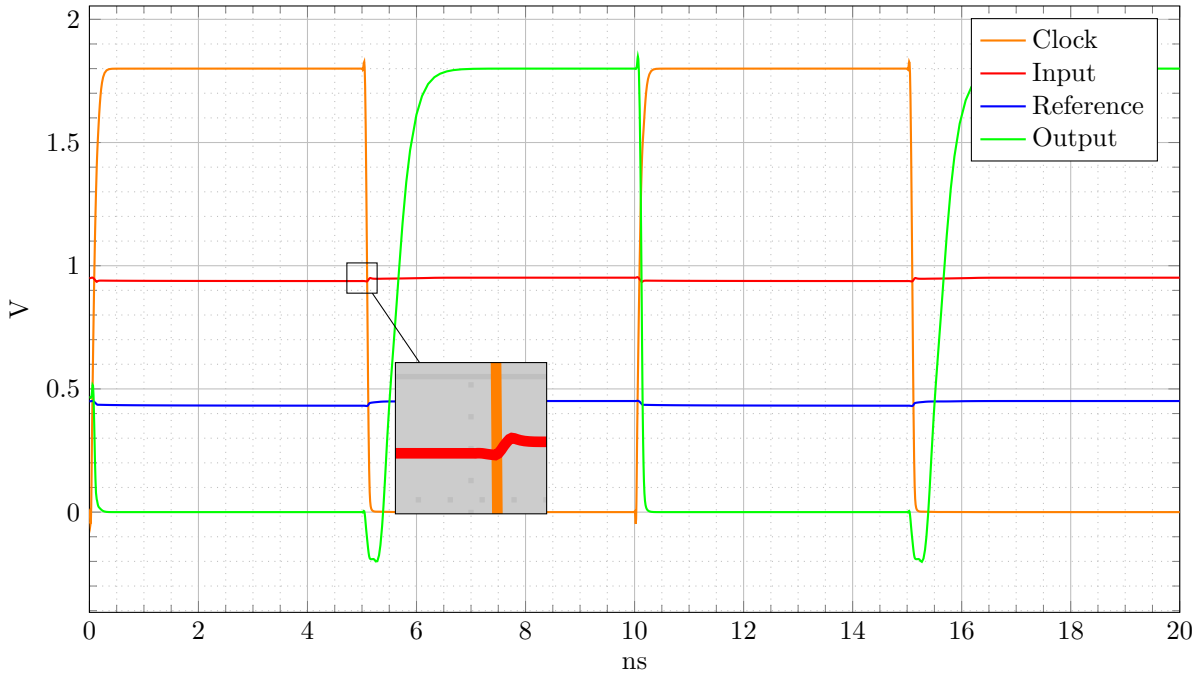
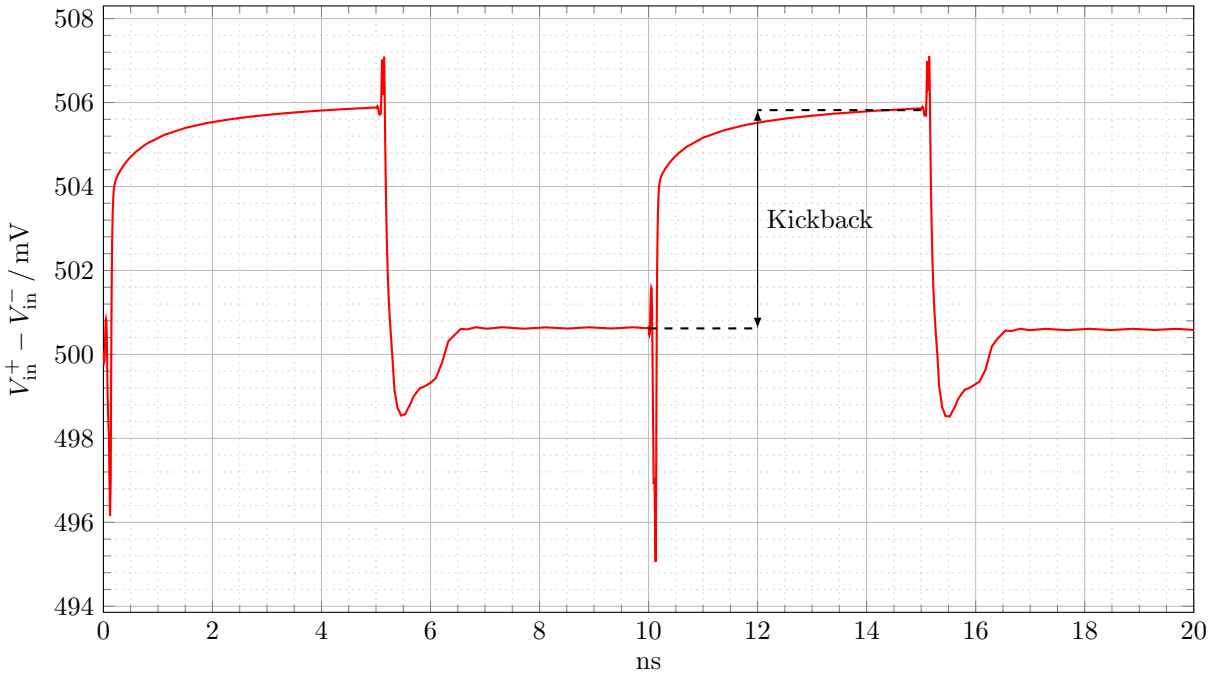


Figure 8: Differential error generated by the kickback



1.3 Noise simulation

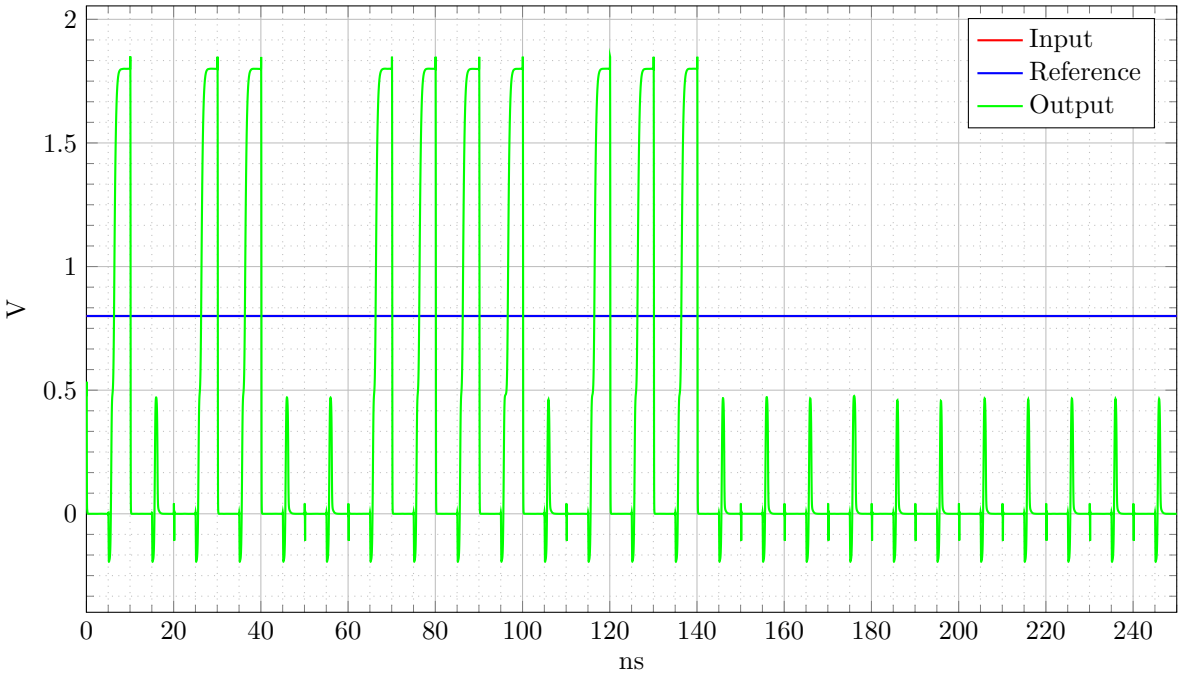
Untill this point, all the simulations were performed with noise-free components. The noise generated by the transistors and passive devices in the comparator can lead to significant error.

To simulate this effects we enable the transient noise and we perform a transient analysis.

When using a input signal of 0.5% of the V_{LSB} the results were identical to Figure 6, this means that the circuit works as expected.

In the other hand, when using a signal of 0.1% of the V_{LSB} the comparator was not working as expected, as can be seen in Figure 9. Note that the input signal cannot be seen in the plot since its amplitude was under 1 mV. This is a extermely low value so we dont have to worry about noise effects

Figure 9: Transient analysis with noise



with this configuration.

1.4 Power Consumption

To obtain the power consumption of our circuit, we can measure the current that is being drawn from the V_{DD} power supply. Using this method we obtain a power consumption of 76.82 µW.

1.5 HDL Description

The Verilog-AMS description of the comparator can be seen in the Sample Code 1. To account for the propagation delay we used the functions `riseTime` and `fallTime` that are provided by Cadence ADE. We measured a rise time of 574.4 ps and a fall time of 71.03 ps. To simulate this propagation delay we added the delays expressions to the Verilog-AMS code (lines 21 and 29).

1.6 Layout

The layout was based on the layout that was provided. We just changed the sizes of the input transistors and adjusted the connections. Te final layout can be seen in Figure 10.

```
`timescale 10ps/1ps
`include "constants.vams"
`include "disciplines.vams"

module comp_v2 ( outn, outp, CLK, VDD, VSS, in1, in2 );
    output outn;
    inout  VDD;
    inout  CLK;
    input  in2;
    input  in1;
    inout  VSS;
    output outp;

    logic CLK;
    logic outn, outp;
    electrical VDD, VSS, in1, in2;
    reg outp, outn;

    always @(posedge CLK)
    begin
        #5
        outn = 0;
        outp = 0;
    end
    always @(negedge CLK)
    begin
        if (V(in1) > V(in2))
        begin
            #57
            outn = 1;
            outp = 0;
        end
        else
        begin
            #57
            outn = 0;
            outp = 1;
        end
    end
endmodule
```

Sample Code 1: Verilog-AMS description of the comparator

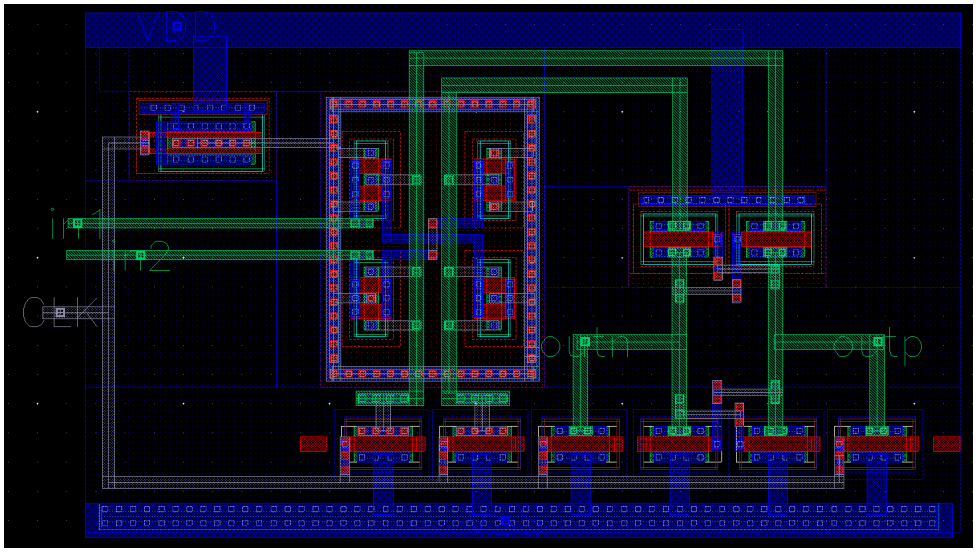


Figure 10: Final layout of the ADC