Brussels, November 5, 2020

Analog Electronics Exercises

Session 1

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The CMOS table

The follwoing table taken from the class lectures, chapter 1, summarizes the behaviour of small signal and large signal parameters given the inversion levels of a transistor. In the following exercises we will try to build intuition out of the different regions and the impact in the design of amplifiers.

inversion level	IDS – VGS dependence in saturation	gm – VGS dependence in saturation	VDSAT	Required W for given gm or IDS	gm/IDS	Main capacitors in saturation	fT	linearity
weak	exponential	exponential	Minimal (few times Ut)	Very high	Maximal (1/nUt)	1. Extrinsic Cgs and Cgd 2. Junction caps Csb and Cdb 3. Intrinsic Cgb	low	low
moderate	TRANSITION BETWEEN WEAK AND STRONG INVERSION							
strong	quadratic (linear with velocity saturation)	linear (constant with velocity saturation)	Larger than in weak inv.: Vov/a (long channel), less for short channel	low	Less than in weak inv.: 2/Vov 1/Vov with velocity saturation	1. Total Cgs 2. Junction caps Csb and Cdb 3. Extrinsic Cgd	high	higher

Figure 1: General table with MOS characteristics versus inversion level

Exercise 1

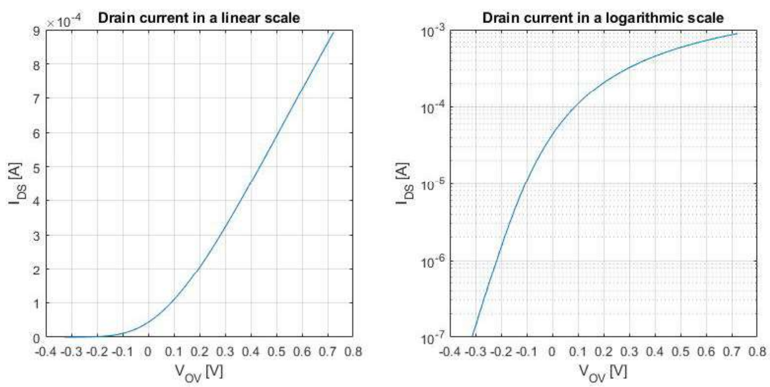

Figure 2: $I_{DS} \times V_{OV}$ curves (similar to Fig.1.22 from the class notes) showing the drain current per micrometer width ($W = 1\mu m$) as a function of V_{OV} on a linear scale (left) and logarithmic scale (right). The plots are generated for a $65nm$ nMOS transistor in saturation with $V_{DS} = 1V$, $V_{SB} = 0V$ and a gate length of $65nm$.

Given the I_{DS} curve in Fig.2 and the table in Fig.1, define the approximate range of V_{OV} for the three inversion regions: weak, moderate and strong.

a) Weak inversion:

b) Moderate inversion:

c) Strong inversion:

Exercise 2

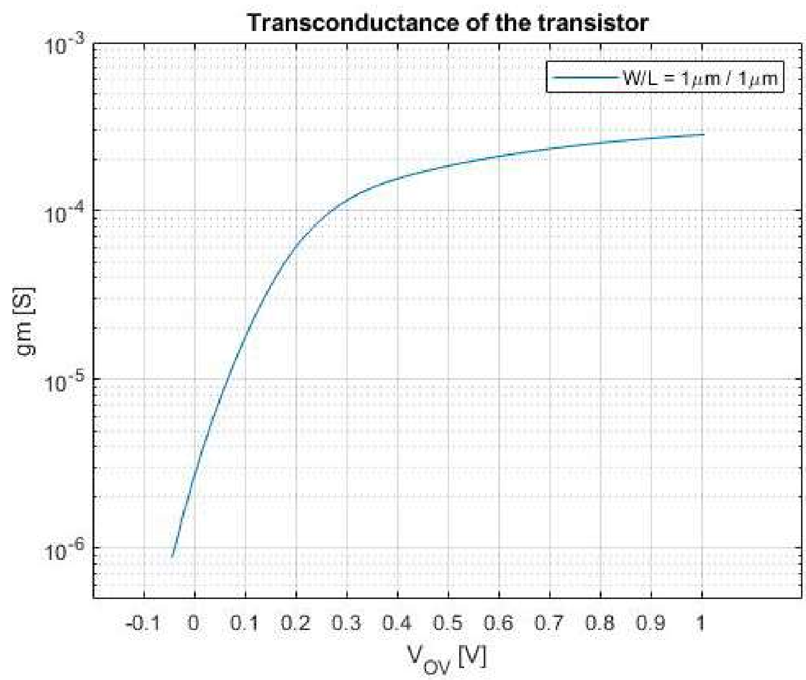

Figure 3: $gm \times V_{OV}$ curve (similar to Fig.1.25 from the class notes) showing the transconductance per unit width of a long-channel nMOS transistor from a $65nm$ process as a function of V_{OV} . The transistor operates in saturation with $V_{DS} = 1.1V$, $V_{SB} = 0V$, $W = 1\mu m$, and $L = 1\mu m$.

Assuming we have a discrete component in the lab, which is a nMOS transistor in a $65nm$ technology with a W/L ratio of $1\mu m/1\mu m$ (Figure 3) and assuming the V_{th} of this nMOS is $0.3V$. How do we need to size V_{GS} to implement a transconductance of $0.1mS$? How to increase the gm to $1mS$?
Hint: there are multiple answers. Cite as many as you can.

Exercise 3

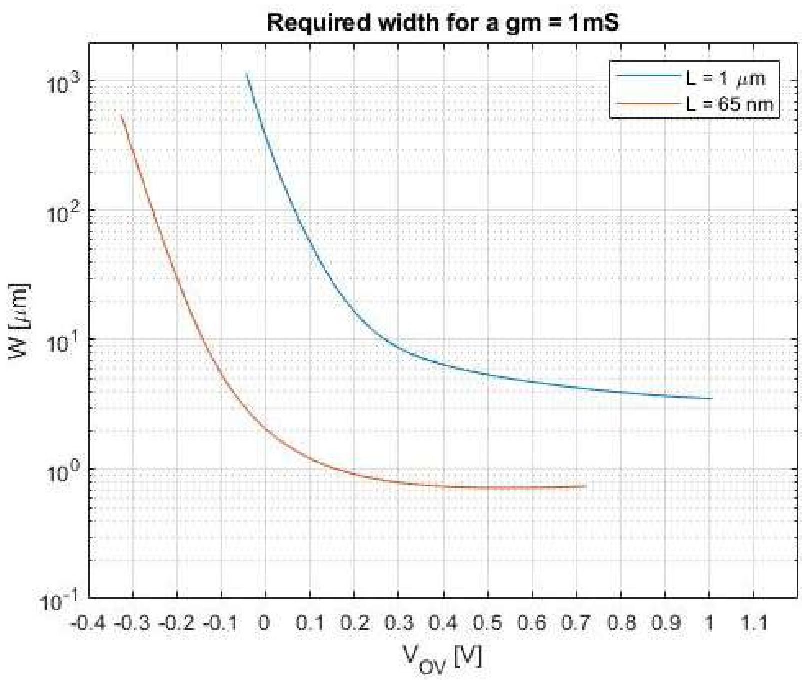

Figure 4: $W \times V_{OV}$ curve (similar to Fig.1.45 from the class notes) showing the required width as a function of the overdrive voltage for an nMOS transistor from a $65nm$ process with $V_{DS} = 1.1V$, $V_{SB} = 0V$, $L = 1\mu m$, and $L = 65nm$, to realize a transconductance of $1mS$.

Assuming now we can control on the W of the transistor and the L is fixed at $1\mu m$ such that we can derive the Figure 4. How can one approach to find the W to implement a $gm = 10mS$ in the three inversion levels?
Hint: assume that $gm = W \times f(ConstantParameters)$.

Exercise 4

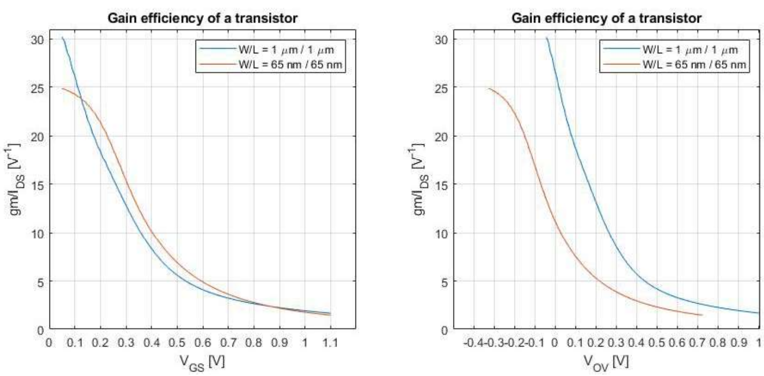

Figure 5: $gm/I_{DS} \times V_{OV}$ curve (similar to Fig.1.26 from the class notes) showing the ratio gm/I_{DS} for a transistor from a $65nm$ process with $V_{DS} = 1.1V$, $V_{SB} = 0V$, and two different channel lengths: $L = 1\mu m$ and $L = 65nm$.

a) What is the required I_{DS} current necessary to bias a $W/L = 1\mu m/1\mu m$ transistor with $gm = 10mS$ at different inversion levels?

b) Assuming that this current is generated by a resistive load R_L, what is the voltage gain realized by the transistor?

Exercise 5

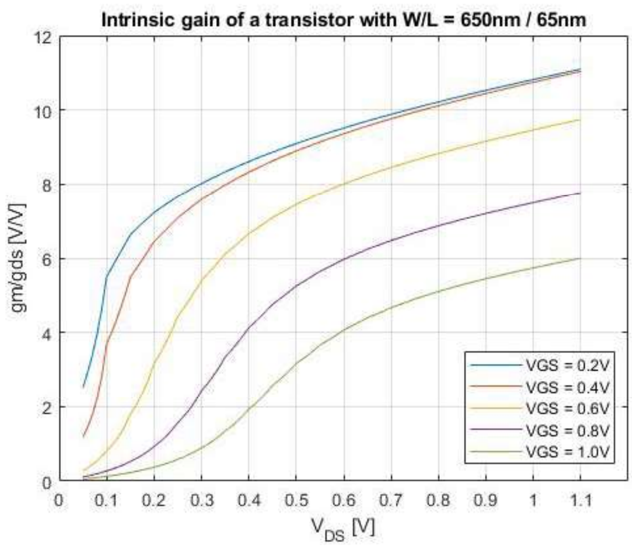

Figure 6: $gm/gds \times V_{DS}$ curve (similar to Fig.1.32 from the class notes) showing the intrinsic gain as a function of V_{DS} for different V_{GS} values for a minimum-length transistor of a $65nm$ process with $V_{SB} = 0V$. Note that V_{th} is around $300mV$.

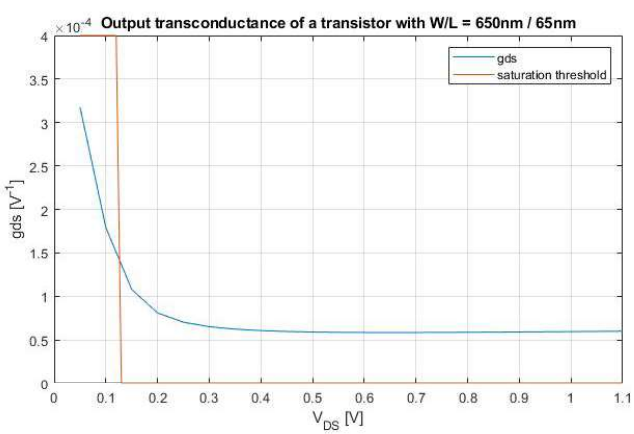

Figure 7: $gds \times V_{DS}$ curve (similar to Fig.1.30 from the class notes) showing the output conductance as a function of V_{DS} for a transistor in a $65nm$ process with $W = 650nm$, $L = 65nm$, $V_{GS} = 525mV$ (about $200mV$ above V_{th}), and $V_{SB} = 0V$.

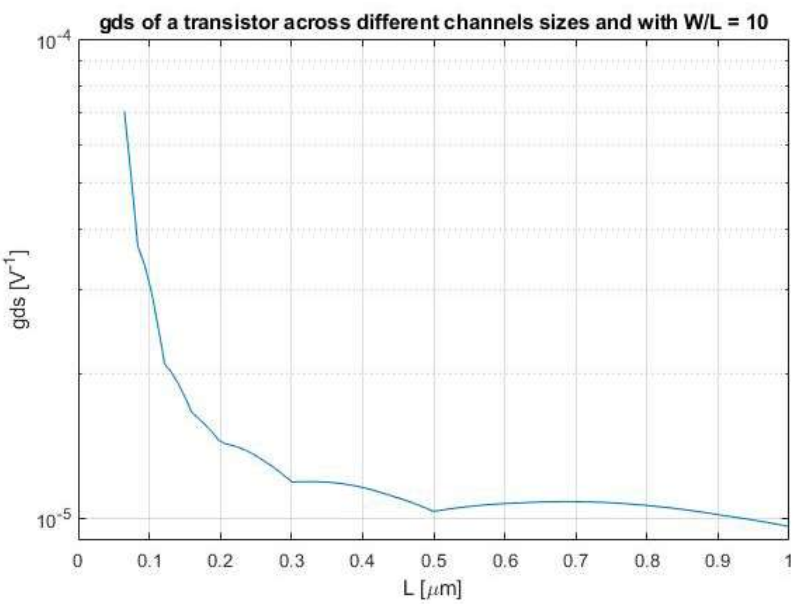

Figure 8: $gds \times L$ curve (similar to Fig.1.30 from the class notes) showing the output conductance as a function of channel length for a transistor in a $65nm$ process with $V_{OV} = 200mV$, $V_{DS} = 1.1V$, $V_{SB} = 0V$ and W is adapted such that W/L is constant and equal to 10.

Assuming now that this transistor is driven by a PMOS load as a current source and that the profiles of curves in Figure 7 and 8 are true for both PMOS and NMOS with the proper consideration of V_{DS} polarity: how does one chose the biasing conditions to maximize the gain of the common source amplifier?