Opamp Simulation Project

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Aim

To simulate a Operational Amplifier in LTSpice using the TSMC 0.18μm model with the following specifications :

- DC Gain = 2
- -3db frequency of Closed Loop = 5MHz
- PM between 60^o - 80^o
- Input Pair = PMOS
- C_L = 5 pf
- R_L = 5 kΩ
- Use reference current as $\frac{1}{10}th$ of total current in first stage of opamp.

Specifications

TSMC 0.18μm Specification :

V_{dd}	1.8V
$\mu_n C_{ox}$	230 $\mu A/V^2$
$\mu_p C_{ox}$	100 $\mu A/V^2$
V_{t_n}	0.37V
V_{t_p}	0.39V
L_{min}	0.27 μm
W_{min}	0.18 μm
ad, as	$2L_{min} * W sq.units$
pd, ps	$2(2L_{min} + W) units$
λ	0.09 S/A

Hand Calculation

Through Miller Compensation,

$$\boxed{Closed\ Loop\ Zero \approx \frac{g_{m_5}}{C_c}}$$

$$\boxed{Open\ Loop\ Unity\ Gain\ Frequency \approx \frac{g_{m_1}}{C_c}}$$

Also, $\boxed{\beta = 0.5}$, so to get the parameters, let us first assume that $\boxed{C_c = 2pf.}$ Thus,

$$\frac{g_{m_1}}{C_c} = \frac{50 * 10^6 * 2 * \pi}{\beta} \implies \boxed{g_{m_1} \approx 0.12mS}$$

Also, for assuming the single pole approximation, we must push the zero much further than the unity gain frequency.

$$\frac{g_{m_5}}{C_c} = \frac{10 g_{m_1}}{C_c} \implies \boxed{g_{m_5} \approx 1.2mS}$$

Also, $DC\ Gain = \dfrac{g_{m_1} g_{m_5} R_L}{g_{ds_2} + g_{ds_4}}$,

$$\implies g_{ds_2} + g_{ds_4} = \frac{g_{m_1} g_{m_5} R_L}{DC\ Gain} \approx 2 * 10^{-6}\ S$$

We can assume each channel length modulation to be equal,

$$\implies \boxed{g_{ds_2} = g_{ds_4} \approx 1 * 10^{-6}\ S}$$

Now, to find bias current, we use the formula for channel length modulation,

$$g_{ds_2} = \lambda I_d \implies \boxed{I_d \approx 11\mu A}$$

Thus, to supply this current to both the arms, we should supply a total of $I = 22\mu A$. Thus the reference current will be $\boxed{I_b \approx 2.2\mu A}$

Using these values, we can start the initial building of the opamp. Let us assume a gemeral overdrive voltage of 0.2V

For opamp :

$$g_m = \mu_p C_{ox} \left(\frac{W}{L}\right)_p V_{ov} \implies \left(\frac{W}{L}\right)_p \approx 6$$

$$g_m = \mu_n C_{ox} \left(\frac{W}{L}\right)_n V_{ov} \implies \left(\frac{W}{L}\right)_n \approx 1.7$$

For current mirrors to first stage, it should be 1:10 correspondence i.e.

$$10 \left(\frac{W}{L}\right)_{ref} = \left(\frac{W}{L}\right)_{first\ stage}$$

For the second stage,

$$g_m = \mu_n C_{ox} \left(\frac{W}{L}\right)_n V_{ov} \implies \left(\frac{W}{L}\right)_n \approx 17.9$$

Also the current mirror should mainly supply current to keep DC voltage at output, which will be twice the common mode voltage.

$$V_{in_{cm}} = 0.5V \implies V_{out_{cm}} = 1V \implies I = V/R_L = 1/5000 = 200\mu A$$

Also, the M5 diode also draws a current of

$$I_d = \frac{g_m(V_{GS} - V_T)}{2} = 180\mu A$$

Thus the current mirror of second stage must supply 180+200 = 380 A

$$I_d = 0.5\mu_p C_{ox} \left(\frac{W}{L}\right)_p V_{ov} \implies \left(\frac{W}{L}\right)_p = 190$$

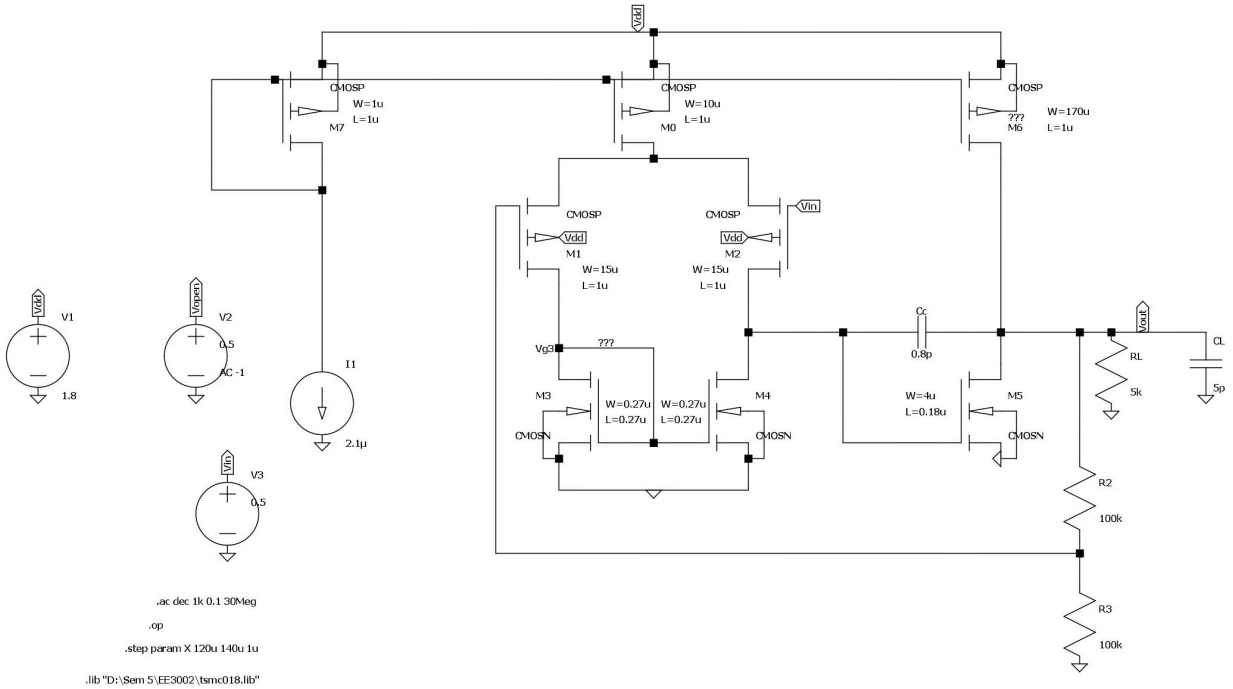
Thus, to tabulate the MOSFET hand calculation results :

MOSFET Name	$\left(\frac{W}{L}\right)$	g_m	g_{ds}	$V_{GS} - Vt$	I_d
M0	10	$0.22mS$	$1.98\mu S$	$0.2V$	$22\mu A$
M1*	6	$0.12mS$	$1\mu S$	$0.2V$	$11\mu A$
M2*	6	$0.12mS$	$1\mu S$	$0.2V$	$11\mu A$
M3*	1.7	$0.12mS$	$1\mu S$	$0.2V$	$11\mu A$
M4*	1.7	$0.12mS$	$1\mu S$	$0.2V$	$11\mu A$
M5	17.9	$1.2mS$	$16.2\mu S$	$0.2V$	$180\mu A$
M6	190	$2mS$	$18\mu S$	$0.2V$	$380\mu A$
M7	1	$0.022mS$	$0.198\mu S$	$0.2V$	$2.2\mu A$

* - Although the values don't seem to match (since I focused more on g_{ds} than g_m), I left the simulator to take care of it, as I assumed the values for these to be rough and not very precise.

Other components are $\boxed{C_c = 2pF}$, $\boxed{R_L = 5k\Omega}$, $\boxed{C_L = 5pF}$
DC calculated gain = 2
Power consumed (approx.) $= V_{dd} * \sum I_{mirrors} = 1.8 * (380 + 22 + 2.2) * 10^{-6} = 0.73mJ$

Simulated Design Diagram



Note - In some places, L_{min} could not be used due to high channel length modulation when L_{min} was used.

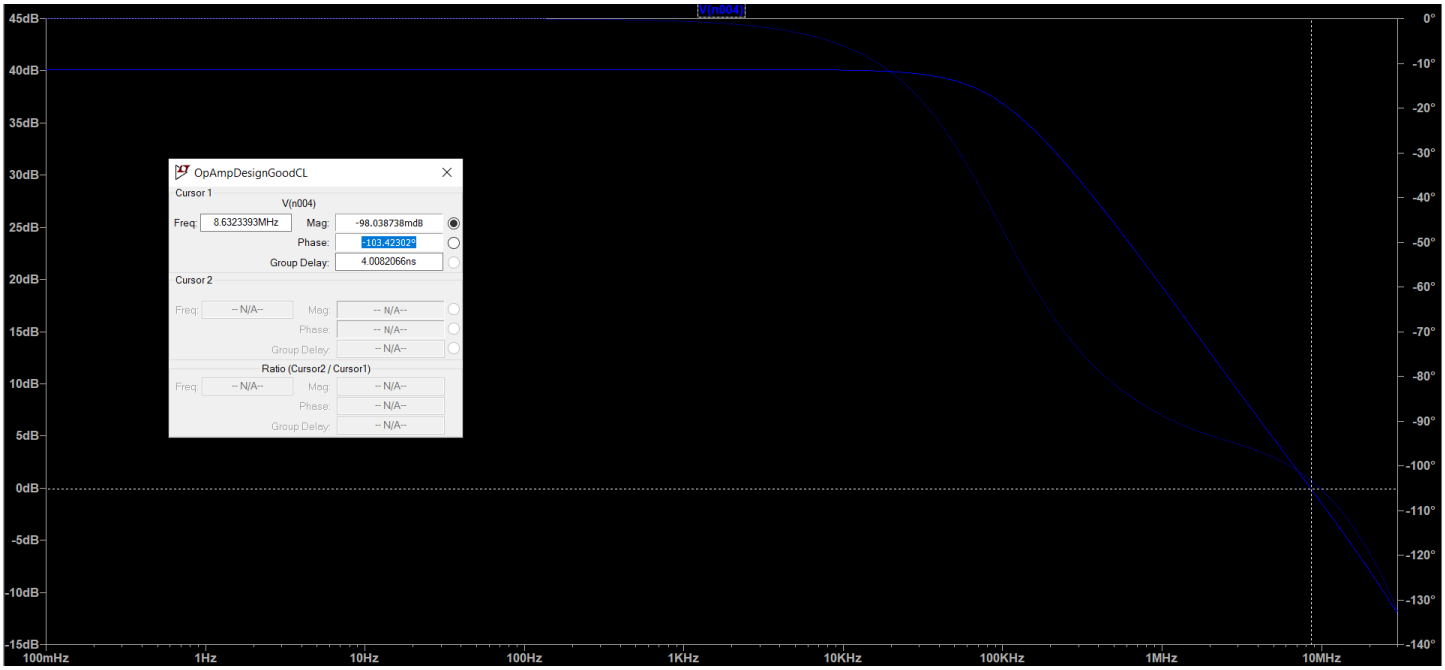
Simulated Values Table

Note - Some values may differ vastly due to changes incorporated to get the required phase margin

Name	W	L	$\left(\frac{W}{L}\right)$	g_m	g_{ds}	$V_{GS} - Vt$	I_d
M0	$10\mu m$	$1\mu m$	10	$0.146mS$	$1.55\mu S$	$0.27V$	$20.6\mu A$
M1	$15\mu m$	$1\mu m$	15	$0.122mS$	$1.06\mu S$	$0.146V$	$10.3\mu A$
M2	$15\mu m$	$1\mu m$	15	$0.122mS$	$1.06\mu S$	$0.146V$	$10.3\mu A$
M3	$0.27\mu m$	$0.27\mu m$	1	$0.0788mS$	$1.86\mu S$	$0.233V$	$10.3\mu A$
M4	$0.27\mu m$	$0.27\mu m$	1	$0.0789mS$	$1.85\mu S$	$0.233V$	$10.3\mu A$
M5	$4\mu m$	$0.18\mu m$	22.22	$1.31mS$	$37.2\mu S$	$0.19V$	$151\mu A$
M6	$170\mu m$	$1\mu m$	170	$2.52mS$	$21.9\mu S$	$0.27V$	$356\mu A$
M7	$1\mu m$	$1\mu m$	1	$0.0149mS$	$0.140\mu S$	$0.27V$	$2.10\mu A$

Other components are $\boxed{C_c = 0.8pF}$, $\boxed{R_L = 5k\Omega}$, $\boxed{C_L = 5pF}$
DC gain = 1.981003168
Power consumed (approx.) $= V_{dd} * \sum I_{mirrors} = 1.8 * (356 + 20.6 + 2.1) * 10^{-6} = 0.681mJ$

Loop Gain



Loop Gain Plot with Phase at ω_u

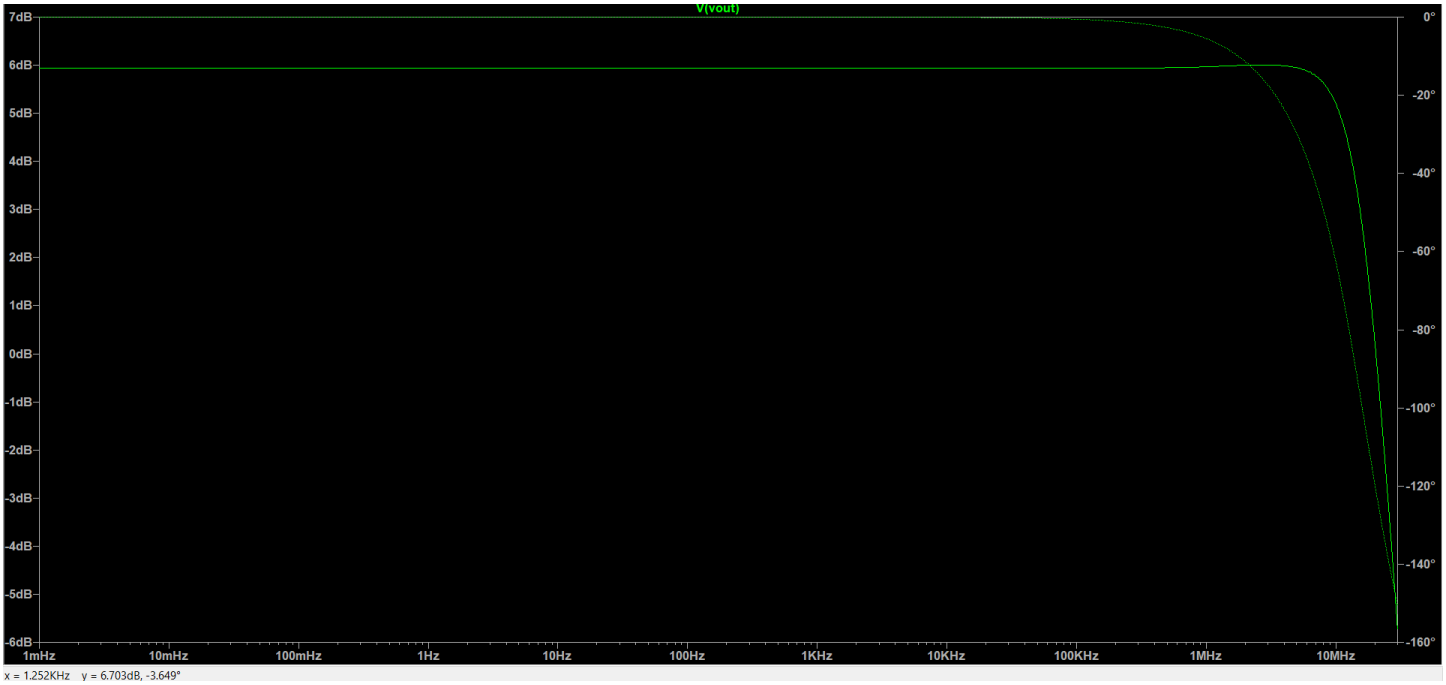
We can see that phase at ω_u = -103.4^o.

Thus, Phase Margin = 180 + ϕ where ϕ = Phase of Open Loop Transfer function at ω_u

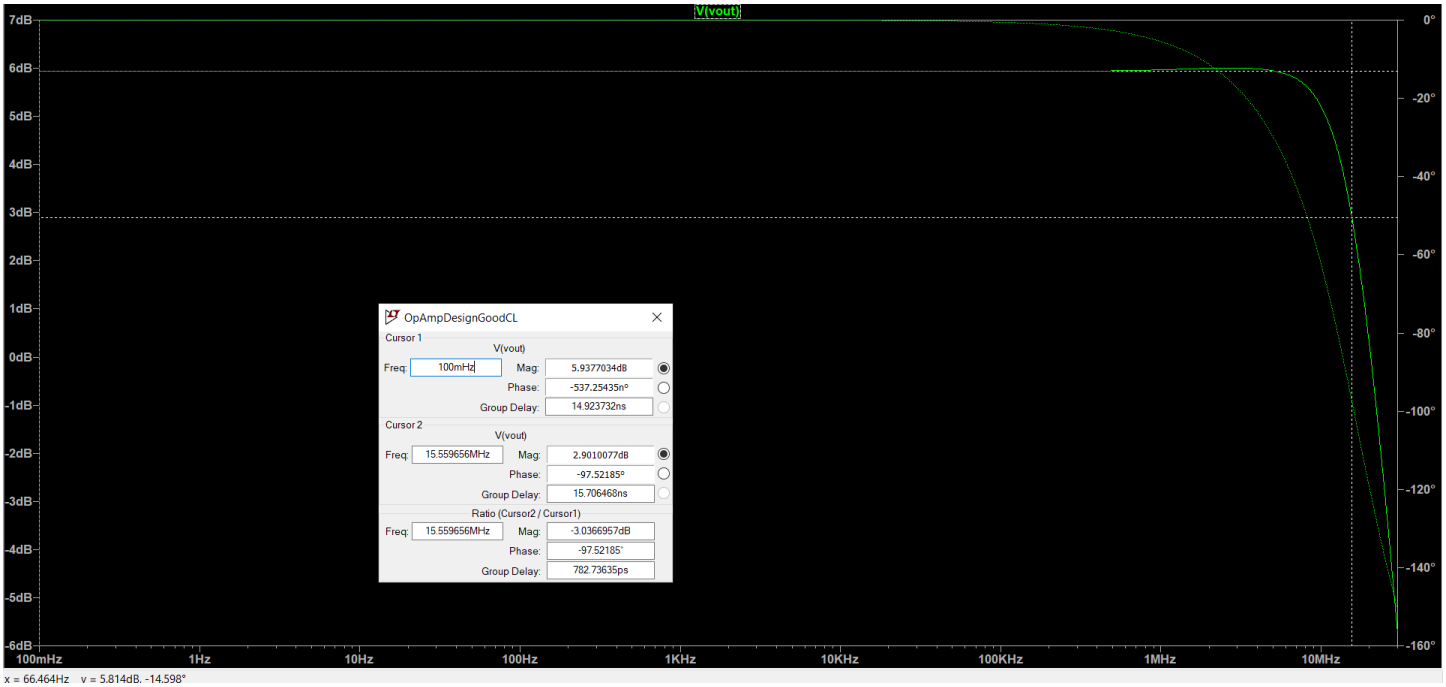
$$\implies PM = 180 - 103.4 = 76.6^o$$

Thus, we have got the Phase Margin at acceptable levels.

Closed Loop Gain



A. Clean Plot of Closed Loop Response

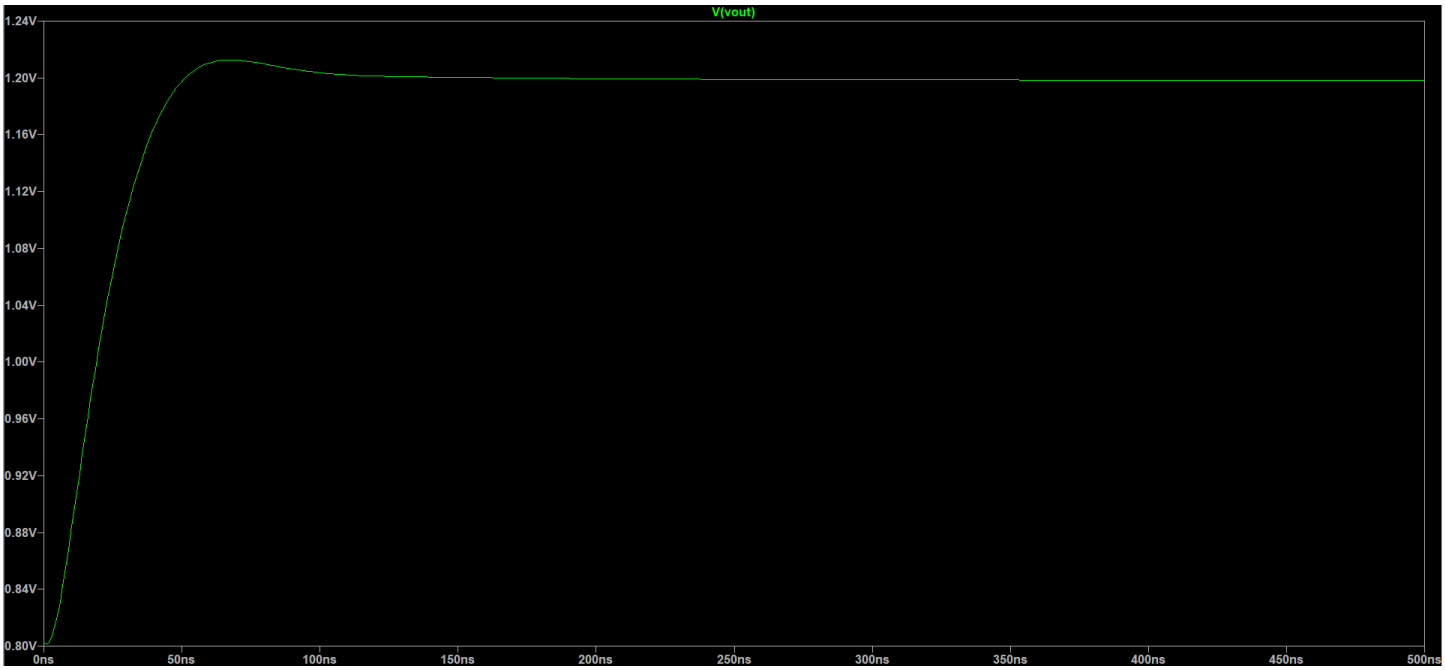


B. Plot of Closed Loop Response with DC Gain and -3dB Gain Frequencies Shown

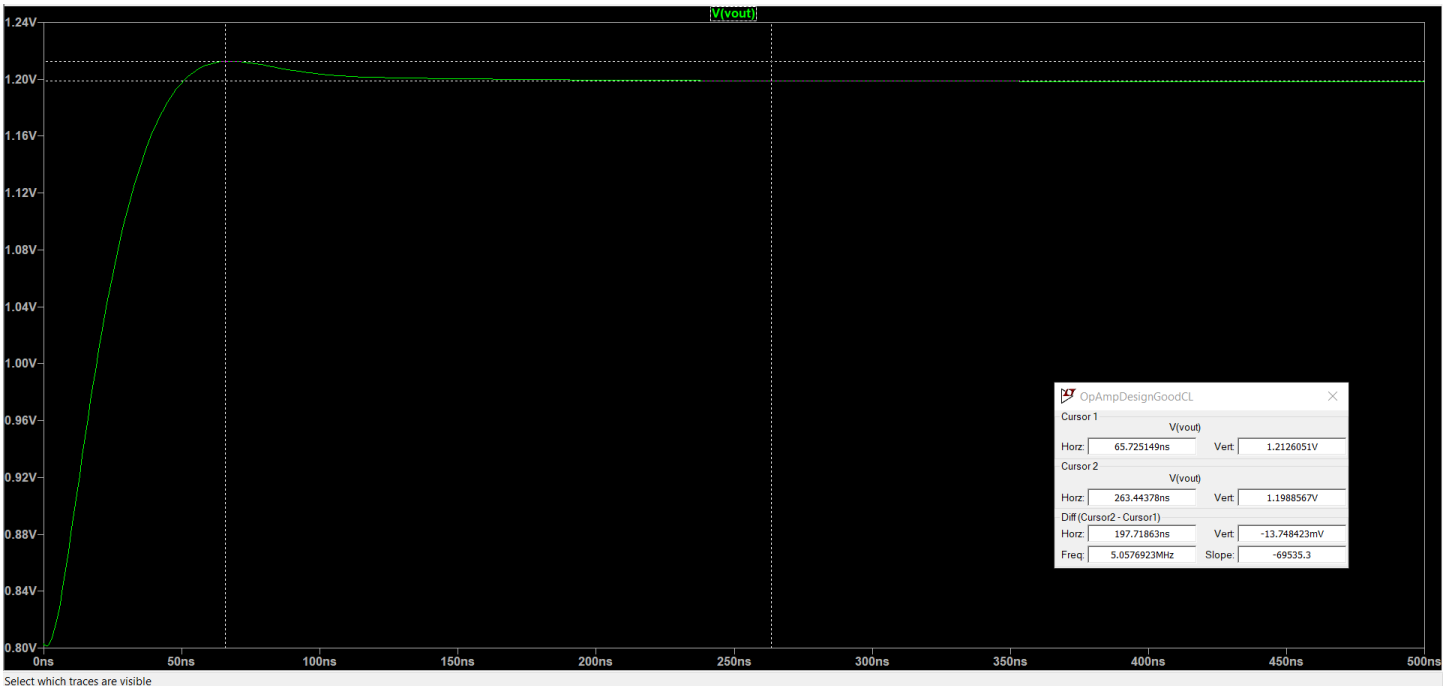
We see that the bandwidth (-3dB) frequency of the function is 15.5MHz, which is much greater than the required 5MHz.
Thus, the bandwidth criteria is satisfied.

Step Response

The step response was given as - Vin goes from 0.4V to 0.6V with rise and settling time = 0.1ns



A. Clean Plot of Step Response



B. Plot of Step Response with Values Shown

$$\text{Overshoot percentage} = \frac{(1.2126 - 1.1989) * 100}{1.1989} = 1.054738625\%$$

Conclusion

Thus, we were able to simulate the opamp with following properties :

- DC Gain = 1.981003168
- Bandwidth = 15.55 MHz
- Phase Margin = 76.6^o