EE204 – Submission deadline 25th May, 2019
Last Assignment, Partial, submission through Moodle.

Submit a comprehensive report for the following design problems. The report should consist of the following things:

A. Design methodology
B. Analytical design as obtained from the understanding of the circuit. In this case, the MOSFET will be replaced by an appropriate small signal model based on the bias condition and the circuit has to be first analytically designed. The entire design has to be properly depicted.
C. All the circuits and plots should have proper label.
D. The source code should be attached. The code should generate all the plots as required for the respective problems.
E. Use V_{DD} = +5 V

1. Using the model file shared in Moodle, design a differential amplifier in SPICE with differential input and single ended output with the following specifications:
    a. The amplifier is designed as a cascade combination of differential input single ended output followed by a source follower.
    b. The circuit is designed without any resistor and inductor.
    c. The differential gain of the amplifier is given > 10^4.
    d. The output impedance of the amplifier is 100 ohm or less.
    e. Draw the Bode plot for the gain and phase.
    f. When the circuit is used as an OPAMP in inverting amplifier configuration with R_1 = 1 kΩ and R_2 = 2 kΩ, check if the gain is approximately -2.
    g. Draw the Bode plot the gain and frequency for the amplifier in (f).
    h. Compare the gain-bandwidth product obtained in (e) and (g).
2. Design a low pass (1 kHZ cutoff), high pass (10 kHz cut off) and band pass (pass band 1 kHz to 10 kHz) filter in SPICE using the amplifier designed in (1). The pass band gain in each of the filter ~10 dB.
3. Design a Wein bridge Oscillator in SPICE using the amplifier design in (a) for an oscillating frequency of 1 kHz.
4. Design a cross-coupled oscillator for an oscillating frequency of 1 kHz using the circuit in (1).
5. Design a negative differential resistor using (1). Choose an appropriate topology.