Total No. of Questions : 8]

SEAT No. : ____

PA-1191

[Total No. of Pages : 2

[5925]-213

S.E. (Electronics/E & T.C/Electronics & Computer)

DIGITAL CIRCUITS

(2019 Pattern) (Semester-III) (204182)

Time : 2½ Hours] ***[Max. Marks : 70***

Instructions to the candidates:

1) ***Answer Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.8.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***

Q1) a) Draw the logic diagram of full-adder and its truth table. **[7]**

b) Implement a full-adder using Demultiplexer. **[5]**

c) Implement the given logic function using a 4:1 multiplexer **[5]**

$$f(A,B,C) = \sum m(0,2,4,6)$$

OR

Q2) a) Explain the working of a half-adder? Draw its logic diagram. **[7]**

b) Implement the full subtractor using a 1:8 demultiplexer. **[5]**

c) Implement the following function using multiplexer **[5]**

$$f(A,B,C) = \sum m(0,2,4,6)$$

Q3) a) Design a sequence generator using T FFs. **[8]**

b) Explain the types of shift register. **[5]**

c) Explain with diagram the working of D type Flip-flop. Give its truth table. **[5]**

OR

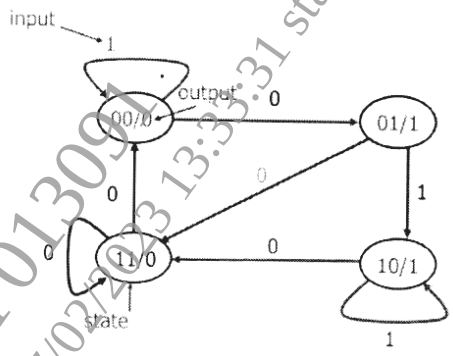
Q4) a) Design a 3-Bit synchronous counter using JK FF. **[8]**

b) With the neat diagram, explain the working operation of 4-bit SISO. **[5]**

c) Explain S-R flip-flop using NOR gates. **[5]**

P.T.O.

Q5) a) Design the clocked sequential circuit for the state diagram using JK flip flop. **[9]**



b) Draw ASM chart for 2 bit binary counter having one enable line E such that: E=1, **[8]**

c) Count Enable and E=0, Count Disable.

OR

Q6) a) Design a sequence detector to detect a sequence 1101 using D FF **[9]**
(Use Moore machine).

b) Explain in short: **[8]**
i) State Assignment
ii) ASM chart

Q7) a) Explain the classification based on their physical characteristics. **[8]**

b) Explain the concept of PLA with the help of a block diagram. **[10]**

OR

Q8) a) Explain the meaning of static and dynamic memories. State their applications. **[8]**

b) Describe with neat diagram AND-OR structure of PLA and PAL. **[10]**

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