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Lab #2

Intro to Hierarchical design

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CST 231 – DIGITAL SYSTEM DESIGN I

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Abstract

For this lab you are to design a basic 16-bit counter with reset and enable signals. You will need to divide the system clock into something more useful as 50MHz is way too fast. You will then display that counter on the 7-segment displays.

Introduction

The goal of this lab was to create a 16-bit counter that displays the count to several seven segment displays. A clock divider was needed to slow the counting, since it is incrementing on the clock's positive edge. The counter must have a reset, clock, and enable.

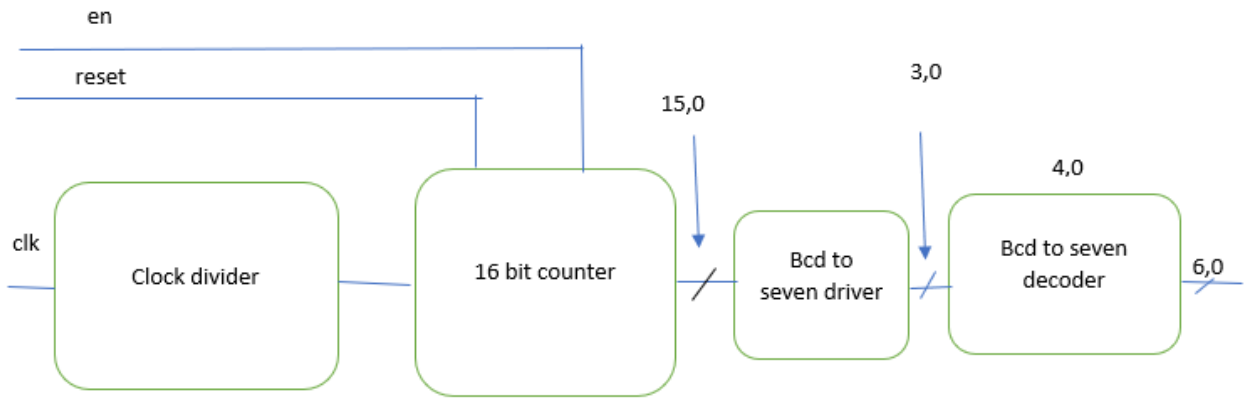

Figure 1: block diagram

Design

Physical hardware design

The only necessary hardware was the DE1-SoC development board. Inputs and outputs were included on the board.

Synthesized hardware design

A clock divider was needed to reduce the speed of counting. It has an input of the board's clock. A counter was connected to this output. This counter's output was fed to a driver for multiple seven segment displays. This driver broke up large numbers into single digits and output the number in BCD. This BCD, for each digit, was sent to five seven-segment decoders. These decoders were wired to HEX0 through HEX4. All of these modules were accessed by the top-level module named, "lab02". Two switches were used to create an enable and reset.

Design Structure

See figure 1 for block diagram of lab 2. To reuse the BCD decoder, this module needed a driver that would split large numbers into single digit outputs for the BCD decoder to use.

Modules

clk_divider

See figure 2 for clk_divider RTL. This clock divider uses registers to affect the output. It has parameters to affect the output frequency. One parameter makes the resulting clock speed to be frequency *

1/(2N). The other parameter is the number of bits needed to store parameter one. The input is from the board's clock. The output is the divided clock.

counter

See figure 3 for counter RTL. Counter accepts one parameter and one input. The parameter is the number of bits the counter can count to. The input is the clock. On positive edge of the clock, the counter increments. It outputs the count in BCD form.

bcd_to_seven_driver

See figure 4 for bcd_to_seven_driver RTL. This module accepts a large BCD number. This driver breaks down the number into separate digits. These BCD digits are output separately and cannot exceed 9.

bcd_decoder

See figure 5 for bcd_decoder RTL. This accepts single digit BCD numbers and outputs the seven segment display equivalent.

Simulation and Testing

Each module was tested individually. See figures 7 – 9 for module simulations. The only inputs that effected the program were enable and reset. Each functioned correctly. The enable makes the counter continue to count. The reset resets the number to zero.

Problems

The top-level module contained errors at first. The counter module was outputting 16 bits, but the wire connecting it to the driver was only one bit long. Changing it fixed the undefined behavior.

Results and Conclusion

The lab was executed correctly. It has helped my knowledge on using parameters and configuring inputs and outputs automatically.

Appendix

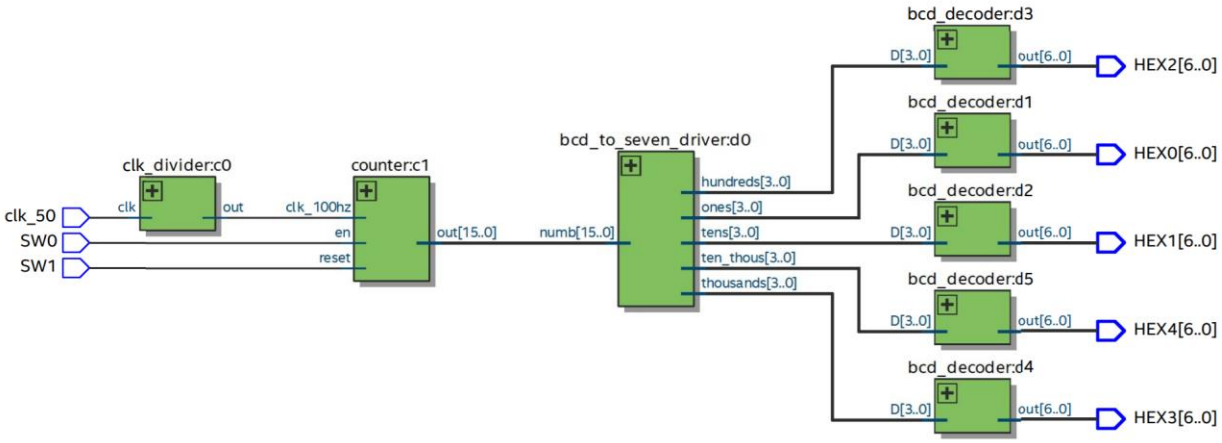

Figure 2: Top level block diagram

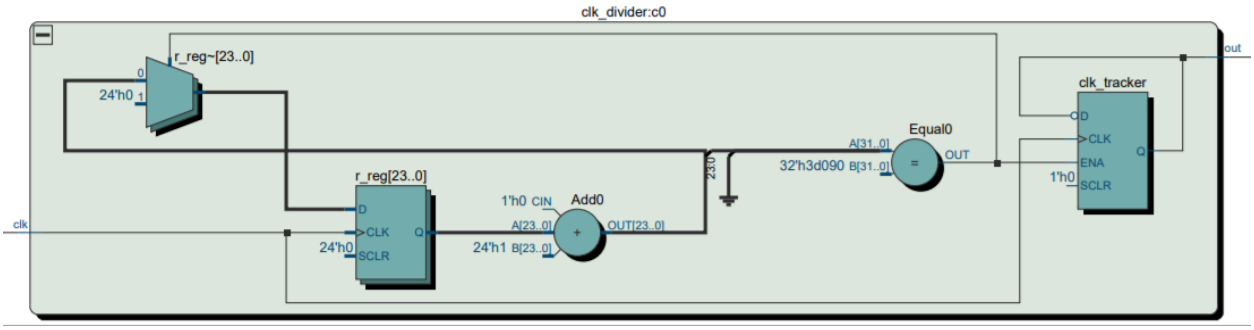

Figure 3: clk_divider RTL

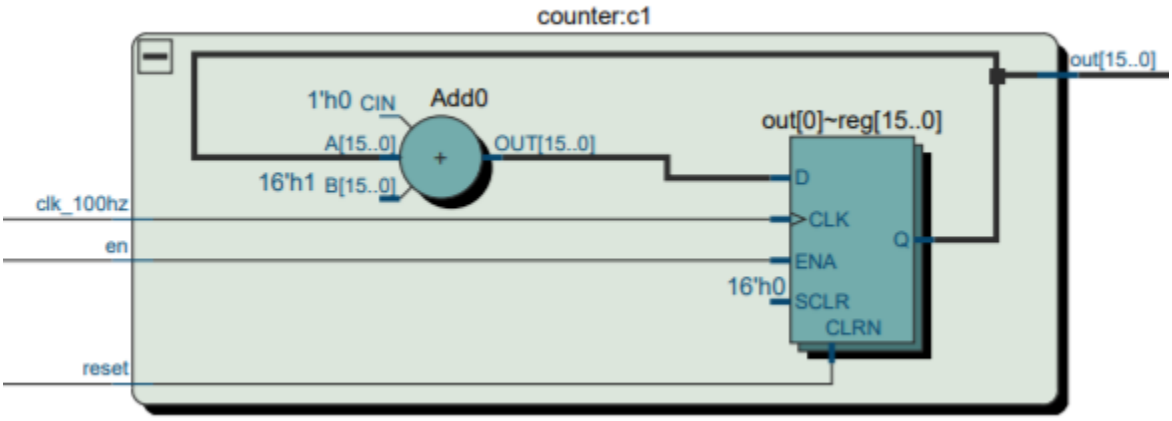

Figure 4: counter RTL

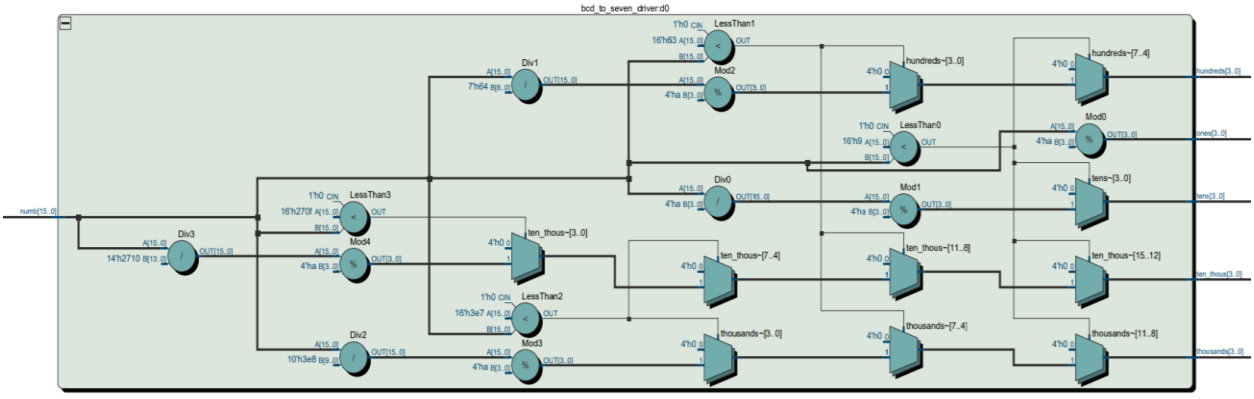

Figure 5: bcd_to_seven_driver RTL

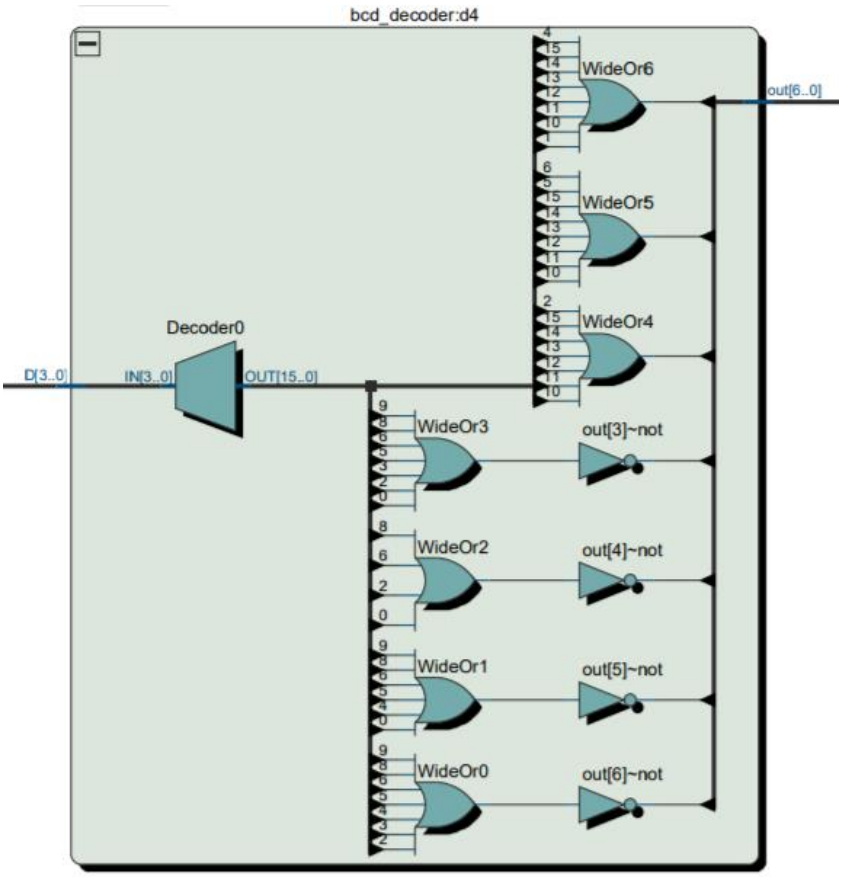

Figure 6: bcd_decoder RTL

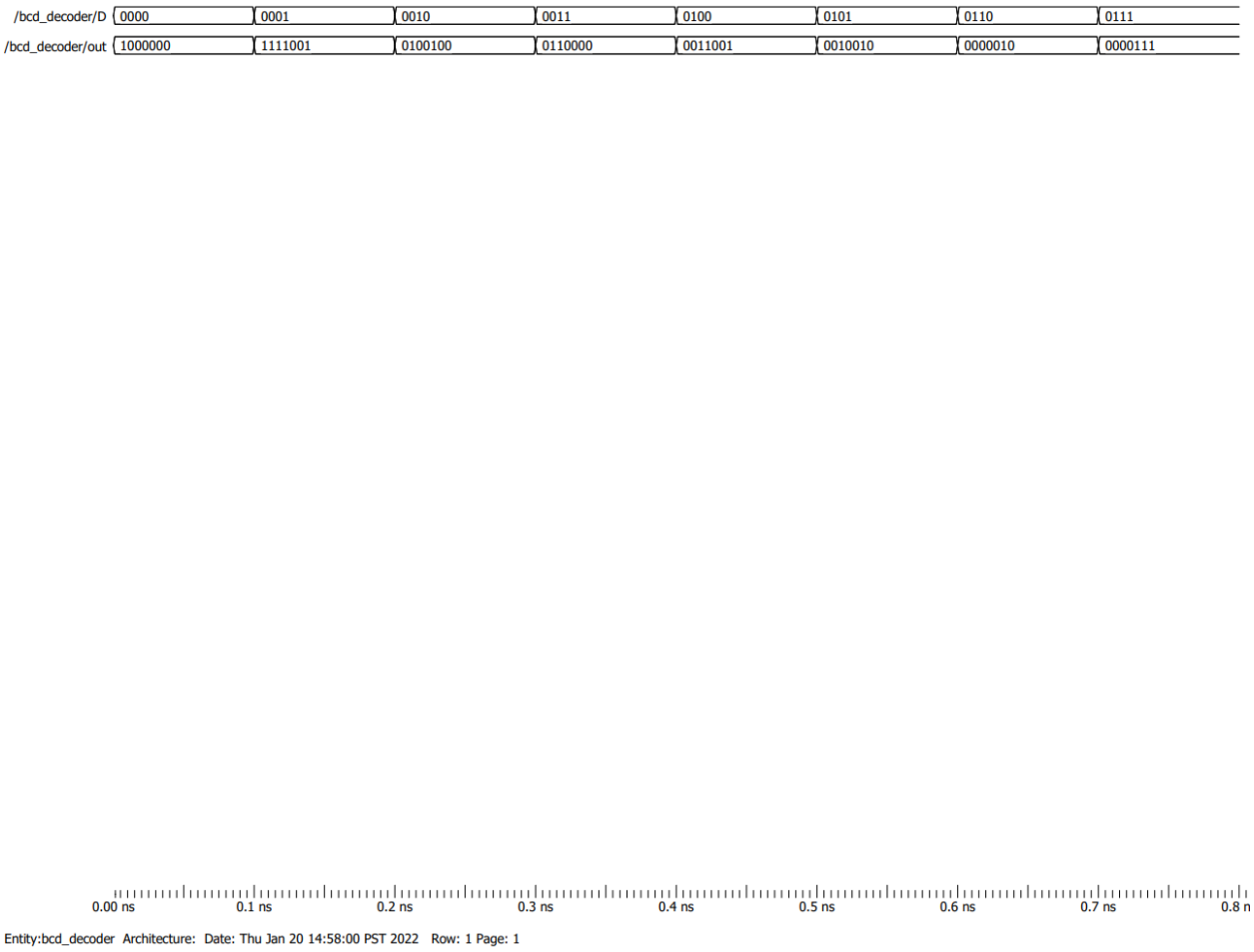

Figure 7: bcd_decoder simulation

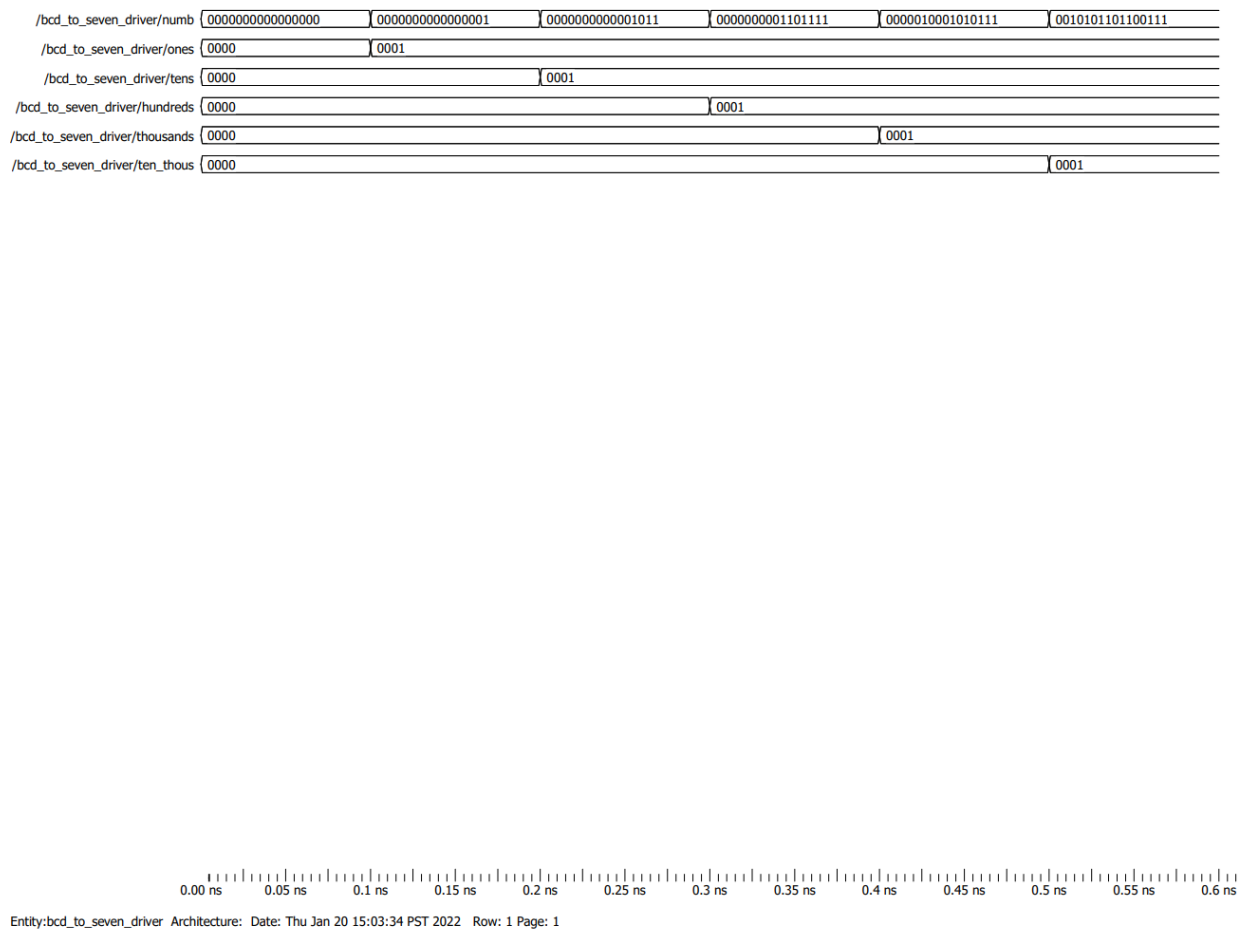

Figure 8: bcd_to_seven_driver simulation

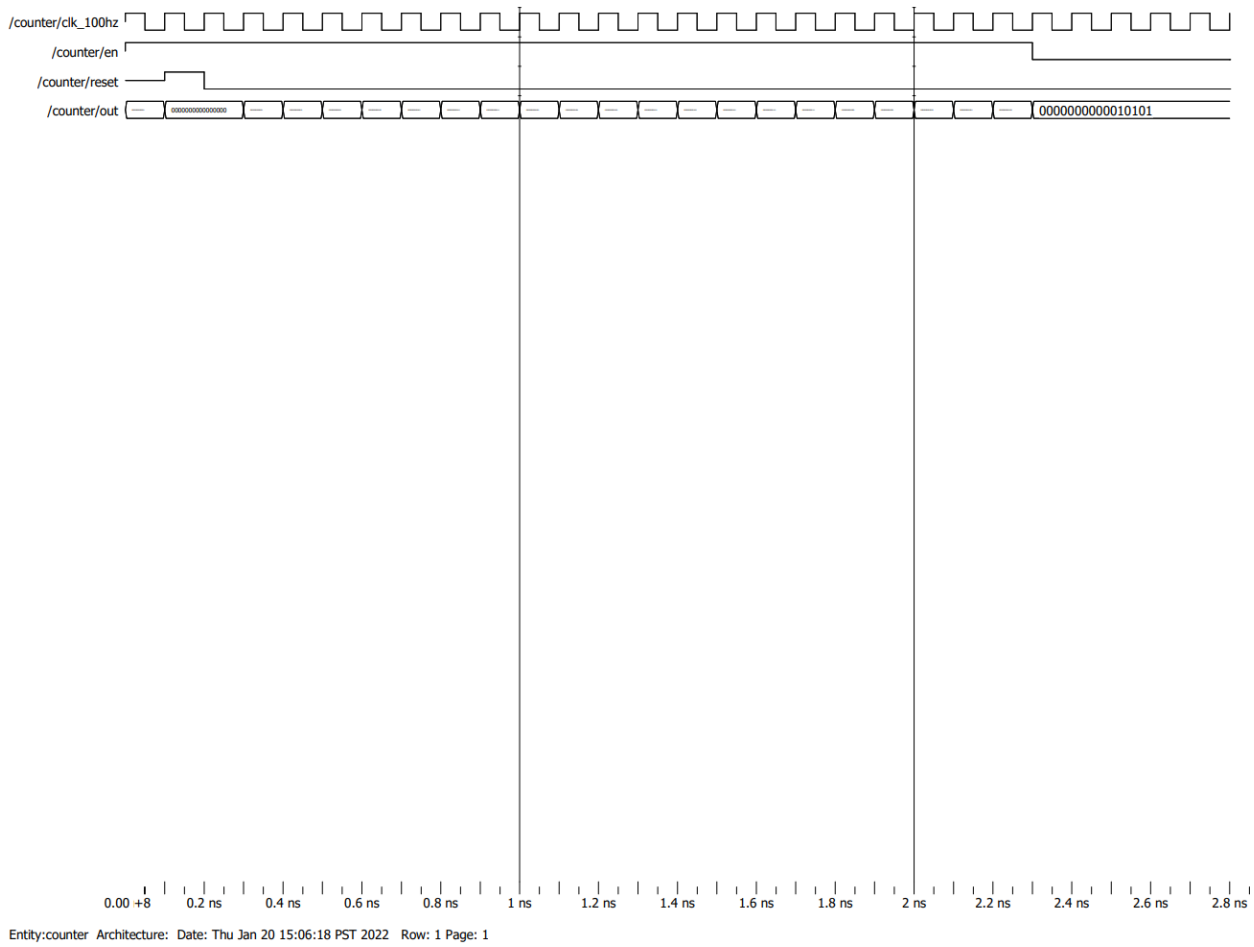

Figure 9: counter simulation

Table 1: pin mapping

Node Name	Customize Columns...	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved	Current Strength	S
HEX0[0]		Unknown	PIN_AE26	5A	B5A_N0	3.3-V LVTTL		16mA (default)	
HEX0[1]		Unknown	PIN_AE27	5A	B5A_N0	3.3-V LVTTL		16mA (default)	
HEX0[2]		Unknown	PIN_AE28	5A	B5A_N0	3.3-V LVTTL		16mA (default)	
HEX0[3]		Unknown	PIN_AG27	5A	B5A_N0	3.3-V LVTTL		16mA (default)	
HEX0[4]		Unknown	PIN_AF28	5A	B5A_N0	3.3-V LVTTL		16mA (default)	
HEX0[5]		Unknown	PIN_AG28	5A	B5A_N0	3.3-V LVTTL		16mA (default)	
HEX0[6]		Unknown	PIN_AH28	5A	B5A_N0	3.3-V LVTTL		16mA (default)	
HEX1[0]		Unknown	PIN_AJ29	5A	B5A_N0	3.3-V LVTTL		16mA (default)	
HEX1[1]		Unknown	PIN_AH29	5A	B5A_N0	3.3-V LVTTL		16mA (default)	
HEX1[2]		Unknown	PIN_AH30	5A	B5A_N0	3.3-V LVTTL		16mA (default)	
HEX1[3]		Unknown	PIN_AG30	5A	B5A_N0	3.3-V LVTTL		16mA (default)	
HEX1[4]		Unknown	PIN_AF29	5A	B5A_N0	3.3-V LVTTL		16mA (default)	
HEX1[5]		Unknow	PIN_AF30	5A	B5A_N0	3.3-V LV		16mA (de	

Node Name	Customize Columns...	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved	Current Strength
		n				TTL		fault)
HEX1[6]		Unknown	PIN_AD27	5A	B5A_N0	3.3-V LVTTL		16mA (default)
HEX2[0]		Unknown	PIN_AB23	5A	B5A_N0	3.3-V LVTTL		16mA (default)
HEX2[1]		Unknown	PIN_AE29	5B	B5B_N0	3.3-V LVTTL		16mA (default)
HEX2[2]		Unknown	PIN_AD29	5B	B5B_N0	3.3-V LVTTL		16mA (default)
HEX2[3]		Unknown	PIN_AC28	5B	B5B_N0	3.3-V LVTTL		16mA (default)
HEX2[4]		Unknown	PIN_AD30	5B	B5B_N0	3.3-V LVTTL		16mA (default)
HEX2[5]		Unknown	PIN_AC29	5B	B5B_N0	3.3-V LVTTL		16mA (default)
HEX2[6]		Unknown	PIN_AC30	5B	B5B_N0	3.3-V LVTTL		16mA (default)
HEX3[0]		Unknown	PIN_AD26	5A	B5A_N0	3.3-V LVTTL		16mA (default)
HEX3[1]		Unknown	PIN_AC27	5A	B5A_N0	3.3-V LVTTL		16mA (default)
HEX3[2]		Unknown	PIN_AD25	5A	B5A_N0	3.3-V LVTTL		16mA (default)
HEX3[3]		Unknown	PIN_AC25	5A	B5A_N0	3.3-V LVTTL		16mA (default)
HEX		Unk	PIN_	5B	B5B_	3.3-		16m

Node Name	Customize Columns...	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved	Current Strength
3[4]		nown	AB28		N0	V LVTTL		A (default)
HEX3[5]		Unknown	PIN_AB25	5A	B5A_N0	3.3-V LVTTL		16mA (default)
HEX3[6]		Unknown	PIN_AB22	5A	B5A_N0	3.3-V LVTTL		16mA (default)
HEX4[0]		Unknown	PIN_AA24	5A	B5A_N0	3.3-V LVTTL		16mA (default)
HEX4[1]		Unknown	PIN_Y23	5A	B5A_N0	3.3-V LVTTL		16mA (default)
HEX4[2]		Unknown	PIN_Y24	5A	B5A_N0	3.3-V LVTTL		16mA (default)
HEX4[3]		Unknown	PIN_W22	5A	B5A_N0	3.3-V LVTTL		16mA (default)
HEX4[4]		Unknown	PIN_W24	5A	B5A_N0	3.3-V LVTTL		16mA (default)
HEX4[5]		Unknown	PIN_V23	5A	B5A_N0	3.3-V LVTTL		16mA (default)
HEX4[6]		Unknown	PIN_W25	5B	B5B_N0	3.3-V LVTTL		16mA (default)
SW0		Unknown	PIN_AB12	3A	B3A_N0	3.3-V LVTTL		16mA (default)
SW1		Unknown	PIN_AC12	3A	B3A_N0	3.3-V LVTTL		16mA (default)
clk_50		Unknown	PIN_AF14	3B	B3B_N0	3.3-V LVTTL		16mA (default)

Table of Figures

References

"Reference designer," *Verilog Example - Clock Divide by even number*. [Online]. Available: http://www.referencedesigner.com/tutorials/verilogexamples/verilog_ex_04.php. [Accessed: 21-Jan-2022].