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Lab #3

Up down counter implemented on CL3641AH

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CST 231 – DIGITAL SYSTEM DESIGN I
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Abstract

The objective of this lab is to implement an up down counter on a muxed seven segment display component, the CL3641AH. The development board used is the Cyclone V. We are interfacing with the CL3641AH seven segment display. To do this, the GPIO_0 on the development board will be used to interface with the component. I had serious problems completing this lab. The first issue was that my component was faulty. The B segment was bad, and the ones digit does not work. The second issue was my wiring. I initially wired the component wrong, leading to garbage being displayed. Overall, I found this lab to be very difficult. It was nice completing it, and it feels like I have learned a lot about different aspects of embedded design. One aspect that will help me in the future is troubleshooting. I have learned to not rely on just my code being faulty, but to also look at components and wiring. This lab helped me realize that timing is very important and metastability is bad. Although I had setbacks, I have learned a lot.

Introduction

The objective of this lab is to implement an up down counter on a muxed seven segment display component, the CL3641AH. This lab allowed the student to learn about interfacing with third party components.

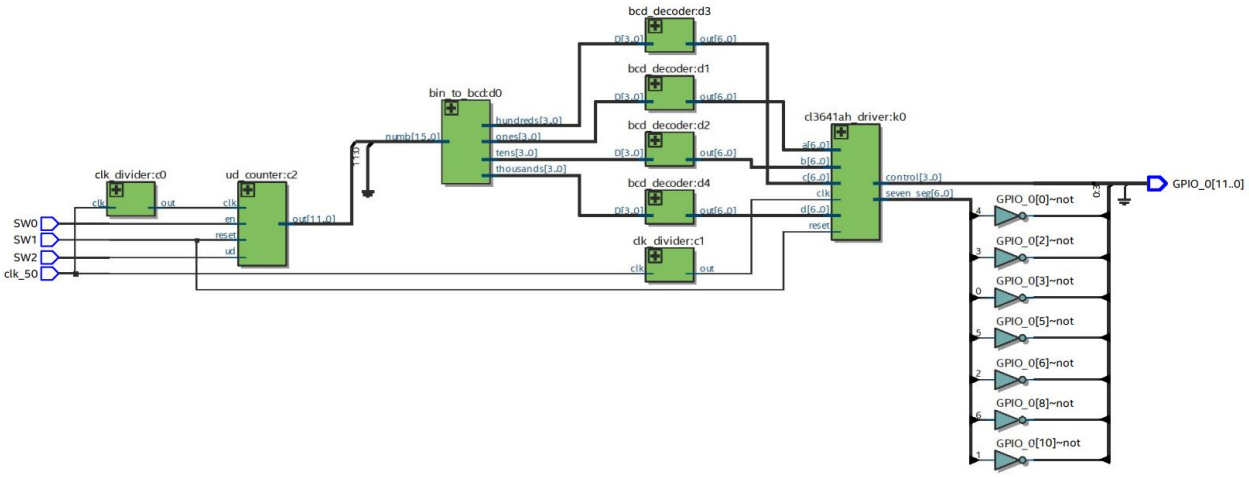

Figure 1: Top level block diagram of project

Design

Physical hardware design

The development board used is the Cyclone V. We are interfacing with the CL3641AH seven segment display. To do this, the GPIO_0 on the development board will be used to interface with the component. See figure 2 for Cyclone pinout. The first twelve pins are used on GPIO_0. Pins 11 and 12 must be skipped since they are ground and Vcc. The seven-segment display will be connected to each pin with a resistor, limiting the voltage. At 10 mA, the ideal voltage would be 1.8 V as shown in the component documentation.

Forward Voltage	VF	1.8		V	IF=10mA

Figure 2: Forward Voltage of CL341AH

$$V_f = 1.8\,V\ at\ 10mA$$

$$v_{GPIO} = 3.3\,V$$

$$i_{\mathrm{GPIOMAX}} = 1.5A$$

$$R = \frac{3.3\,v - 1.8\,v}{.010\,A} = 150\ ohm$$

$$at\ 5mA$$

$$R = \frac{3.3\,v - 1.8\,v}{.005\,A} = 300\ ohms$$

$$150 \leq R \leq 300$$

Figure 3: resistance calculations

It was found that the resistor should be between 150 and 300 ohms for proper voltage levels. To connect the component, a single resistor is placed between the CL3641AH and the GPIO_0 pins. See figure below.

Figure 4: Wiring schematic

CL3641AH uses active high seven segment displays, but active low mux controls to display which digit. See figure 6 for the schematic for the seven-segment display. The top pins are used as controls for the internal mux. The bottom pins are the seven segment controls. This display uses a common cathode for the seven segments.

Synthesized hardware design

Design Structure

See figure 1 for top level block diagram. Three switches are used for enable, reset, and up down set. The board's clock is used to drive the logic. Two clock dividers are used to slow the clock. One regulates the counter and the other regulates the component's displays. An up down counter is used to count up or down. This output is sent to a binary to bcd decoder. This splits the number into ones, tens, hundreds, and thousands digits. These digits are sent to a bcd decoder. These outputs from the four bcd decoders feed into the CL3641AH driver. This driver handles the output to the component.

Modules

Clk_divider

This module slows the clock to a given frequency. The input is the system clock. The output is the desired clock speed. See Lab 2 for more information about the clock divider.

Ud_counter

This module counts up or down. It counts up or down with a parameterized bit length. The inputs are clock, enable, reset, and updown. When updown is high, the module counts up. See figure 7 for ud_counter RTL. See figure 8 for ud_counter simulation.

Bin_to_bcd

Converts 16-bit binary number to single digit bcd. See figure 9 for bin_to_bcd RTL. See figure 10 for bin_to_bcd simulation.

Bcd_decoder

Decodes single bcd digit to seven segment display encoding. See lab 2 for more details.

Cl3641ah_driver

Drives a muxed, 4 digit, seven segment display. The inputs for this module are a clock, a reset, and the data for each seven segment. The clock feeds into the mux controller that count. This count feeds into a controller for the mux in the component. It also feeds into a mux that chooses which digit to output. See figure 11 for RTL. See figure 12 for simulation.

Simulation and Testing

See appendix for simulations of modules. All modules acted as specified in the section above.

Problems

I had serious problems completing this lab. The first issue was that my component was faulty. The B segment was bad, and the ones digit does not work. The second issue was my wiring. I initially wired the component wrong, leading to garbage being displayed.

Results and Conclusion

Overall, I found this lab to be very difficult. It was nice completing it, and it feels like I have learned a lot about different aspects of embedded design. One aspect that will help me in the future is troubleshooting. I have learned to not rely on just my code being faulty, but to also look at components and wiring. This lab helped me realize that timing is very important and metastability is bad. Although I had setbacks, I have learned a lot.

Appendix

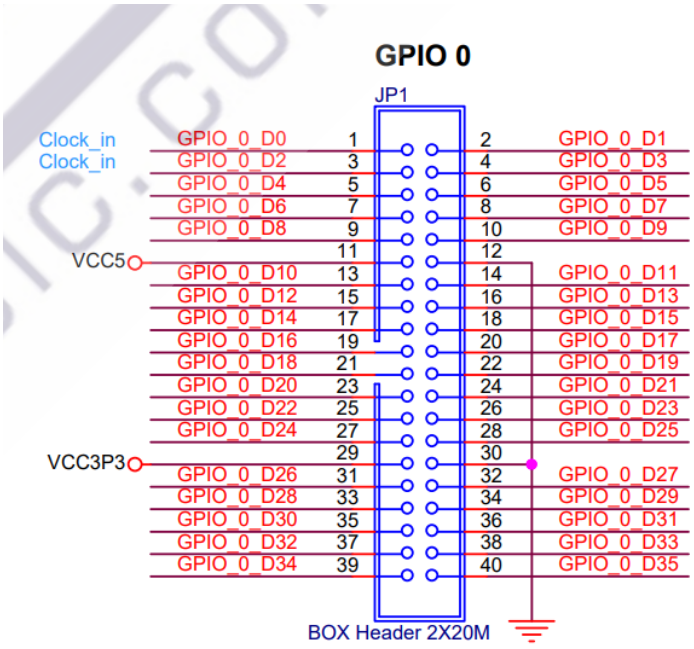

Figure 5: Cyclone V GPIO_0 pinout

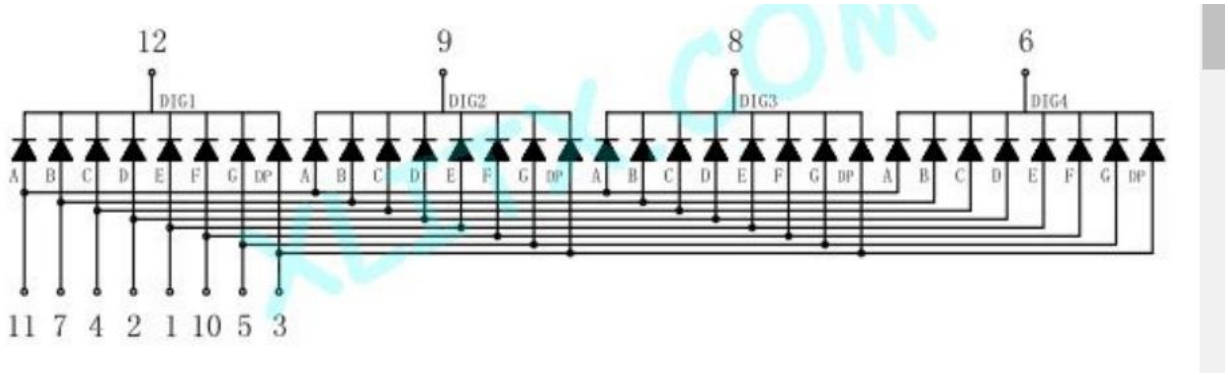

Figure 6:CL3641AH schematic

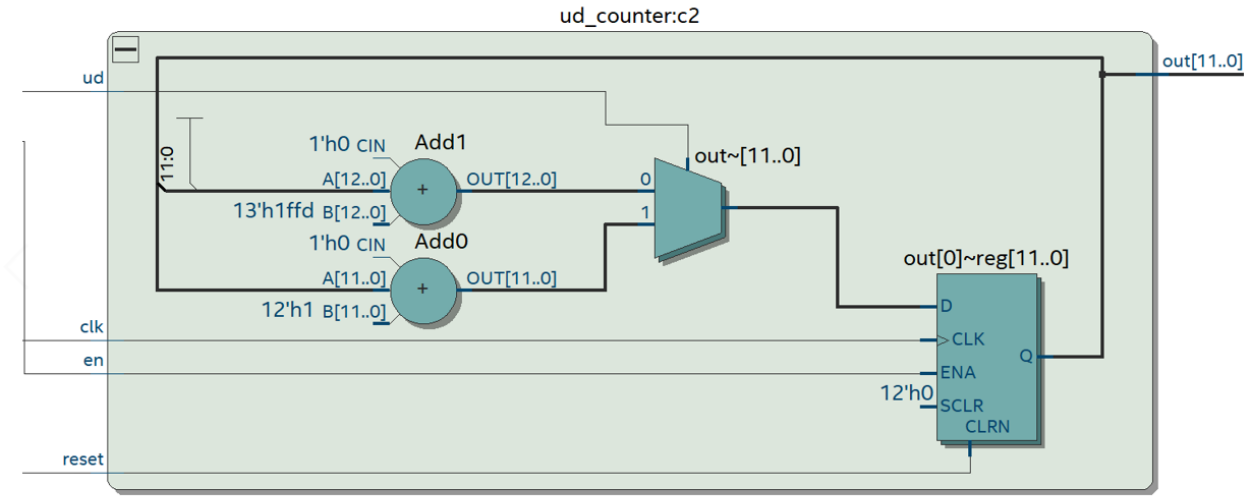

Figure 7: ud_counter RTL

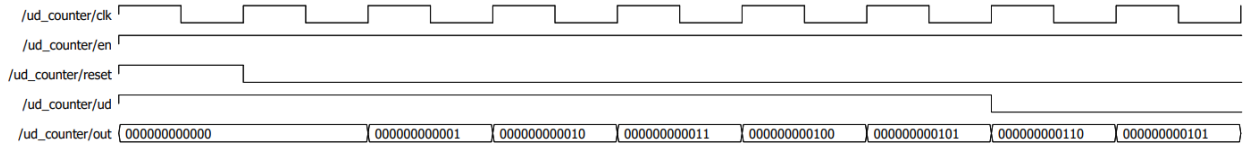

Figure 8: ud_counter simulation

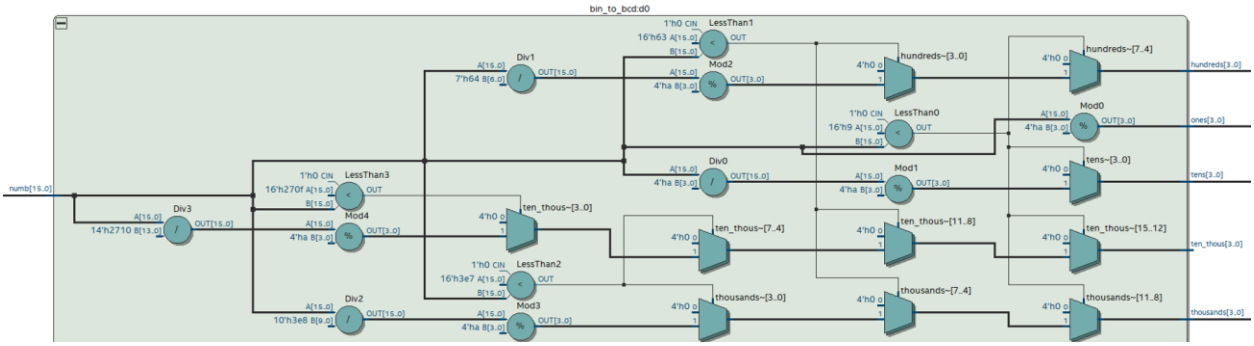

Figure 9: bin_to_bcd RTL

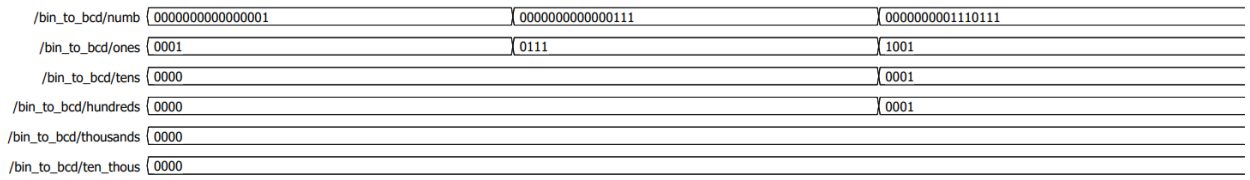

Figure 10: bin_to_bcd simulation

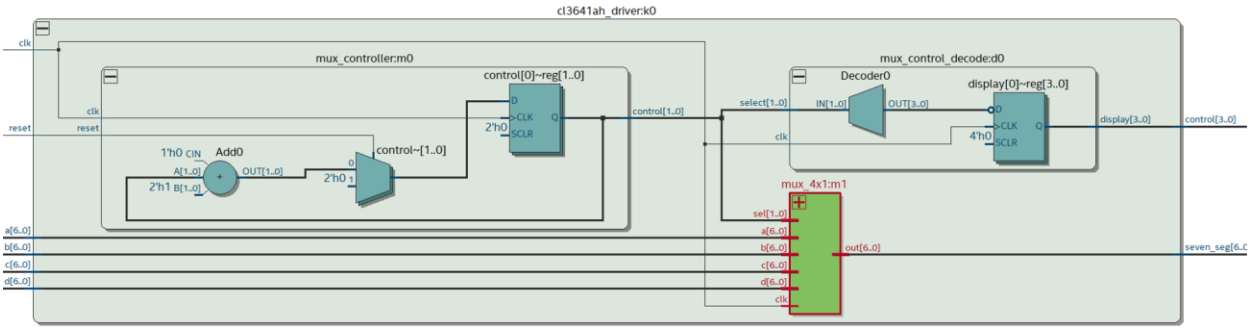

Figure 11: cl3641ah_driver RTL

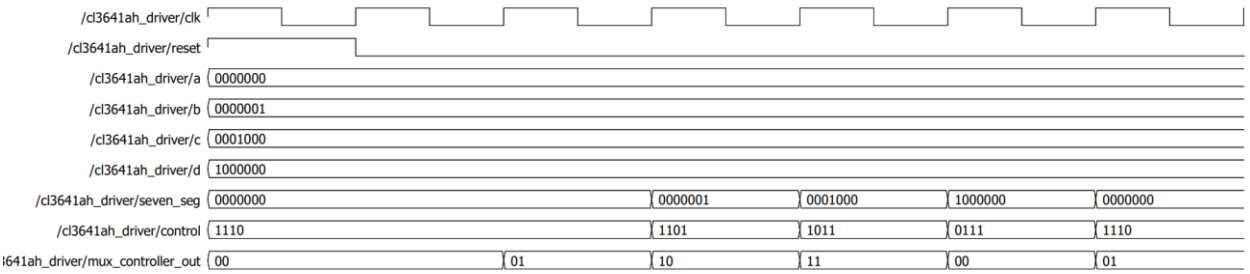

Figure 12: cl3641ah_driver simulation

Node Name	Customize Columns...	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	Transceiver Analog Settings Protocol	VCCR_GXB/VCCT_GXB Voltage	Transceiver I/O Pin Termination	Transceiver Dedicated Refclk Pin Termination	Transmitter Common Mode Driver Voltage	Transmitter Slew Rate Control	Transmitter Differential Output Voltage	Receiver Buffer Common Mode Voltage	Strict Preservation
GPIO_0[0]		Unknown	PIN_AC18	4A	B4A_N0	3.3V LV TTL		16mA (default)											
GPIO_0[10]		Unknown	PIN_AG16	4A	B4A_N0	3.3V LV TTL		16mA (default)											
GPIO_0[11]		Unknown	PIN_AE16	4A	B4A_N0	3.3V LV TTL		16mA (default)											
GPIO_0[1]		Unknown	PIN_Y17	4A	B4A_N0	3.3V LV TTL		16mA (default)											
GPIO_0[2]		Unknown	PIN_AD17	4A	B4A_N0	3.3V LV TTL		16mA (default)											
GPIO_0[3]		Unknown	PIN_Y18	4A	B4A_N0	3.3V LV TTL		16mA (default)											
GPIO_0[4]		Unknown	PIN_AK16	4A	B4A_N0	3.3V LV TTL		16mA (default)											
GPIO_0[5]		Unknown	PIN_AK18	4A	B4A_N0	3.3V LV TTL		16mA (default)											
GPIO_0[6]		Unknown	PIN_AK19	4A	B4A_N0	3.3V LV TTL		16mA (default)											
GPIO_0[7]		Unknown	PIN_AJ19	4A	B4A_N0	3.3V LV TTL		16mA (default)											
GPIO_0[8]		Unknown	PIN_AJ17	4A	B4A_N0	3.3V LV TTL		16mA (default)											

Figure 13: pinout of lab 3

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References

"Reference designer," *Verilog Example - Clock Divide by even number*. [Online]. Available: http://www.referencedesigner.com/tutorials/verilogexamples/verilog_ex_04.php. [Accessed: 21-Jan-2022].

"CL3641AH documentation," [online]. Available: http://www.xlitx.com/datasheet/CL3641AH.pdf [Accessed: 21-Jan-2022].