



AVR[®] DU Family

AVR[®] DU Product Brief

Introduction

The AVR[®] DU family of microcontrollers is using the AVR[®] CPU with a hardware multiplier running at clock speeds up to 24 MHz. They include 16/32/64 KB of Flash, 2/4/8 KB of SRAM, and 256 bytes of EEPROM. The microcontrollers are available in 14-, 20-, 28-, and 32-pin packages. The family uses the latest technologies from Microchip Technology, with a flexible and low-power architecture, including Event System, intelligent analog features, and advanced digital peripherals such as a USB 2.0 full-speed device.

Features

- AVR[®] CPU
 - Running at up to 24 MHz
 - Single-cycle I/O access
 - Two-level interrupt controller
 - Two-cycle hardware multiplier
 - Immutable boot
 - Supply voltage range: 1.8V to 5.5V
- Memories
 - 16/32/64 KB in-system self-programmable Flash memory with a true read-while-write operation
 - 2/4/8 KB SRAM
 - 256B EEPROM
 - 512B of user row in nonvolatile memory that can keep data during chip erase and be programmed while the device is locked
 - 256B of boot row
 - Write/erase endurance
 - Flash 10,000 cycles
 - EEPROM 100,000 cycles
 - Data retention: 40 years at 55°C
- System
 - Power-on Reset (POR) circuit
 - Brown-out Detector (BOD)
 - Voltage Level Monitor (VLM) with interrupt at a programmable level above the BOD
 - Clock options
 - High-precision internal high-frequency oscillator with selectable frequency up to 32 MHz (OSCHF)
 - Auto-tuning for improved internal oscillator accuracy
 - 32.768 kHz internal oscillator (OSC32K)
 - 32.768 kHz external crystal oscillator (XOSC32K)
 - External clock input
 - External high-frequency crystal oscillator (XOSCHF) with clock failure detection
 - Single-pin Unified Program and Debug Interface (UPDI)
 - Three sleep modes

- Idle with all peripherals running for immediate wake-up
- Standby with a configurable operation of selected peripherals
- Power-Down with full data retention
- Automated Cyclic Redundancy Check (CRC) Flash memory scan
- Watchdog Timer (WDT) with Window mode, with a separate on-chip oscillator
- External interrupt on all general purpose pins
- Peripherals
 - One 16-bit Timer/Counter type A (TCA) with three compare channels for Pulse-Width Modulation (PWM) and waveform generation
 - Two 16-bit Timer/Counter type B (TCB) with input capture and signal measurements
 - One 16-bit Real-Time Counter (RTC) that can run from an external crystal or internal oscillator
 - One USB 2.0 full-speed device⁽¹⁾
 - Optional internal 3.3V voltage regulator
 - OSCHF oscillator can be tuned to the USB start-of-frames (SOFs) for crystal-less operation
 - 16 endpoint addresses each with one input and one output endpoint for up to 31 endpoints
 - Multi-Packet transfer for reduced interrupt load and software intervention
 - Two USARTs
 - Operation modes: RS-485, LIN client, SPI host, and IrDA
 - Fractional baud rate generator, auto-baud, and start-of-frame detection
 - One SPI with host/client operation modes
 - One Two-Wire Interface (TWI) with dual address match
 - Simultaneous host/client operation (dual mode)
 - Philips Inter-Integrated Circuit (I²C) compatible
 - Standard mode (Sm, 100 kHz)
 - Fast mode (Fm, 400 kHz)
 - Fast mode plus (Fm+, 1 MHz)⁽²⁾
 - Event System for CPU independent and predictable inter-peripheral signaling
 - Configurable Custom Logic (CCL) with four programmable Look-up Tables (LUTs)
 - One 10-bit 200 ksps Analog-to-Digital Converter (ADC)
 - One Analog Comparator (AC)
 - Internal 2.048V, 2.500V and 4.096V voltage references, and external reference option (VREF)
- I/O and Packages:
 - Up to 25 (24) programmable GPIO (I/O) pins
 - 32-pin VQFN 5x5 mm and TQFP 7x7 mm
 - 28-pin VQFN 4x4 mm, SPDIP and SSOP
 - 20-pin SOIC
 - 14-pin SOIC
- Temperature Ranges:
 - Industrial: -40°C to +85°C
 - Extended: -40°C to +125°C

Notes:

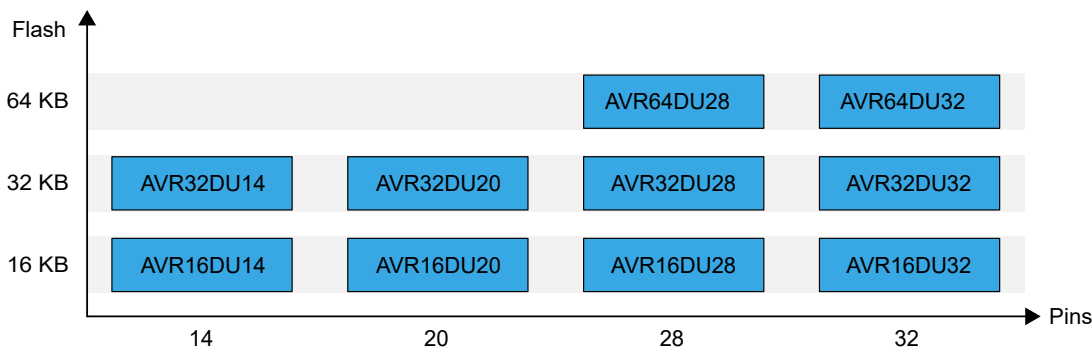
1. USB function is only available for VDD above 3.0V.
2. I²C Fm+ is only supported for 2.7V and above.

AVR® DU Family Overview

The figure below shows the AVR DU devices, laying out pin count variants and memory sizes:

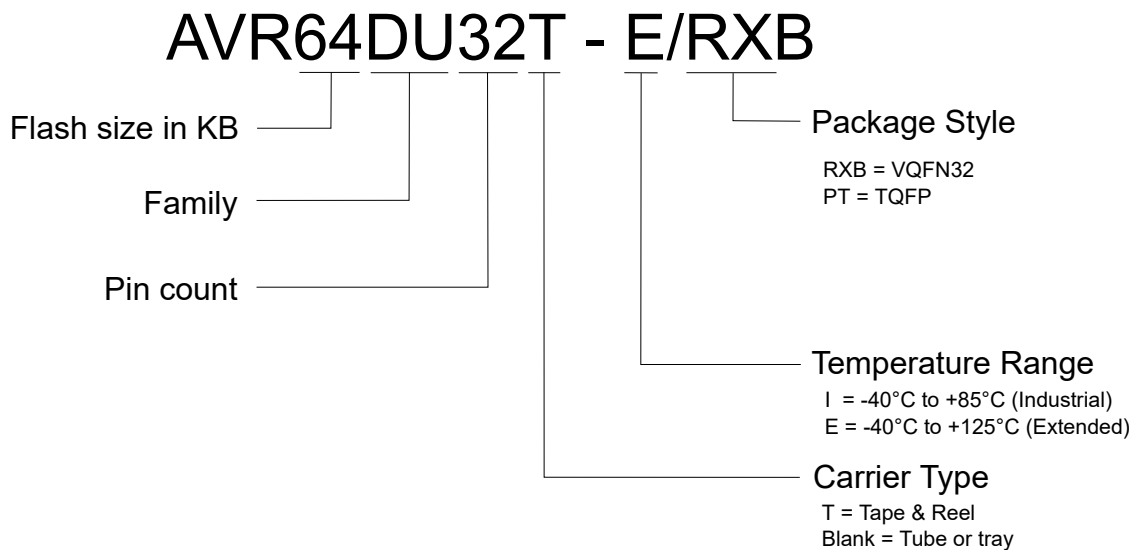
- Vertical migration is possible without code modification, as these devices are fully pin and feature compatible
- Horizontal migration to the left reduces the pin count and, therefore, the available features

Figure 1. AVR® DU Family Overview



The name of a device in the AVR DU Family is decoded as follows:

Figure 2. AVR® DU Device Designations



Memory Overview

The following table shows the memory overview of the entire AVR DU family.

Table 1. Memory Overview

Devices	AVR16DU14 AVR16DU20 AVR16DU28 AVR16DU32	AVR32DU14 AVR32DU20 AVR32DU28 AVR32DU32	AVR64DU28 AVR64DU32
Flash memory	16 KB	32 KB	64 KB

.....continued

Devices	AVR16DU14 AVR16DU20 AVR16DU28 AVR16DU32	AVR32DU14 AVR32DU20 AVR32DU28 AVR32DU32	AVR64DU28 AVR64DU32
SRAM	2 KB	4 KB	8 KB
EEPROM	256B	256B	256B
User row	512B	512B	512B
Boot row	256B	256B	256B

Peripheral Overview

The following table shows the peripheral overview of the entire AVR DU family.

Table 2. Peripheral Overview

Feature	AVR16DU14 AVR32DU14	AVR16DU20 AVR32DU20	AVR16DU28 AVR32DU28 AVR64DU28	AVR16DU32 AVR32DU32 AVR64DU32
Pins	14	20	28	32
Max. frequency (MHz)	24	24	24	24
16-bit Timer/Counter type A (TCA)	1	1	1	1
16-bit Timer/Counter type B (TCB)	2	2	2	2
Real-Time Counter (RTC)	1	1	1	1
USB 2.0 full-speed device	1	1	1	1
USART	2	2	2	2
SPI	1	1	1	1
TWI/I ² C ⁽¹⁾	1 ⁽¹⁾	1 ⁽¹⁾	1 ⁽¹⁾	1 ⁽¹⁾
10-bit ADC (channels)	1 (5)	1 (11)	1 (17)	1 (21)
Analog Comparator (AC)	1	1	1	1
Peripheral Touch Controller (PTC)	-	-	-	-
Operational amplifier (OP)	-	-	-	-
Configurable Custom Logic Look-up Table (CCL LUT)	4	4	4	4
Watchdog Timer (WDT)	1	1	1	1
Event System (EVSYS) channels	6	6	6	6
General Purpose I/O ⁽²⁾	9/8 ⁽²⁾	15/14 ⁽²⁾	21/20 ⁽²⁾	25/24 ⁽²⁾
PORT	PA[1:0], PC[3], PD[7:4], PF[7:6]	PA[7:0], PC[3], PD[7:4], PF[7:6]	PA[7:0], PC[3], PD[7:0], PF[7,6,1,0]	PA[7:0], PC[3], PD[7:0], PF[7:0]
External interrupts	9	15	21	25
CRSCAN	1	1	1	1

.....continued

Feature	AVR16DU14 AVR32DU14	AVR16DU20 AVR32DU20	AVR16DU28 AVR32DU28 AVR64DU28	AVR16DU32 AVR32DU32 AVR64DU32
Pins	14	20	28	32
Unified Program and Debug Interface (UPDI)	1	1	1	1

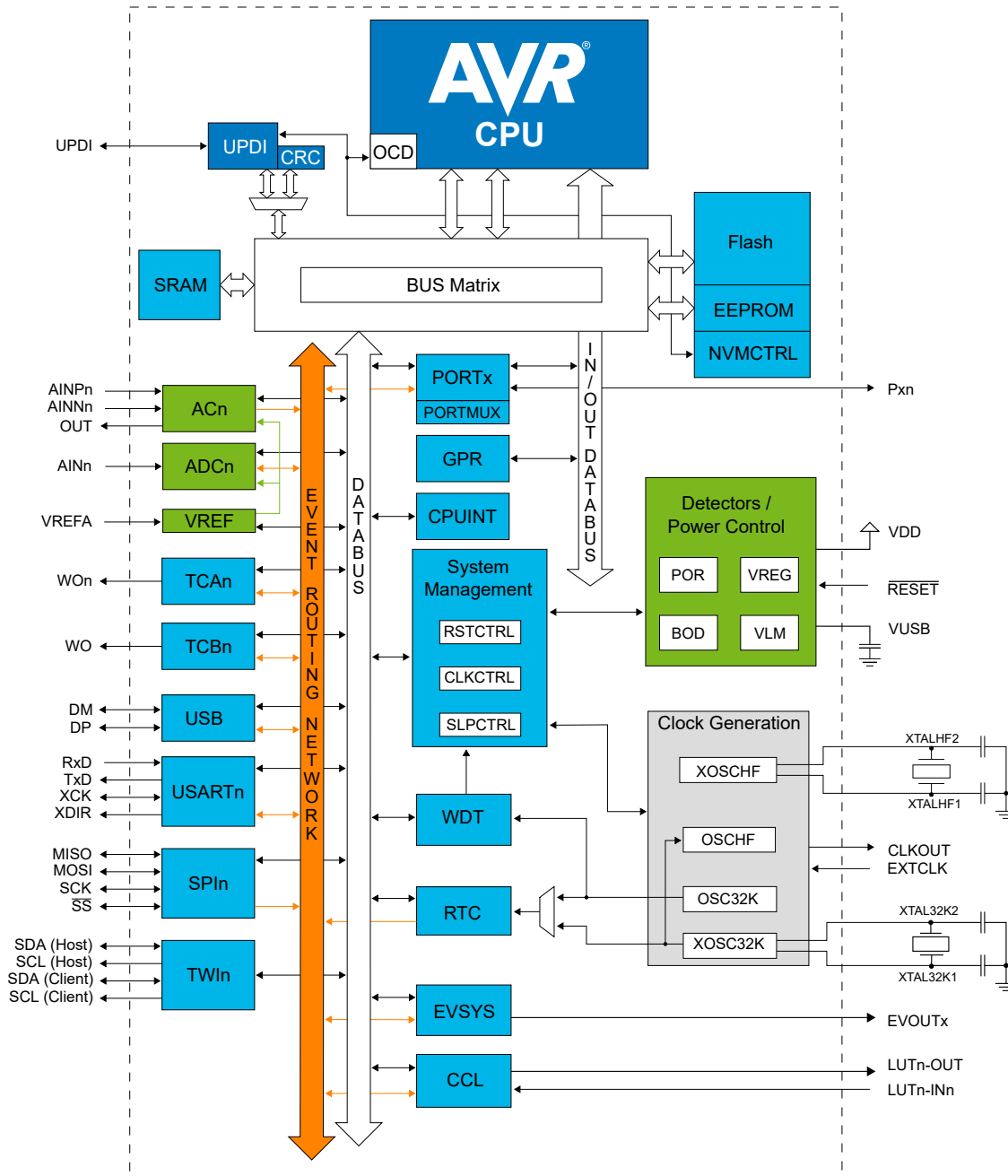
Notes:

1. The TWI/I²C can operate simultaneously as both host and client on different pins.
2. PF6/RESET pin is input only.

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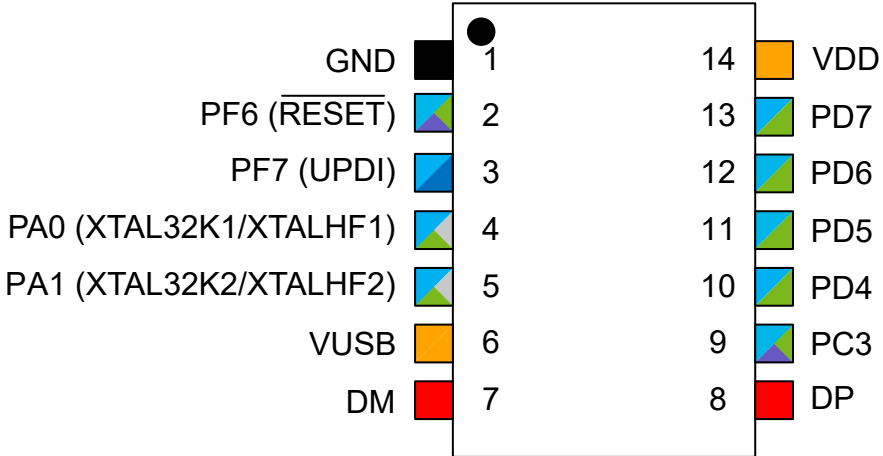
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1. Block Diagram



2. Pinout

2.1 14-Pin SOIC



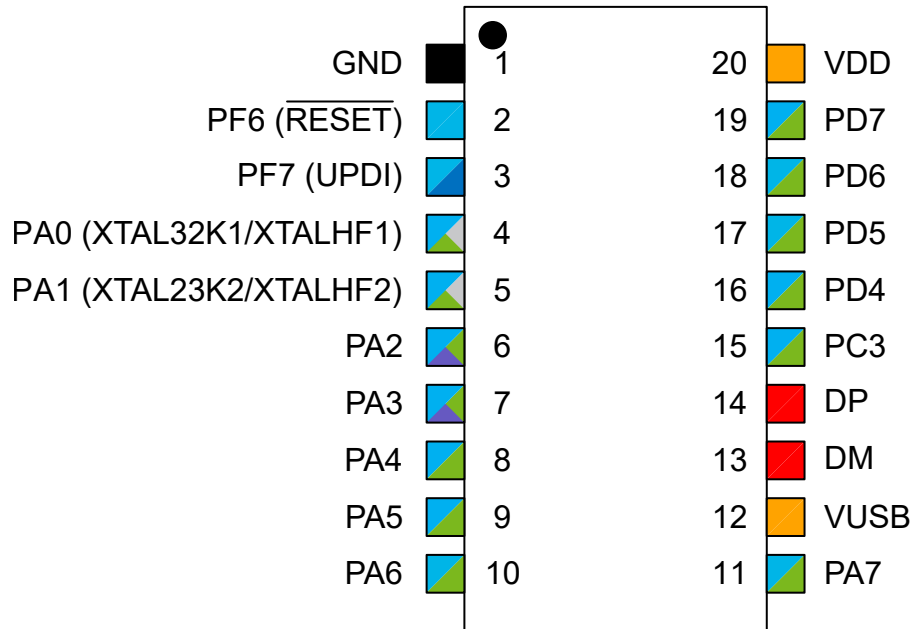
Power

- Input supply
- Ground
- PIN on VDD power domain
- PIN on VUSB power domain





Functionality

- Programming/Debug
- Clock/Crystal
- Digital Function Only
- Analog Function
- TWI
- USB







2.2 20-Pin SOIC



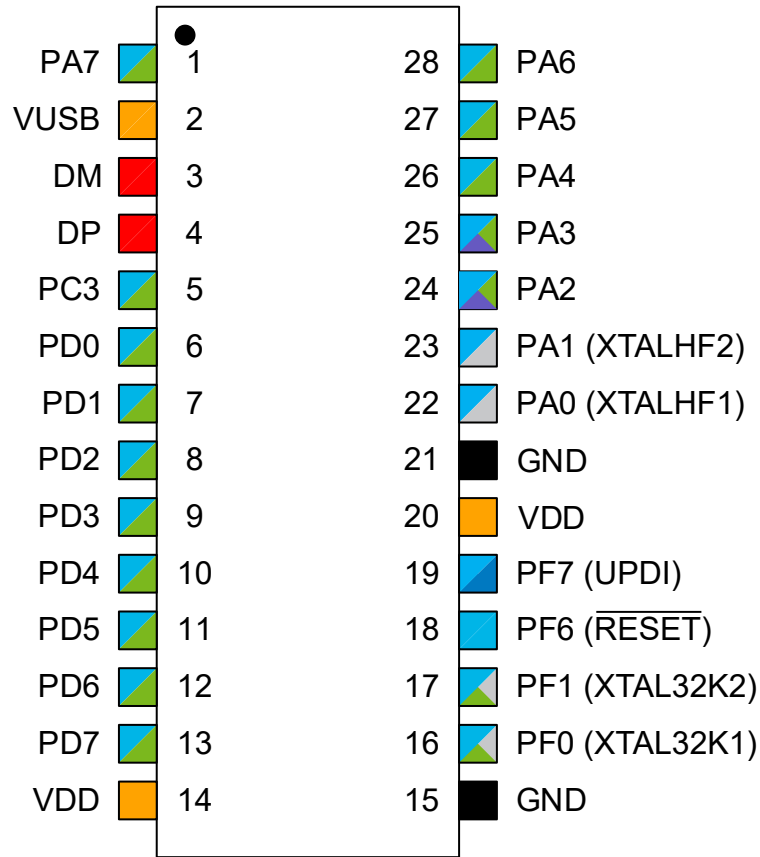
Power

-  Input supply
-  Ground
-  PIN on VDD power domain
-  PIN on VUSB power domain





Functionality

-  Programming/Debug
-  Clock/Crystal
-  Digital Function Only
-  Analog Function
-  TWI
-  USB







2.3 28-Pin SPDIP and SSOP



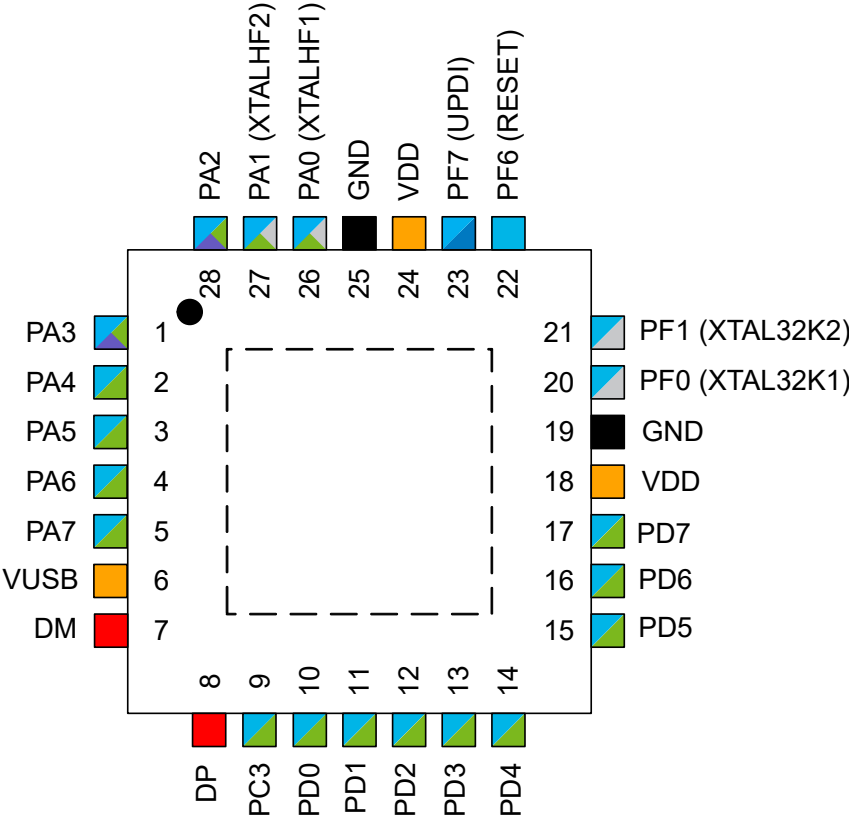
Power

-  Input supply
-  Ground
-  PIN on VDD power domain
-  PIN on VUSB power domain





Functionality

-  Programming/Debug
-  Clock/Crystal
-  Digital Function Only
-  Analog Function
-  TWI
-  USB







2.4 28-Pin VQFN



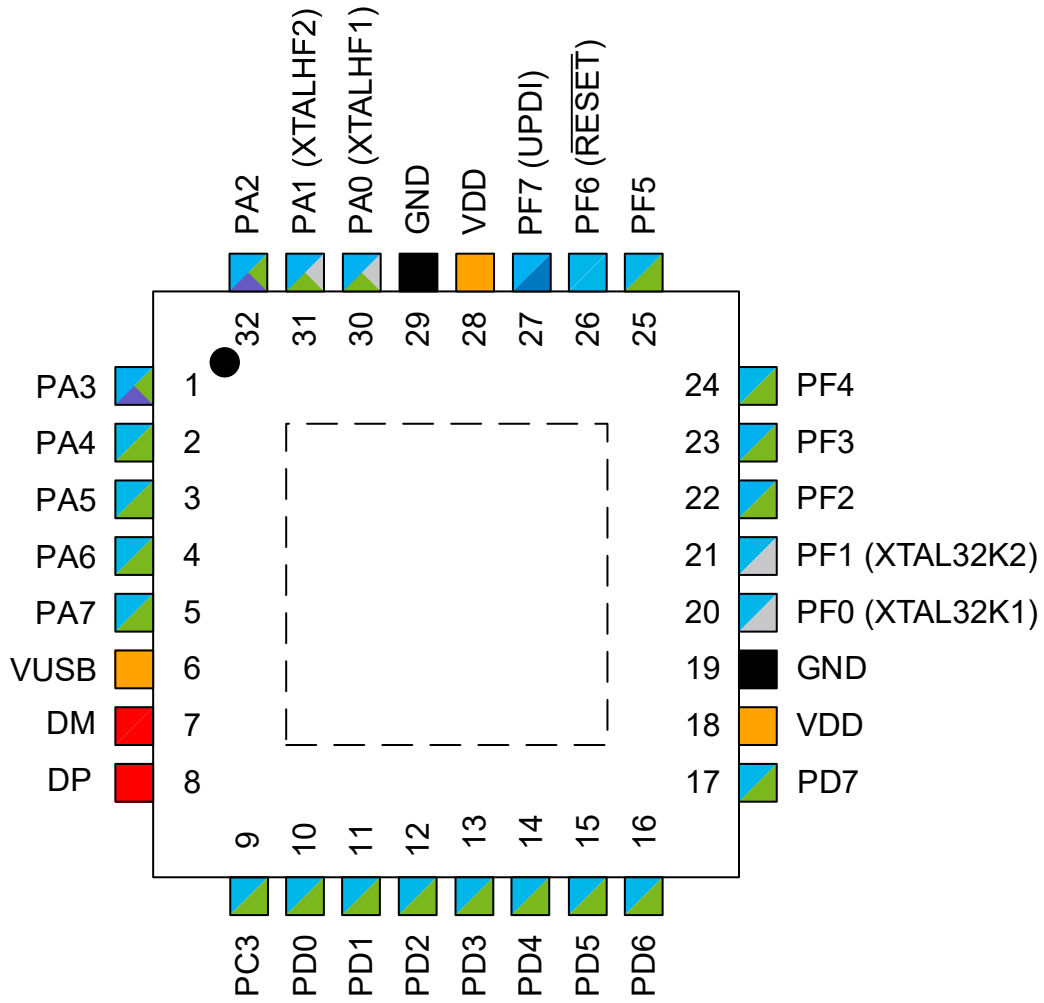
Power

-  Input supply
-  Ground
-  PIN on VDD power domain
-  PIN on VUSB power domain





Functionality

-  Programming/Debug
-  Clock/Crystal
-  Digital Function Only
-  Analog Function
-  TWI
-  USB







2.5 32-Pin TQFP and VQFN



Power

-  Input supply
-  Ground
-  PIN on VDD power domain
-  PIN on VUSB power domain

Functionality

-  Programming/Debug
-  Clock/Crystal
-  Digital Function Only
-  Analog Function
-  TWI
-  USB

3. I/O Multiplexing and Considerations

3.1 I/O Multiplexing

VQFN32 TQFP32	SPDIP28 SSOP28	VQFN28	SOIC20	SOIC14	Pin name (1,2)	Special	ADC0	ACC0	USB	USARTm	SPI0	TWI0(4)	TCA0	TCBn	EVSYS	CCL
30	22	26	4	4	PA0	XTAL32K1(6) XTALHF1 EXTCLK				0,TxD		SDA(HC)(3)	WO0			LUT0,IN0
31	23	27	5	5	PA1	XTAL32K2(6) XTALHF2				0,RxD		SCL(HC)(3)	WO1			LUT0,IN1
32	24	28	6		PA2		AIN22			0,XCK 0,TxD(3)		SDA(HC)	WO2	0,WO	EVOUTA	LUT0,IN2
1	25	1	7		PA3		AIN23			0,XDIR 0,RxD(3)		SCL(HC)	WO3	1,WO		LUT0,OUT
2	26	2	8		PA4		AIN24			0,TxD(3)	MOSI		WO4			
3	27	3	9		PA5		AIN25			0,RxD(3)	MISO		WO5			
4	28	4	10		PA6		AIN26			0,XCK(3)	SCK					LUT0,OUT(3)
5	1	5	11		PA7	CLKOUT	AIN27	OUT		0,XDIR(3)	SS				EVOUTA(3)	
6	2	6	12	6	VUSB				VUSB							
7	3	7	13	7	DM				DM							
8	4	8	14	8	DP				DP							
9	5	9	15	9	PC3		AIN31	AINP4					WO3(3)			LUT1,OUT
10	6	10			PD0		AIN0	AINN1					WO0(3)			LUT2,IN0
11	7	11			PD1		AIN1						WO1(3)			LUT2,IN1
12	8	12			PD2	EVOUTD	AIN2	AINP0					WO2(3)		EVOUTD	LUT2,IN2
13	9	13			PD3		AIN3	AINN0					WO3(3)			LUT2,OUT
14	10	14	16	10	PD4		AIN4			0,TxD(3)	MOSI(3)		WO4(3)	0,WO(3)		
15	11	15	17	11	PD5		AIN5			0,RxD(3)	MISO(3)		WO5(3)	1,WO(3)		
16	12	16	18	12	PD6		AIN6	AINP3		0,XCK(3) 1,TxD(3)	SCK(3)					LUT2,OUT(3)
17	13	17	19	13	PD7	VREFA	AIN7	AINN2		0,XDIR(3) 1,RxD(3)	SS(3)				EVOUTD(3)	
18	14	18	20	14	VDD											
19	15	19	1	1	GND											
20	16	20			PF0	XTAL32K1	AIN16						WO0(3)			LUT3,IN0
21	17	21			PF1	XTAL32K2	AIN17						WO1(3)			LUT3,IN1
22					PF2		AIN18						WO2(3)		EVOUTF	LUT3,IN2
23					PF3		AIN19						WO3(3)			LUT3,OUT
24					PF4		AIN20						WO4(3)	0,WO(3)		
25					PF5		AIN21						WO5(3)	1,WO(3)		
26	18	22	2	2	PF6(5)	RESET										
27	19	23	3	3	PF7	UPDI									EVOUTF(3)	
28	20	24			VDD											
29	21	25			GND											

Notes:

1. The pin names are of Pxn type, with x being the PORT instance (A, B, C, ...) and n, the pin number. The notation for signals is PORTx_PINn. All pins can be used as event input.
2. All pins can be used for external interrupt.
3. Alternate pin positions. For selecting the alternate positions, refer to the *PORTMUX - Port Multiplexer* section.
4. The TWI pins that can be used as host or client are marked *H*. The pins with client-only are marked *C*.
5. Input-only.
6. Only for 14-pin and 20-pin devices.

4. Data Sheet Revision History

Note: The data sheet revision is independent of the die revision and the device variant (last letter of the ordering number).

4.1 Revision History

Doc. Rev.	Date	Description
A	08/2021	Initial document revision

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