Spencer Gass

spencer.gass@gmail.com | 256.541.3116 | LinkedIn: spencer-gass | GitHub: spencer-gass

EXPERIENCE

SENIOR FPGA ENGINEER | Adtran | June 2016 – Present | Huntsville, AL (Remote since 2020)

Current Responsibilities:

- Contributing to the design specification and verification plan for a telecom ASIC.
- Front-end ASIC development: RTL design and Synthesis.
- Creating FPGA designs which implement key features for telecom networking equipment and supporting those designs through their life cycle (design specification, RTL design, simulation, synthesis/implementation, timing closure, on-target testing, and maintenance).
- Designs I am responsible for include: HSPON/XGS-PON/GPON DBA engines, 10G/100G Ethernet traffic generator/analyzer products, Ethernet MAC and SerDes IP, PCIe DMA IP, and 5 FPGA designs which perform SyncE and board management functions on different products.
- Collaborating with product management, engineers, and research staff to facilitate product development.
- Leading the FPGA team's co-op program. Mentoring and supervising 2 co-ops per year. Co-ops start the semester with minimal RTL/FPGA knowledge and leave with a strong grasp of the fundamentals. By the end of the semester they are often able to contribute to a production FPGA design.

Past Accomplishments:

- Inherited ownership of a 100 Gbps Ethernet traffic generator/analyzer and advanced it from minimum viable product to full function by refactoring RTL to close timing, implementing technically difficult features like 100 Gbps packet capture, and deficit waited round robin scheduling, and implementing UI, application, and driver features in Javascript, Python, and C. This is a ubiquitous internal product with over 250 units manufactured, saving the company over $100M .
- Contributed to the development of the 518F1 Adtran's bestselling line card. Approximately 36,000 units sold, generating $250M in revenue as of Q4 2023. Collaborated with a staff researcher to develop 25G Ethernet MAC and SerDes IP. Integrated and verified back plane Ethernet links. Supported a principal engineer in the development of a multi-100G Ethernet switch generating two patent applications.
- Resolved a critical customer issue shortly after inheriting ownership of the relevant IP which I was previously unfamiliar with. Communicated progress to my VP and resolved the issue in time to salvage the relationship with the customer.
- Recognized the limitations of the PCIe DMA engine used for FPGA register access and exception traffic, and proactively created a higher performance, lower resource utilizing replacement. The new design is used in 14 FPGA designs on 8 product lines.
- Independently created and maintained 3 FPGA designs which perform SyncE, and board management functions on Adtran's SDX OLTs and aggregation switches.
- Collaborated with a cross functional team to develop a method for configuring large FPGAs to allow for faster boot times and more reliable FPGA initialization.

ENGINEERING CO-OP | Adtran | May 2013 – Dec 2014 | Huntsville, AL

- Worked for one semester each, three semester total, with DVT, hardware, and FPGA groups.

EDUCATION

Georgia Institute of Technology MS ECE | Aug 2019 | GPA: 3.4 / 4.0
Mississippi State University BS EE | May 2016 | GPA: 3.8 / 4.0

SKILLS

RTL Design: VHDL | Verilog | Modelsim | Questasim | Synthesis | Static Timing Analysis | Clock Domain Crossing
FPGA Design: AMD | Xilinx | Vivado
Programming and Scripting: Python | C++ | C | Javascript | Bash | CSH
Relevant Technologies and Standards: Ethernet | PCIe | AXI | DDR | HBM
Knowledge of: System Verilog | UVM

PATENTS

US 11,588,821 B1 – Systems and Methods for Access Control List (ACL) Filtering – 2/21/2023