Spencer Gass

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EXPERIENCE

FPGA DIGITAL DESIGN ENGINEER | Kepler Communications | May 2024 – Present | Toronto, ON (Remote)
Current Responsibilities:

- Collaborating with network software, product hardware, and product management to integrate the FPGA based MPLS router I designed into Kepler's satellites.
- Subject matter expert on network hardware.

Past Accomplishments:

- Specified and designed an MPLS router with 100+Gbps throughput, and a high level of parametrization in SystemVerilog. The design includes ingress, classification, forwarding, queuing, and egress subsystems. Created a full automated test bench suite for verification.

SENIOR FPGA ENGINEER | Adtran | June 2016 – April 2024 | Huntsville, AL (Remote 2020-2024)
Past Accomplishments:

- Created FPGA designs which implement key features for broadband access networking equipment and supported those designs through their life cycle (design specification, RTL design, simulation, synthesis/implementation, timing closure, on-target testing, and customer support).
- Designs include: HSPON/XGS-PON/GPON DBA engines, 10G/100G Ethernet traffic generators/analyzers, 1G/10G/100G Ethernet MAC and SerDes, PCIe DMA, SyncE and board management.
- Lead the FPGA team's co-op program. Mentored and supervised 7 co-ops over a 2 year period.
- Inherited ownership of a 100 Gbps Ethernet traffic generator/analyzer and advanced it from minimum viable product to full function by refactoring RTL to close timing, implementing technically difficult features like 100 Gbps packet capture, and DWRR scheduling, and implementing UI, application, and driver features in Javascript, Python, and C. This is a ubiquitous internal product with over 250 units manufactured, saving the company 10s of millions of dollars.
- Supported a principal engineer in the development of a multi-100G broadband Ethernet switch generating two awarded patents.
- Resolved a critical customer issue shortly after inheriting ownership of the relevant IP which I was previously unfamiliar with. Communicated progress to my VP and resolved the issue in time to salvage the relationship with the customer.
- Recognized the limitations of the PCIe DMA engine used for FPGA register access and exception traffic, and proactively created a higher performance, lower resource utilizing replacement. The new design is used in 14 FPGA designs on 8 product lines.

ENGINEERING CO-OP | Adtran | May 2013 – Dec 2014 | Huntsville, AL

- Worked for one semester each, three semester total, with DVT, hardware, and FPGA engineering groups.

EDUCATION

Georgia Institute of Technology MS ECE | Aug 2019 | GPA: 3.4 / 4.0
Mississippi State University BS EE | May 2016 | GPA: 3.8 / 4.0

SKILLS

RTL Design: VHDL | Verilog | System Verilog | Modelsim | Questasim | Vunit
FPGA Design: AMD | Xilinx | Vivado | Petalinux | Ultrascale+ | Versal
Programming and Scripting: Python | C++ | C | Javascript | Bash
Relevant Technologies and Standards: Ethernet | PCIe | AXI | DDR | HBM | TCP | MPLS
Remote Collaboration: Microsoft Teams | Git | GitHub | GitLab | Jira | Confluence
Knowledge of: UVM

PATENTS

US 11,588,821 B1 – Systems and Methods for Access Control List (ACL) Filtering – 2023-2-21
US 12,174,748 B1 - Systems and Methods for Translating Memory Addresses – 2024-12-24