

Spencer Gass

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EXPERIENCE

SENIOR FPGA DIGITAL DESIGN ENGINEER

KEPLER COMMUNICATIONS | MAY 2024 – PRESENT | TORONTO, ON (REMOTE)

Current Responsibilities:

- Subject matter expert on network hardware. Giving technical presentations to the R&D organization, and providing guidance to technical leadership to support the creation of next-gen satellite network architecture.
- Collaborating with network software, product hardware, and product management to integrate an FPGA based MPLS router into Kepler's satellites.

Past Accomplishments:

- Lead the development of an IP/MPLS router with 100+Gbps throughput, and a high level of parametrization in SystemVerilog. Utilized Xilinx/AMD Vitis Networking P4 IP to perform classification and forwarding. Designed custom RTL for the other subsystems. Created a full automated test bench suite for verification.

SENIOR FPGA ENGINEER

ADTRAN | JUNE 2016 – APRIL 2024 | HUNTSVILLE, AL (REMOTE 2020-2024)

Past Accomplishments:

- Contributed to the requirements definition, design specification and verification specification for a 7nm ASIC.
- Created FPGA designs which implement key features for broadband access networking equipment and supported those designs through their life cycle (design specification, RTL design, simulation, synthesis/implementation, timing closure, on-target testing, and customer support).
- Designs include: HSPON/XGS-PON/GPON DBA engines, 10G/100G Ethernet traffic generators/analyzers, 1G/10G/100G Ethernet MAC and SerDes, PCIe DMA, SyncE and board management.
- Lead the FPGA team's co-op program. Mentored and supervised 7 co-ops over a 2 year period.
- Inherited ownership of an FPGA based 100 Gbps Ethernet traffic generator/analyzer and advanced it from minimum viable product to full function by refactoring RTL to close timing, implementing missing features in RTL, and implementing UI, application, and driver layers in Javascript, Python, and C.
- Supported a principal engineer in the development of a multi-100G broadband Ethernet switch generating two awarded patents.
- Recognized the limitations of the PCIe DMA engine used for FPGA register access and exception traffic, and proactively created a higher performance, lower resource utilizing replacement. The new design is used in 14 FPGA designs on 8 product lines.

ENGINEERING CO-OP | ADTRAN | MAY 2013 – DEC 2014 | HUNTSVILLE, AL

- Worked for one semester each, three semester total, with DVT, hardware, and FPGA engineering groups.

EDUCATION

Georgia Institute of Technology MS ECE | Aug 2019 | GPA: 3.4 / 4.0

Mississippi State University BS EE | May 2016 | GPA: 3.8 / 4.0

SKILLS

RTL Design: VHDL | Verilog | System Verilog | Modelsim | Questasim | Vunit

FPGA Design: AMD | Xilinx | Vivado | Petalinux | Ultrascale+ | Versal | P4

Programming and Scripting: Python | C++ | C | Javascript | Bash

Relevant Technologies and Standards: Ethernet | PCIe | AXI | DDR | HBM | TCP | MPLS

Remote Collaboration: Microsoft Teams | Git | GitHub | GitLab | Jira | Confluence

Editors and AI Tools: Windsurf | Codeium | ChatGPT | Claude | Vscod | VIM

PATENTS

US 11,588,821 B1 – Systems and Methods for Access Control List (ACL) Filtering – 2023-2-21

US 12,174,748 B1 - Systems and Methods for Translating Memory Addresses – 2024-12-24