# Spencer Gass

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## EXPERIENCE

**SENIOR FPGA DIGITAL DESIGN ENGINEER**
Kepler Communications | May 2024 – Present | Toronto, ON (Remote)

- Led the development of an FPGA based IP/MPLS router with 100+Gbps throughput, targeting an AMD MPSoC.
- Integrated that router design into Kepler's satellites via collaboration with a cross-functional engineering team.
- Subject matter expert on network hardware. Gave technical presentations to the R&D organization, and provided guidance to technical leadership to support the creation of next-gen satellite network architecture.

**SENIOR FPGA ENGINEER**
Adtran | June 2016 – April 2024 | Huntsville, AL (Remote 2020-2024)

- Created FPGA designs which implement key features for broadband access networking equipment and supported those designs through their life cycle (design specification, RTL design, simulation, synthesis/implementation, timing closure, on-target testing, and customer support).
- Designs include: HSPON/XGS-PON/GPON DBA engines, 10G/100G Ethernet traffic generators/analyzers, 1G/10G/100G Ethernet MAC and SerDes, PCIe DMA, SyncE and board management.
- Advanced an FPGA based 100 Gbps Ethernet traffic generator/analyzer from minimum viable product to full function by refactoring RTL to close timing, implementing missing features, and extending UI, application, and driver layers in Javascript, Python, and C. This is a ubiquitous internal product with over 250 units manufactured, saving the company 10s of millions of dollars.
- Developed a multi-100G broadband Ethernet switch in collaboration with a principle engineer, generating two awarded patents. This was a key component of the 518F1, Adtran's bestselling line card. Generating 100s of millions of dollars of revenue.
- Resolved a critical customer issue shortly after inheriting ownership of the relevant IP which I was previously unfamiliar with. Communicated progress to my VP and resolved the issue in time to salvage the relationship with the customer.
- Developed requirements, design specification, and verification specification for a 7nm ASIC.
- Created a higher performance lower resource utilization, PCIe DMA engine used for FPGA register access and exception traffic, The new design is used in 14 FPGA designs on 8 product lines.
- Implemented a dynamic queue memory allocation system for Adtran's Ethernet switch IP.
- Created and maintained 3 FPGA designs which perform SyncE, and board management functions on Adtran's SDX OLTs and aggregation switches.
- Implemented a FPGA configuration method to allow for faster boot times and more reliable FPGA initialization.
- Led the FPGA team's co-op program. Mentored and supervised 7 co-ops over a 2 year period.

**ENGINEERING CO-OP** | Adtran | May 2013 – Dec 2014 | Huntsville, AL

- Worked for one semester each, three semester total, with DVT, hardware, and FPGA engineering groups.

## EDUCATION

**Georgia Institute of Technology** MS ECE | 2019
**Mississippi State University** BS EE | 2016

## SKILLS

**RTL Design:** System Verilog | Verilog | VHDL | ModelSim | QuestaSim | Vunit
**FPGA Design:** AMD | Xilinx | Vivado | Petalinux | Ultrascale+ | Versal | P4
**Programming and Scripting:** Python | C++ | C | Javascript | Bash
**Relevant Technologies and Standards:** Ethernet | PCIe | AXI | DDR | HBM | TCP | MPLS

## PATENTS

US 11,588,821 B1 – Systems and Methods for Access Control List (ACL) Filtering – 2023-2-21
US 12,174,748 B1 - Systems and Methods for Translating Memory Addresses – 2024-12-24