**Spencer Gass**

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**Experience**

**Senior FPGA Engineer – Adtran – Huntsville AL – 6/06/2016-Current**

- Advanced a 100 Gbps Ethernet traffic generator/analyzer from minimum viable product to full function by refactoring RTL to close timing, implementing technically difficult features like 100 Gbps packet capture, and deficit waited round robbing scheduling, and implementing UI, application, and driver features in Javascript, Python, and C. This is a ubiquitous internal product with over 250 units manufactured, saving the company approximately 100 million dollars.

- Contributed to the development of the 518F1 Adtran’s best selling line card. Approximately 36,000 units sold, generating 250 million dollars in revenue as of Q4 2023.

Collaborated with a staff researcher to develop 25G Ethernet MAC and SerDes IP.

Integrated and verified back plane Ethernet links.

Supported a principal engineer in the development of a multi-100G Ethernet switch generating two patent applications.

- Recognized the limitations of the PCIe DMA engine used for FPGA register access and exception traffic, and proactively created a higher performance, lower resource utilizing replacement. The new design is used in 14 FPGA designs on 8 product lines.

- Independently created and maintained three FPGA designs which perform SyncE, and board management functions on Adtrans SDX OLTs and aggregation switches.

- Resolved a critical customer issue shortly after the relevant subject matter expert left the company. Communicated progress to my VP and resolved the issue in time to salvage the relationship with the customer.

- Created an FPGA based workaround for a rev A clock generator silicon bug which allowed us to ship hardware while waiting for rev B silicon.

- Collaborated with a cross functional team to develop a method for configuring large FPGAs to allow for faster boot times and more reliable FPGA initialization.

- Maintained and extended Adtran’s Ethernet MAC and SerDes IP. Used by nearly all FPGAs in Adtran’s product portfolio.

- Implemented a dynamic queue memory allocation system for Adtran’s Ethernet switch IP so that, rather than assigning fixed memory sizes to queues, queues could increase in size in proportion to free memory before becoming full and discarding incoming packets.

- Integrated a UART 16550 controller into and FPGA to communicate with an off the shelf Ethernet switch chip on the same board. Wrote a driver to create a command line interface that communicates with the switch chip via the FPGA UART. This allowed for in-field debug of the switch chip.

- Designed a high performance packet FIFO to overcome performance limitations with older

generations of packet FIFO and developed automated test coverage beyond what was expected.

- Implemented receive signal strength indicator (RSSI) on Adtran’s 10G EPON OLT.

- Remote since 2020. Thrives in a remote environment evidenced by outstanding performance reviews prior to and while working remotely.

**Engineering Co-op – Adtran – Huntsville AL – 5/15/2013-12/11/2015**

- Worked for one semester each, three semester total, with DVT, hardware, and FPGA groups while in undergrad.

**Undergraduate Researcher for Autonomous Vehicles Project August 2015 - December 2015**

**Education**

Batchelor of Science in Electrical engineering – Mississippi State University May 2016 3.9/4.0 – Summa cum Laude

Master of Science in Electrical and Computer engineering – Georgia Institute of Technology August 2019 3.5/4.0

**Leadership / Mentorship**

Interviewed 26 co-op/interns from 2016 to 2019.

Supervised/Mentored 7 co-ops.

**Patents**

US 11,588,821 B1 – Systems and Methods for Access Control List (ACL) Filtering – 2/21/2023

A Generalized DRAM Arbitration Technique for Optimizing DRAM Bandwidth – Pending

**Skills**

RTL Design: VHDL, Verilog, Modelsim, Questasim, Riviera Pro

FPGA Design: Xilinx, Vivado,

Programming and Scripting: Python, C++, C, Javascript, Bash, CSH

Relevant Technologies and Standards: Ethernet, PCIe, DDR, HBM

Remote Collaboration: Microsoft Teams, Git

Knowledge of: System Verilog, UVM, Perl