LNMIIT
The LNM Institute of
Information Technology

The LNM Institute of Information Technology
Department: Computer Science & Engineering
Computer Organization and Architecture (CSE216)
Exam Type: Mid Term

Time: 90 Minutes   Date: 27-Sep-2019   Max. Marks: 40

Instruction: 1. *There are seven questions. All are compulsory.*
2. *Start each question on a new page and answer them in sequence.*
3. *Be precise while writing your answer.*

Q1. Consider a program segment below: [1+1+2+2=6]

Labels	Instruction Counter	Instruction/Data
	100	Load X
	101	MOV R1
	102	Load Y
	103	Add R1
	104	Store Z
	105	Halt
X:	106	23H
Y:	107	E9H
Z:	108	0000

a) Draw the symbol table.
b) What is the addressing mode used in instruction "Load X"
c) If PC-relative addressing was to be used in place of "X", what would be the offset?
d) What value is stored at Z?

Q2. You are on the design team for a new processor. The clock of the processor runs at 200 MHz. The following table gives instruction count and number of cycles the instructions take for the different classes of instructions for a benchmark program. For this problem, we assume that the processor only executes one instruction at a time.   [6]

Instruction type	Count	Cycles
Load/Store	30	6
Arithmetic	50	4
Others	20	3

a) What is the MIPS processor speed for the benchmark?
b) The compiler expert says that if you double the number of registers, then the compiler will generate code that requires only half the number of Loads & Stores. What will be the CPI?

Q3. In the following expression, what is the state of any two PSW bits (which are being affected by the operation). Assume that machine is of 8-bits. [4]

$$1010\ 1101 + 1110\ 1111$$

Q4. Consider the following expression:

$$X = A + (B * ((C + (D * E))/ F))$$

a) Write a program to compute the value of this expression for the following machines with only the specified instructions available: [3+3=6]

Machine 1: Push M, Pop M, Add, Sub, Mul, Div

Machine 2: Load M, Store M, Add M, Sub M, Mul M, Div M

Here, M is a 16-bit memory address. The opcode is of 8-bits and instruction length is multiple of 4 bits.

b) How many bits does each machine need to compute X? [2]

Q5. Explain briefly: [2*2=4]

a) One morning, the queen bee of a beehive calls all her worker bees and tells them that today's assignment is to collect marigold nectar. The workers then fly off in different directions looking for marigold. Should it be treated as SIMD or MIMD system? Explain.

b) A computation is highly sequential (i.e. each step depends on the preceding step). Would an array processor or a pipeline processor be more appropriate for this? Explain.

Q6. Copute the following expression using IEEE-754 single-precision floating point format [6]

$$-6.5_{10} + 11.25_{10}$$

Q7. Write the micro-sequence for the instruction "**Branch_if_S=0, M**" for a three-bus organization, where **M** is a memory address available in register R5 and S is the sign flag. [6]