Projektiranje programabilnih SoC platformi

Predavanje I - FER, 2022.

Projektiranje programabilnih SoC platformi

- Cilj ovog predmeta je da se upoznate sa postupkom projektiranja SoC sklopa:

  - nije naučna fantastika

  - svakom je dostupno

  - za izvedbu osnovnog dizajn nije potrebno preveliko predznanje

  - specifična prilagodba iziskuje poznavanje HDL jezika i arhitekture sklopova

Predavanja

- Uvod u programabilne sklopove

- Xilinx ZYNQ FPGA

- Podsjetnik na VHDL

- AXI sabirnica (AXI strema, AXI Lite)

- Jednostavan primjer SoC korištenjem Xilinx alata

- Video senzor i kako ga koristiti

- Spajanje video senzora u naš SoC sustav

- Vrijeme za izradu vaših radova

- Prezentacija vaših radova
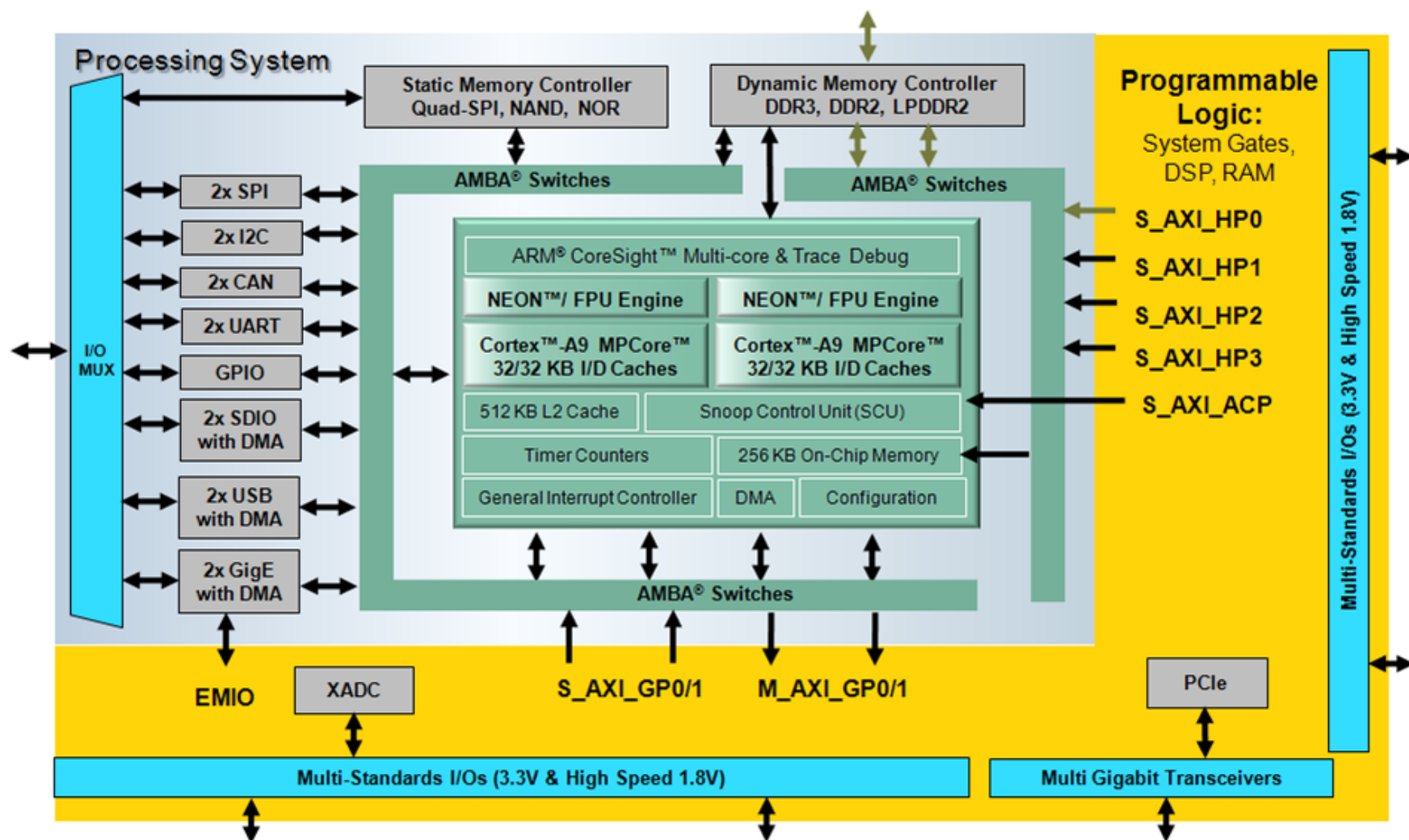
Naš sustav

- Xilinx Zynq SoC FPGA
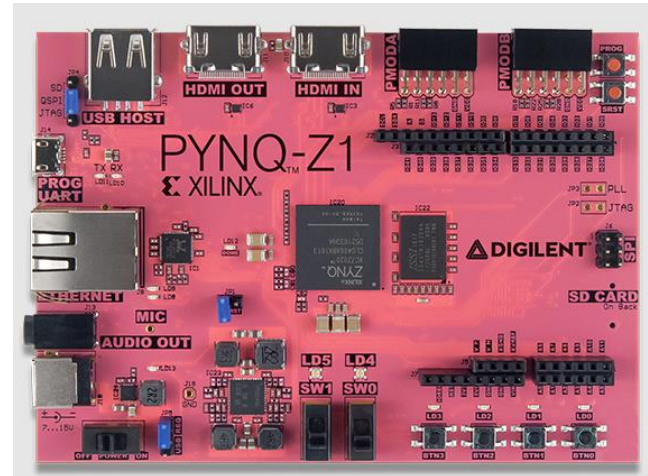
- OmniVision OV7670 senzor

Naš sustav
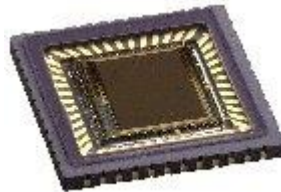
- Zynq SoC FPGA:
  - ZedBoard - Zynq™-7000 SoC XC7Z020
  - PYNQ-Z1 Bord - Zynq™-7000 SoC XC7Z020

- Digitalni video senzor OmniVision OV7670
  - Serial Camera Control Bus (SCCD) – "I2C"
  - Zoom Video Port – Digital video port
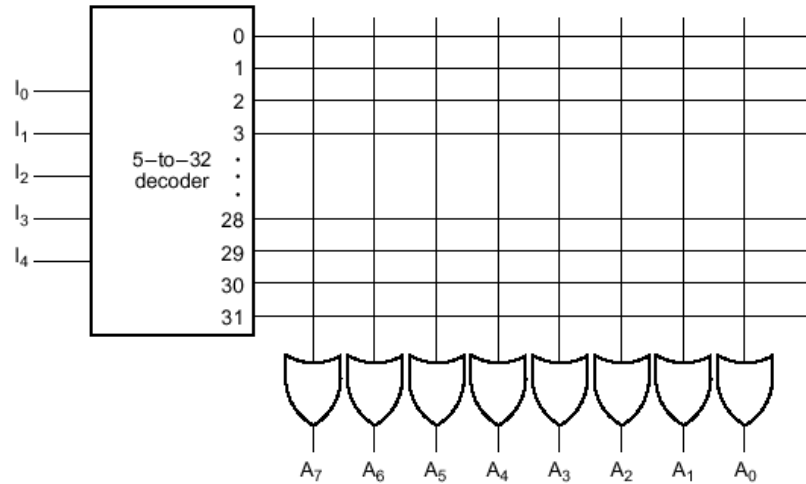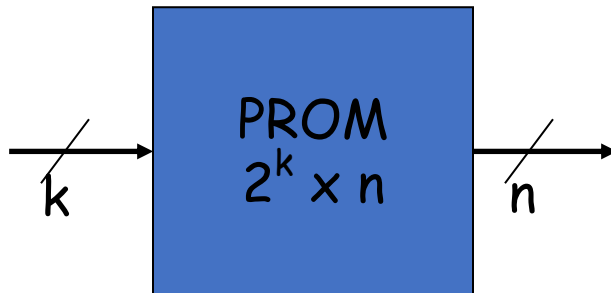
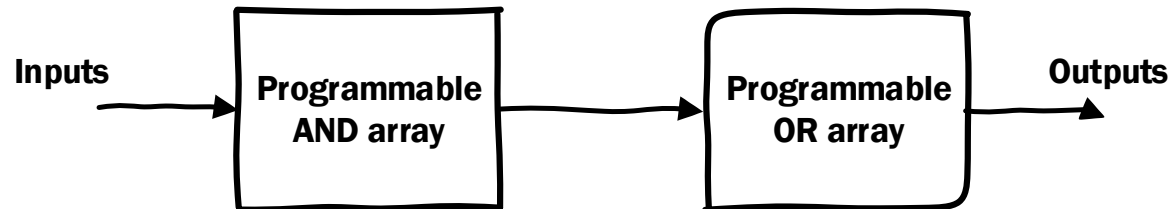# Što je Zynq 7000

Programabilni sklopovi ukratko

- PROM (Programmable ROM)

- PLA (Programmable Logic Array)

- PAL (Programmable Array Logic)

- GAL (Generic Array Logic)

- CPLD (Complex Programmable Logic Device

- FPGA (Field Programmable Gate Array)

Programabilni sklopovi

- PROM (56)

- PLD (početak 70)

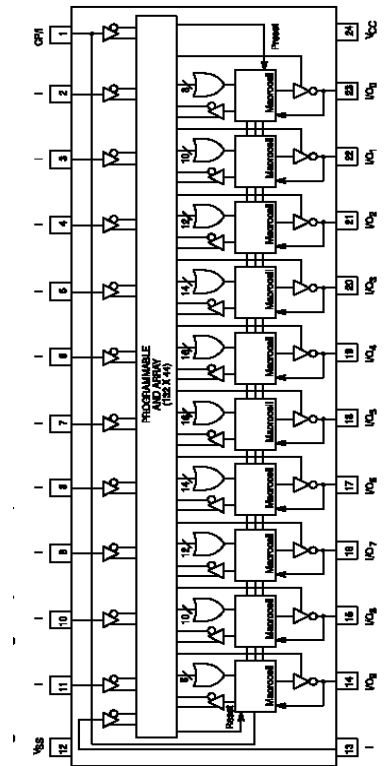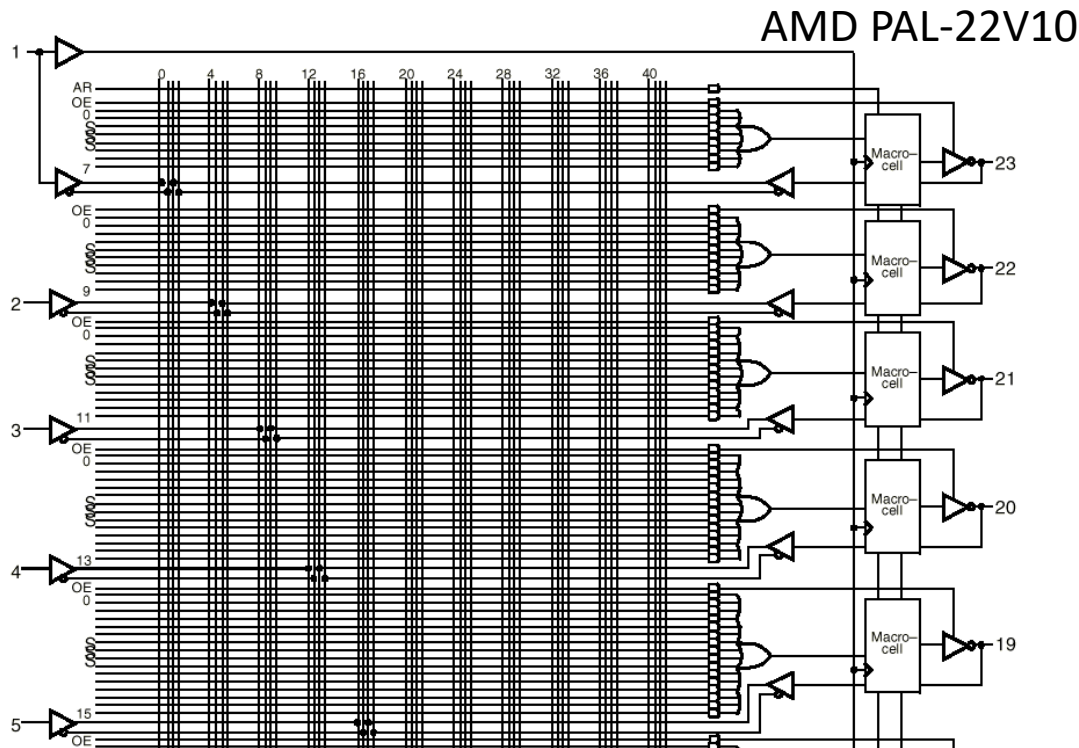# Programabilni sklopovi

- PAL (Monolithic Memories (MMI) 1978)

AMD PAL-22V10
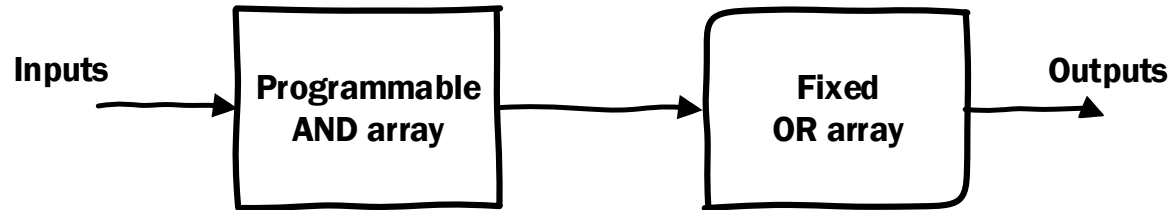
Programabilni sklopovi

- PAL -MACROCELL
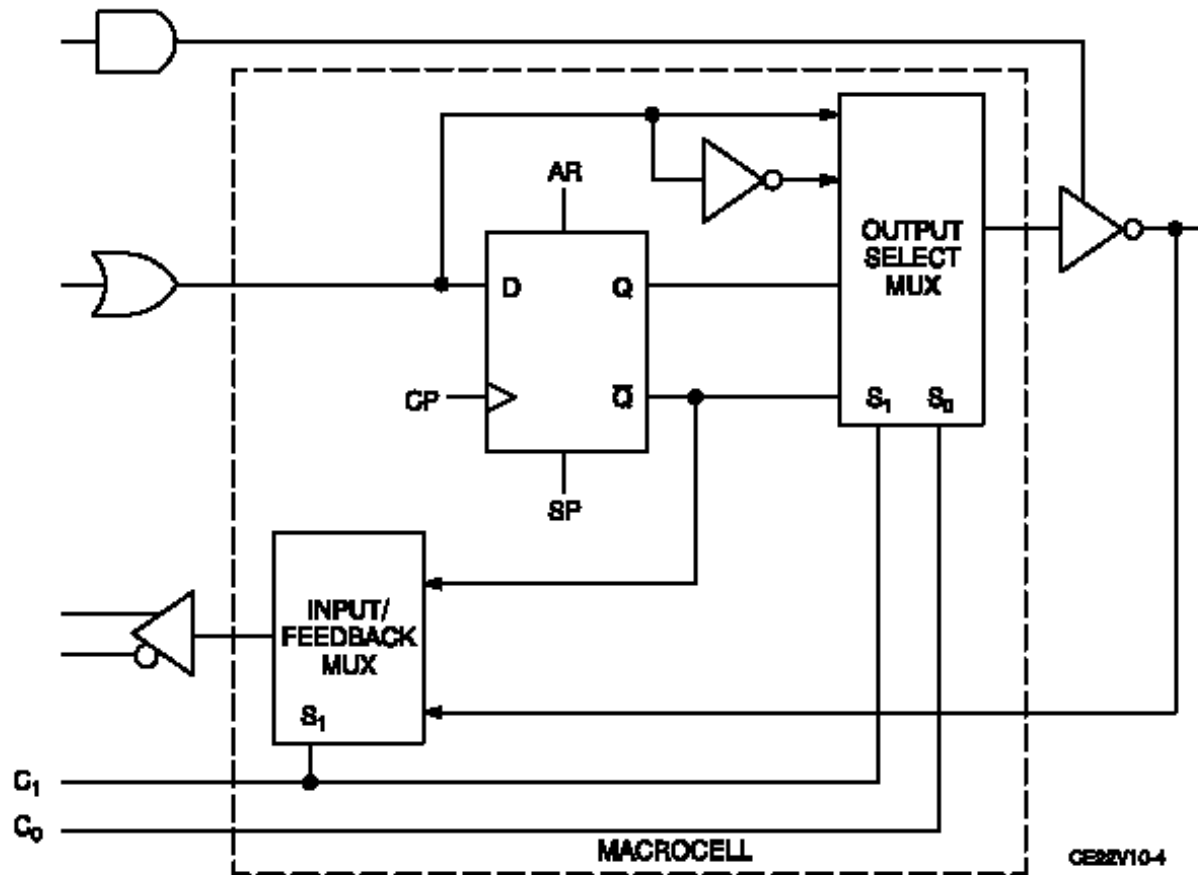
Programabilni sklopovi

- GAL
  - Ista konfiguracija kao i PAL sklopovi
  - Velika prednost mogućnost višestrukog programiranja
  - Podrška za: in-circuit programming
  - PEEL (programmable electrically erasable logic) – International CMOS Technology (ICT) corporation

Programabilni sklopovi

- CPLD
  - Complex Programmable Logic Array
  - Altera proizvela prvi CPLD
  - Usporedbe - 50 SPLD u to doba stalo je u jedan CPLD
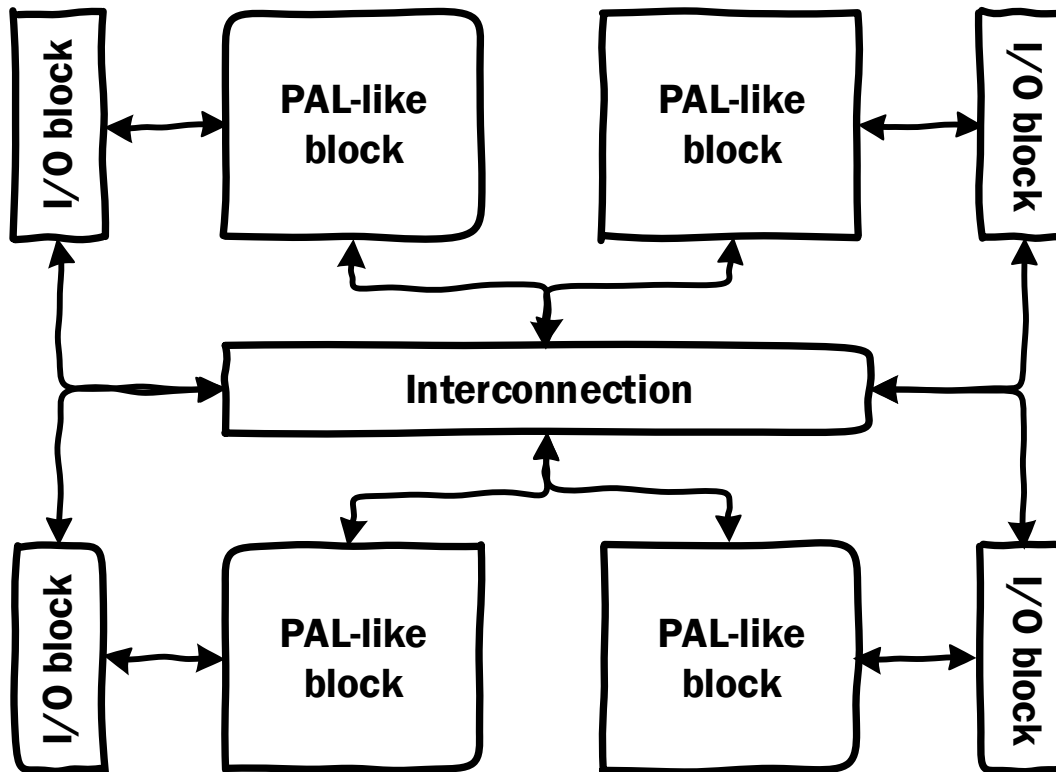
- FPGA
  - FPGA – Filed Programmable Gate Array
  - Sastoje se od blokova koji se nazivaju "Logic Block" i poveznica koji služe za interkonekciju između blokova
  - Konačna funkcija sklopa određuje se naknadnim programiranjem.
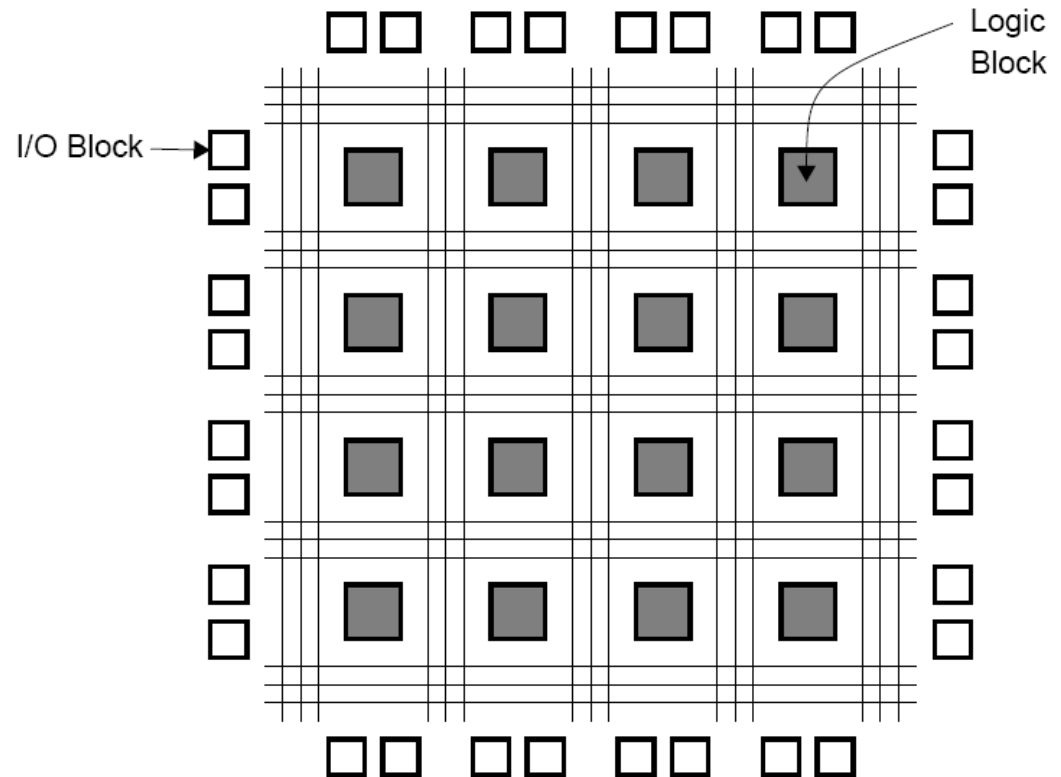
Programabilni sklopovi

- Usporedba tehnologija:

CPLD – 120.000   FPGA > 10.000.000

Equivalent Gates

20000

40000 ***

12000 **

5000 *

2000

1000

200

Legend

***   Altera FLEX 10000, AT&T ORCA 2

**   Altera MAX 9000

*   Altera MAX 7000, AMD Mach, Lattice (p)LSI, Cypress FLASH370, Xilinx XC9500

SPLDs   CPLDs   FPGAs
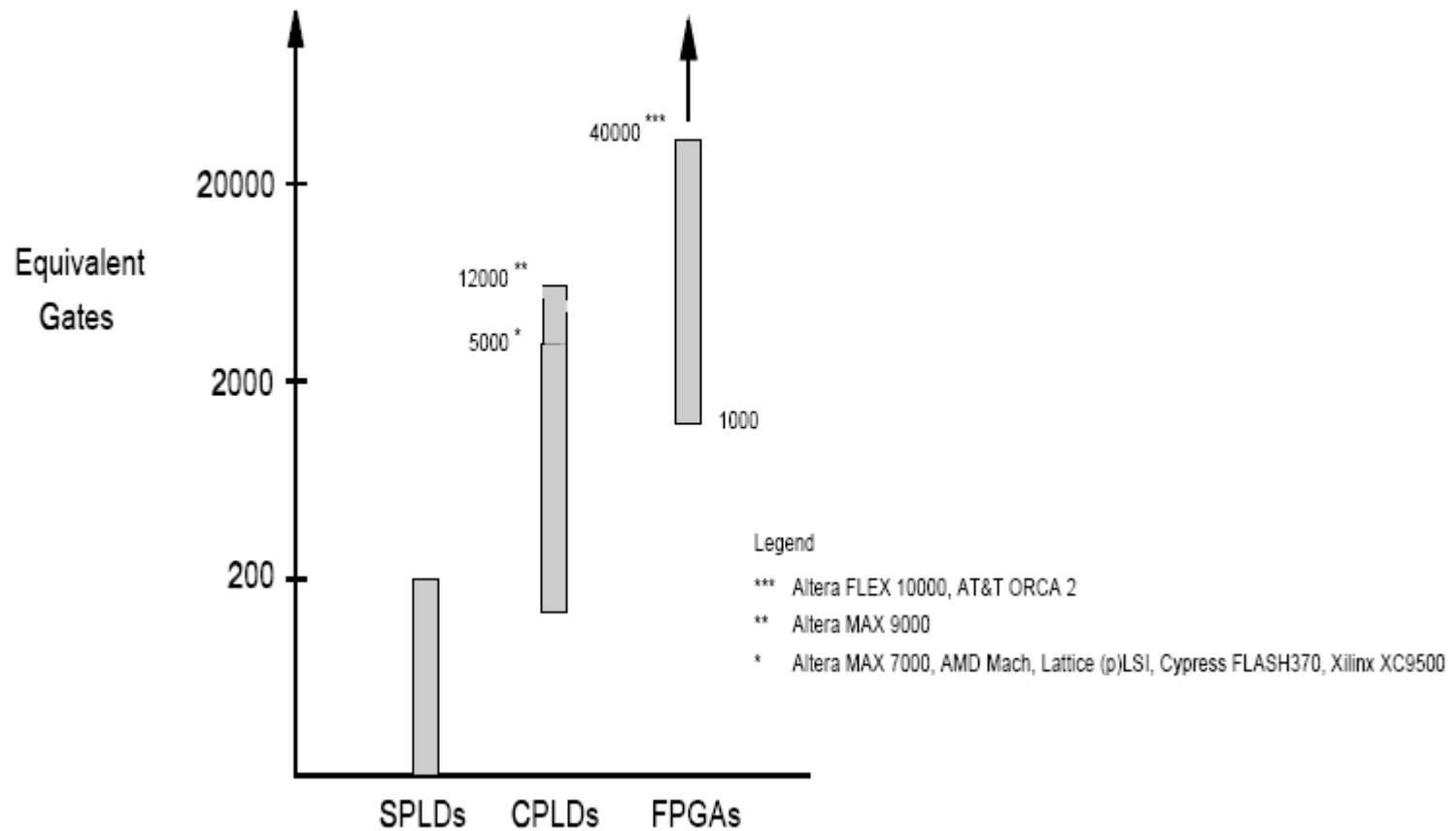
Programabilni sklopovi:

- FPGA sklopovi:
  - CLB (configurable Logic Blocks)
  - Ulazno izlazni blokovi (IO Blocks)
  - Memorijski Blokovi
  - DSP Blokovi
  - Blokovi za digitalnu kontrolu
    perioda signala vremenskog vođenja
    Digital Clock Manager - DCM

DCM   IOB

IOB
IOB   CLB   CLB   CLB   IOB
IOB

CLB   RAM blokovi   Množila
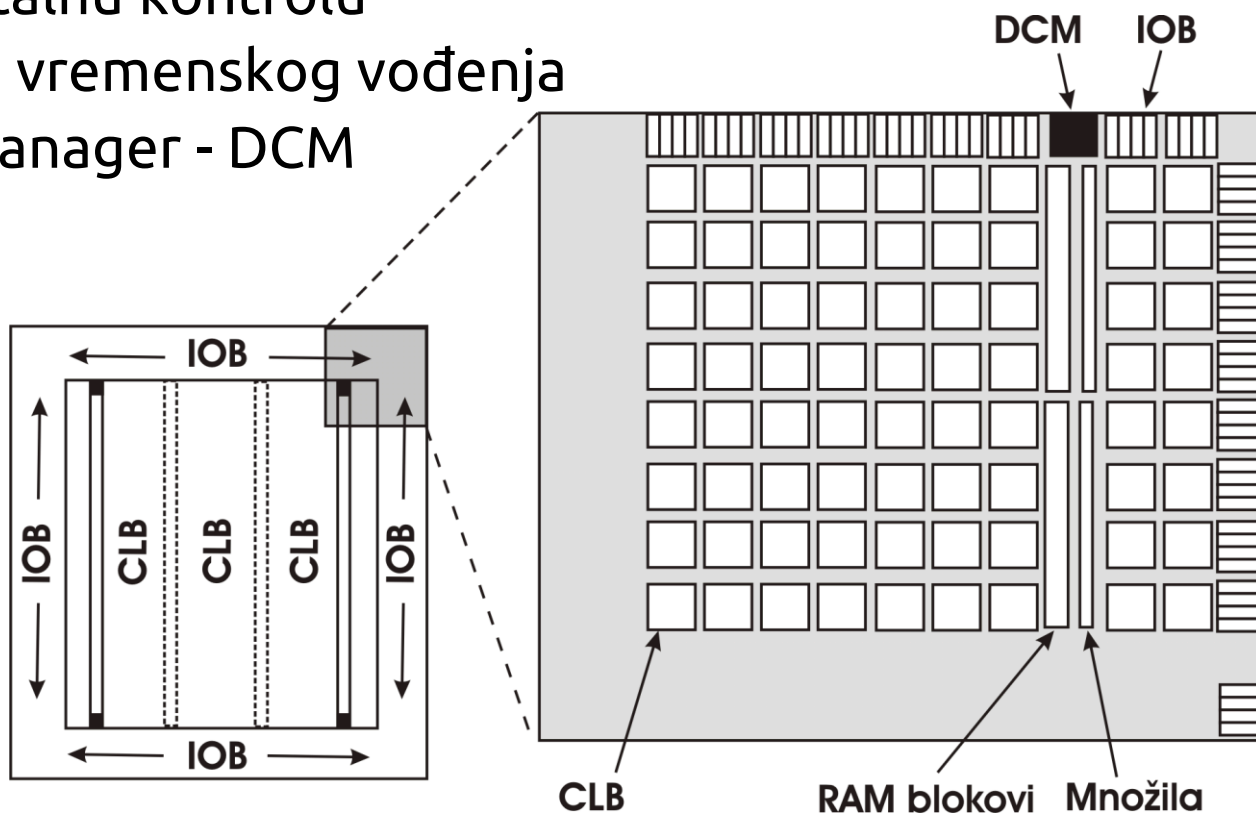
FPGA

- UI Blokovi
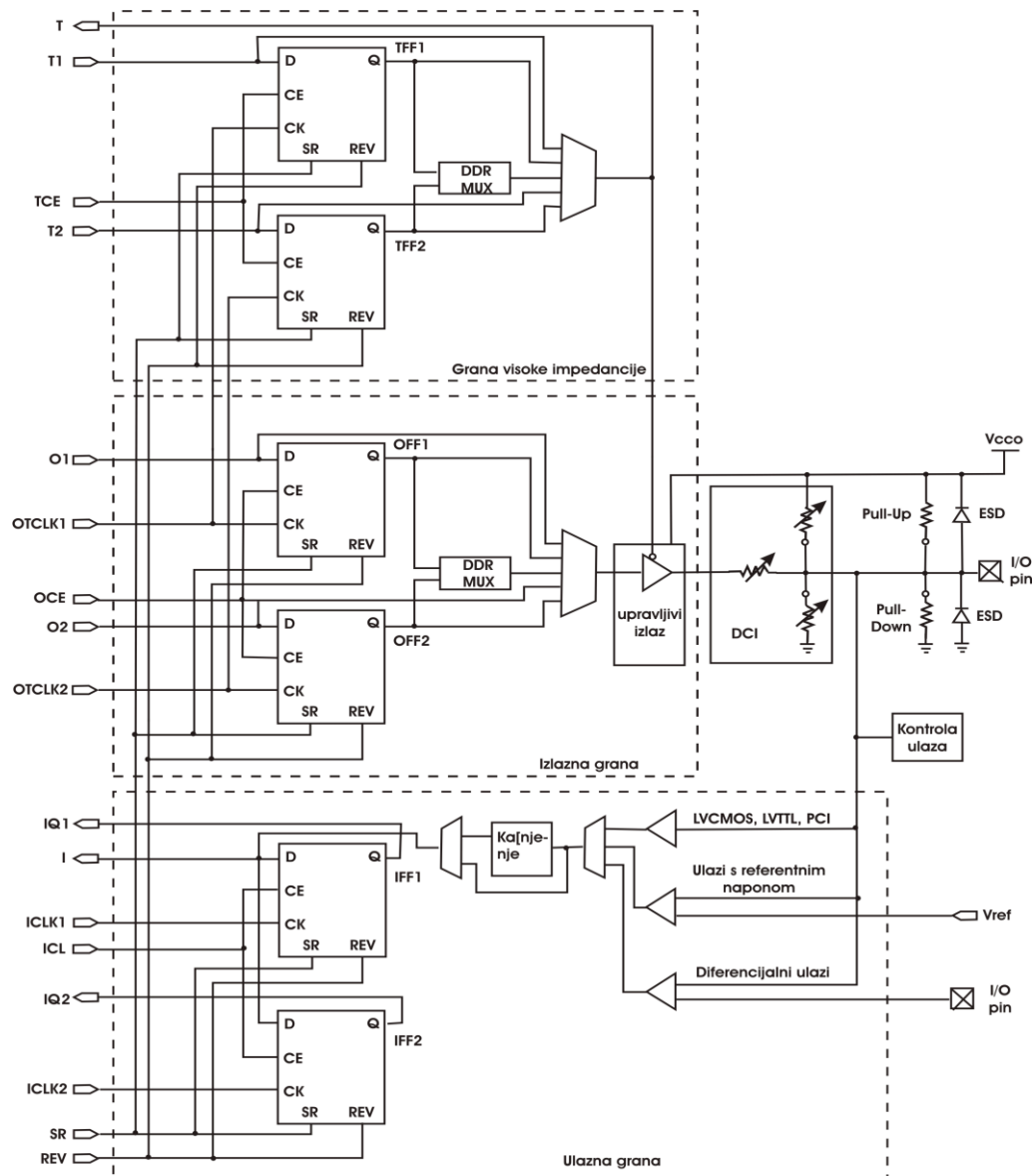
FPGA

- CLB

Programabilni sklopovi
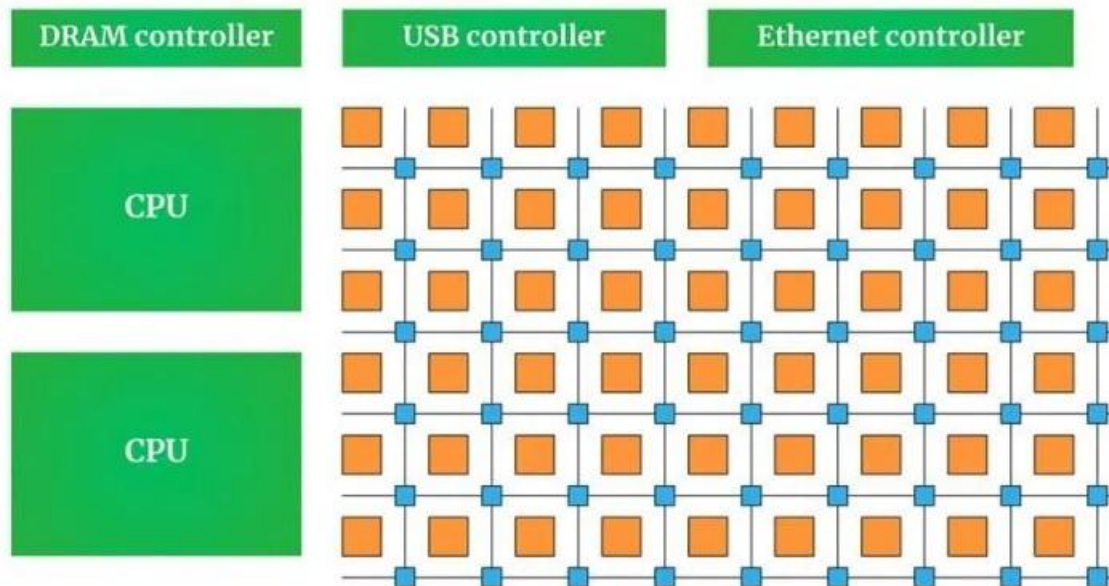
- Današnji trendovi u programabilnim sklopovima

Programabilni sklopovi

• Današnji trendovi u programabilnim sklopovima
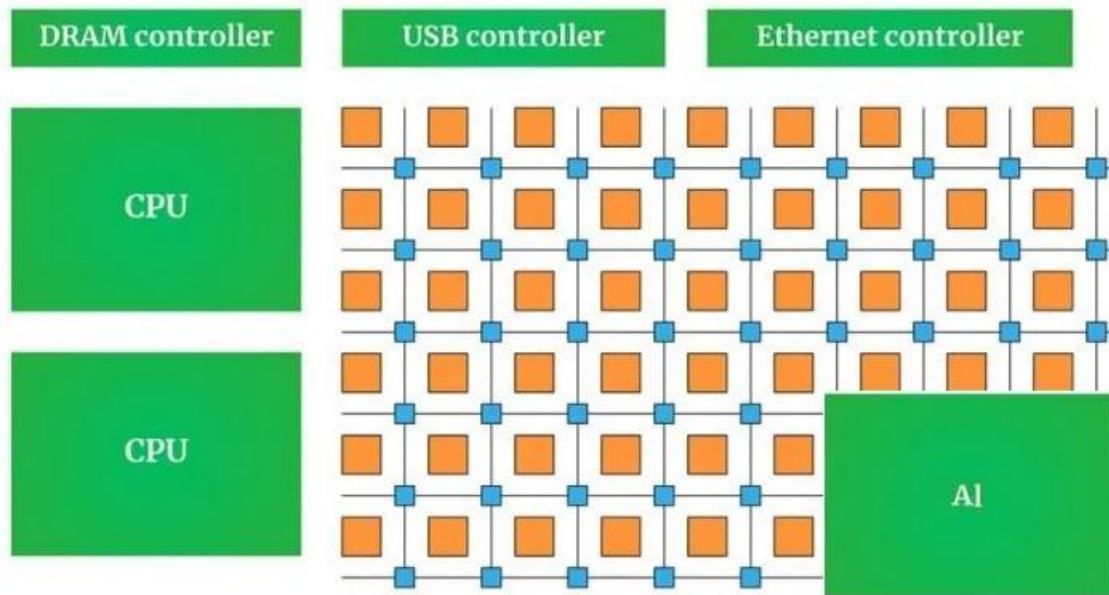
Programabilni sklopovi

- Najveći igrači danas
  - Intel
  - AMD

- Vojko V. bi pjevako „Kako to"

- Ja bi rekao: „zar i to."

- Intel and Altera announced on June 1, 2015, that they had entered into a definitive agreement under which Intel would acquire Altera at approximately $16.7 billion. The transaction closed December 28, 2015.

- AMD said it has completed its $49 billion acquisition of Xilinx to create the "industry's high-performance and adaptive computing leader," marking the largest chip deal in history. (FEBRUARY 14, 2022)

- Lattice Acquires Mirametrix
  - Expands Software Portfolio with Complementary AI and Computer Vision Capabilities

Programabilni sklopovi

- **DynaChip** FPGA knowhow $\xrightarrow{1999}$ **XILINX**

- **GATEFIELD** proASIC-FPGAs $\xrightarrow{1999}$ **ACTEL** proASIC-FPGAs

- **AT&T** ORCA-FPGAs $\xrightarrow{1996}$ **Lucent Technologies** $\xrightarrow{2000}$ **agere** $\xrightarrow{2002}$ **Lattice** ORCA-FPGAs

- **intel** FLEXlogic CPLDs $\xrightarrow{1995}$ **ALTERA** FLASHlogic CPLDs

- **PLUSLOGIC** Hiper EPLDs $\xrightarrow{1992}$ **XILINX** EPLDs XC7200

- **Algotronix** CAL Technology $\xrightarrow{1993}$ **XILINX** FPGAs XC6200

- **PHILIPS** Coolrunner CPLDs/Technology $\xrightarrow{1999}$ **XILINX** Coolrunner CPLDs

- **Concurrent Logic** CL6000-FPGAs $\xrightarrow{1993}$ **ATMEL** AT6000-FPGAs

- **Monolithic Memories** $\xrightarrow{1987}$ **AMD**

- **VANTIS** the PLD division of **AMD** (MACH-CPLDs) $\xrightarrow{1999}$ **Lattice** MACH-CPLDs

- **ALTERA** MAX5000 CPLDs $\xrightarrow{1999}$ **CYPRESS** MAX340/B CPLDs

- **PILKINGTON** MPA-FPGAs $\xrightarrow{1995}$ **Motorola** MPA-FPGAs

SoC

- System On Chip:

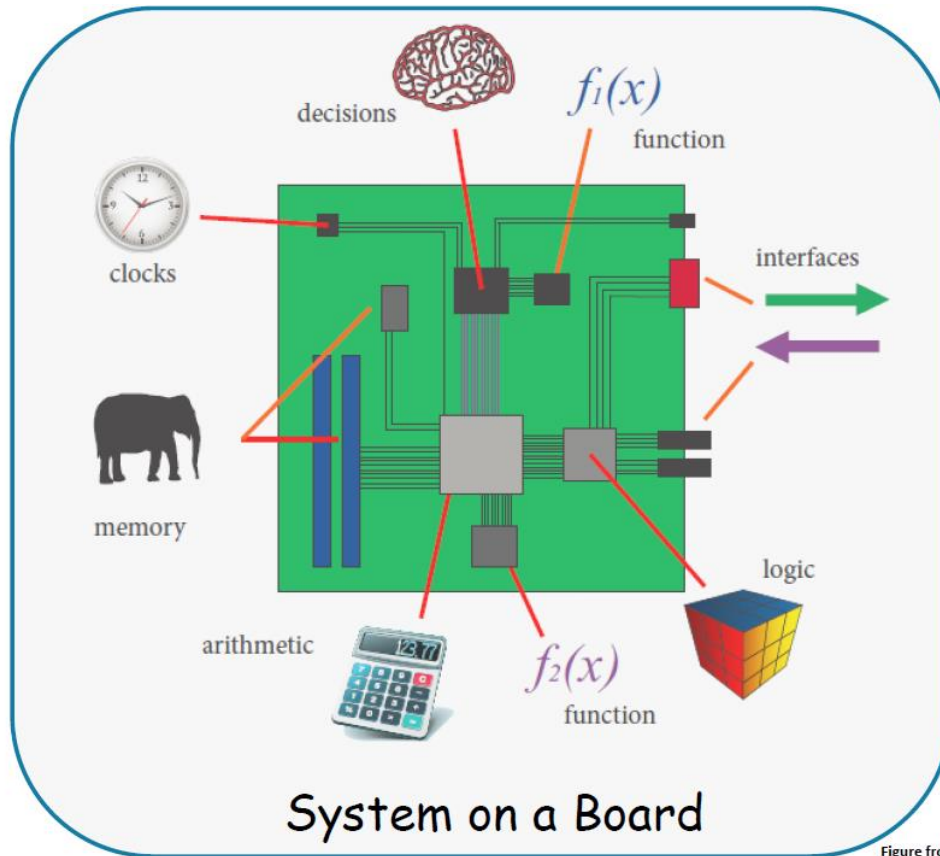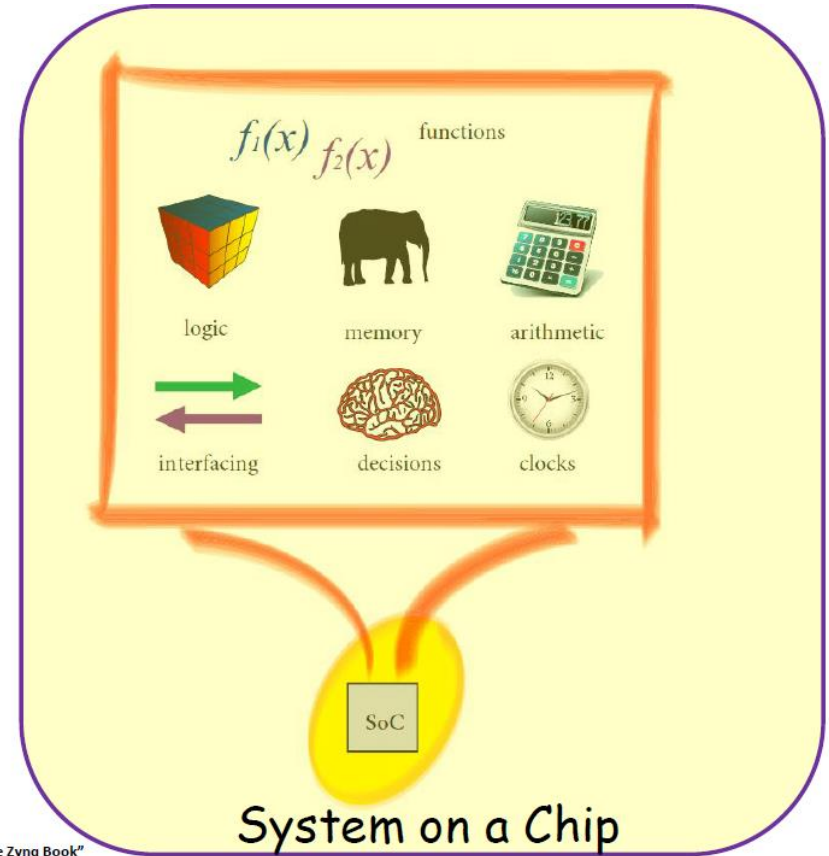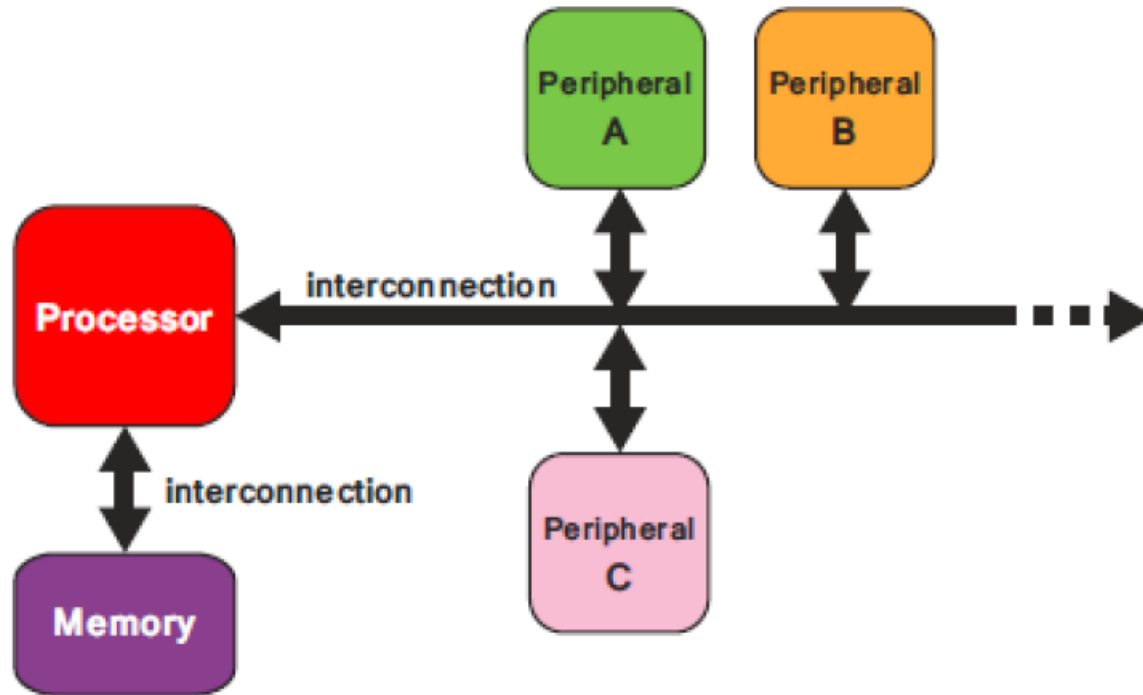

Figure from the "The Zynq Book"

SoC

- A Simple view of an Embededded SoC:

SoC with ZYNQ

- A Simple Vi:ew of the Zynq SoC:

Figure from the "The Zynq Book"

SoC with ZYNQ

Figure from the "The Zynq Book"
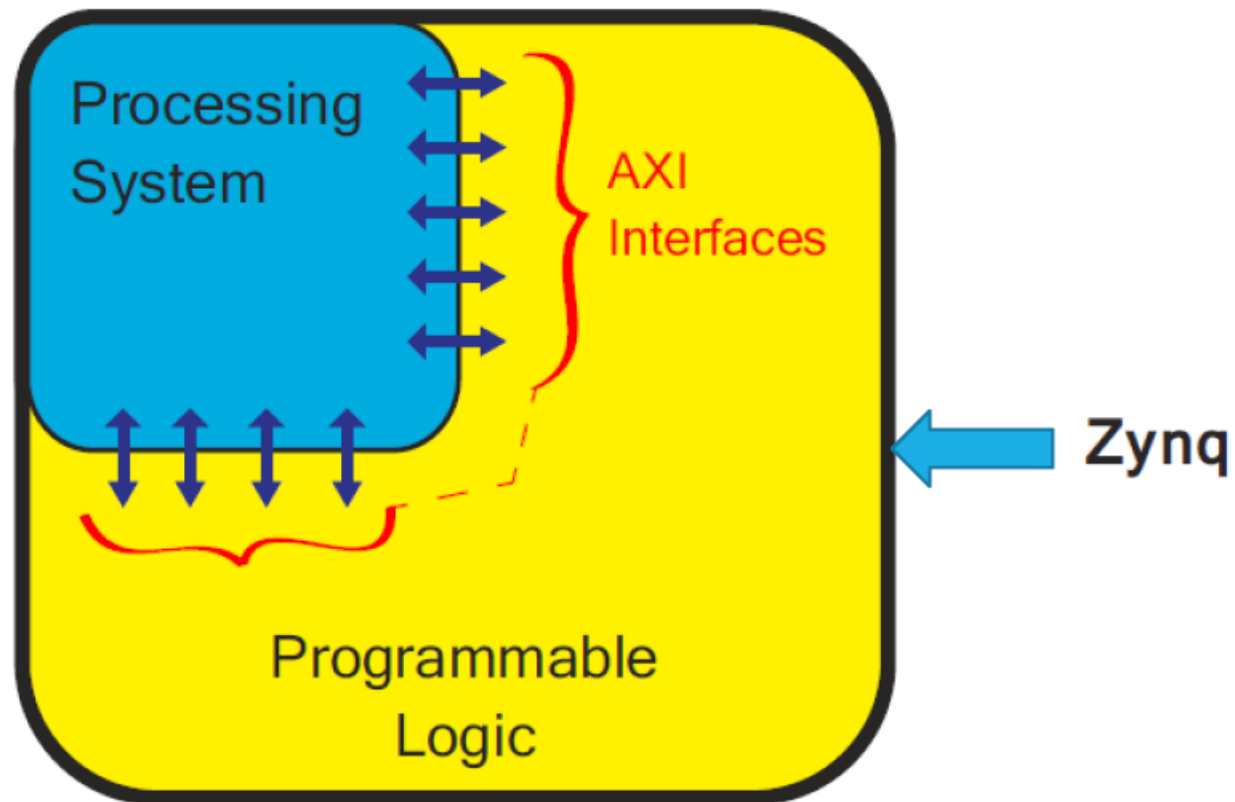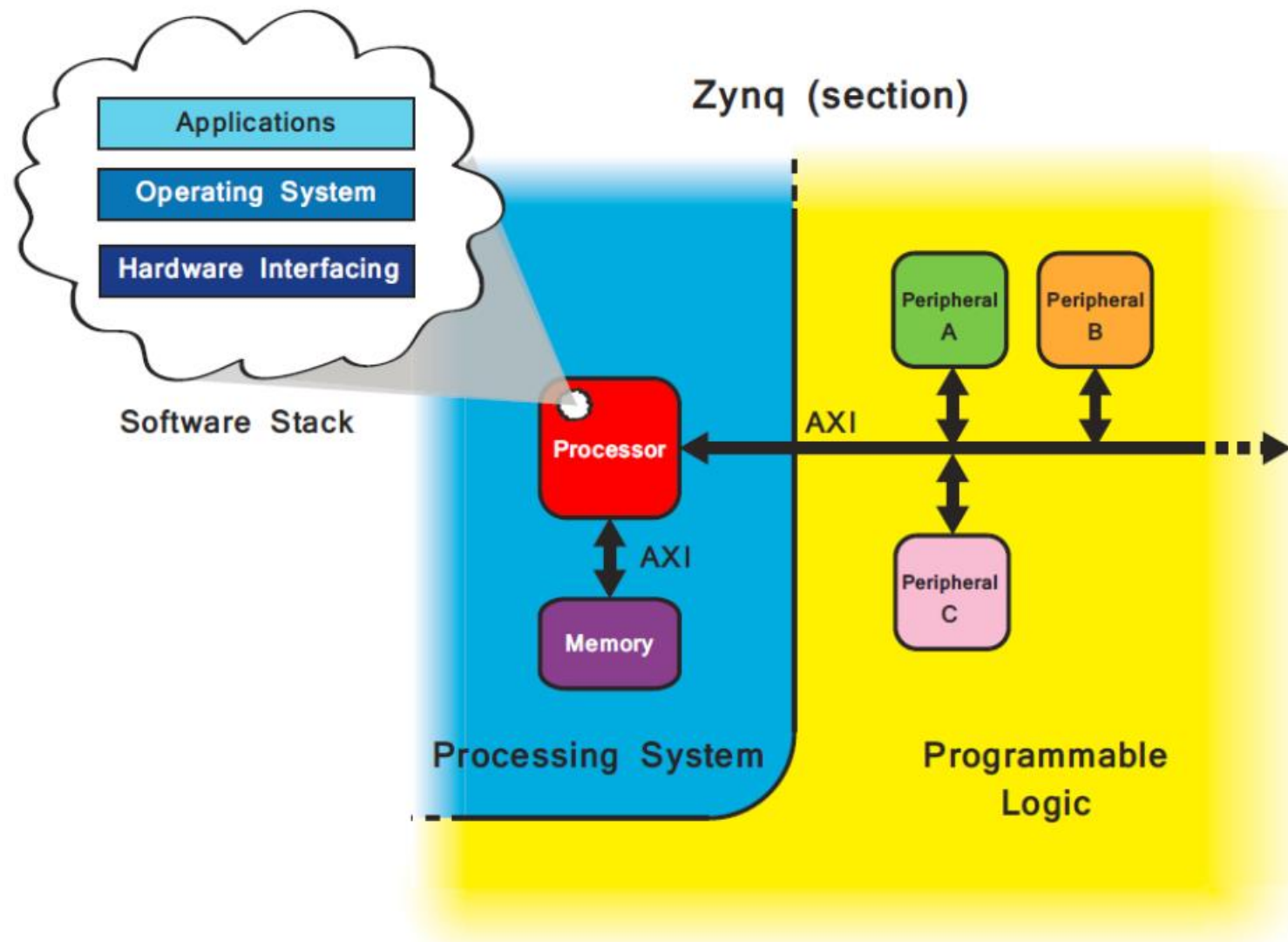
Architectural View of the Zynq

Zynq Architecture and Features

Application Processing Unit (APU)

Processing System

AXI Interfaces

Programmable Logic

Package, pins, and IOBs
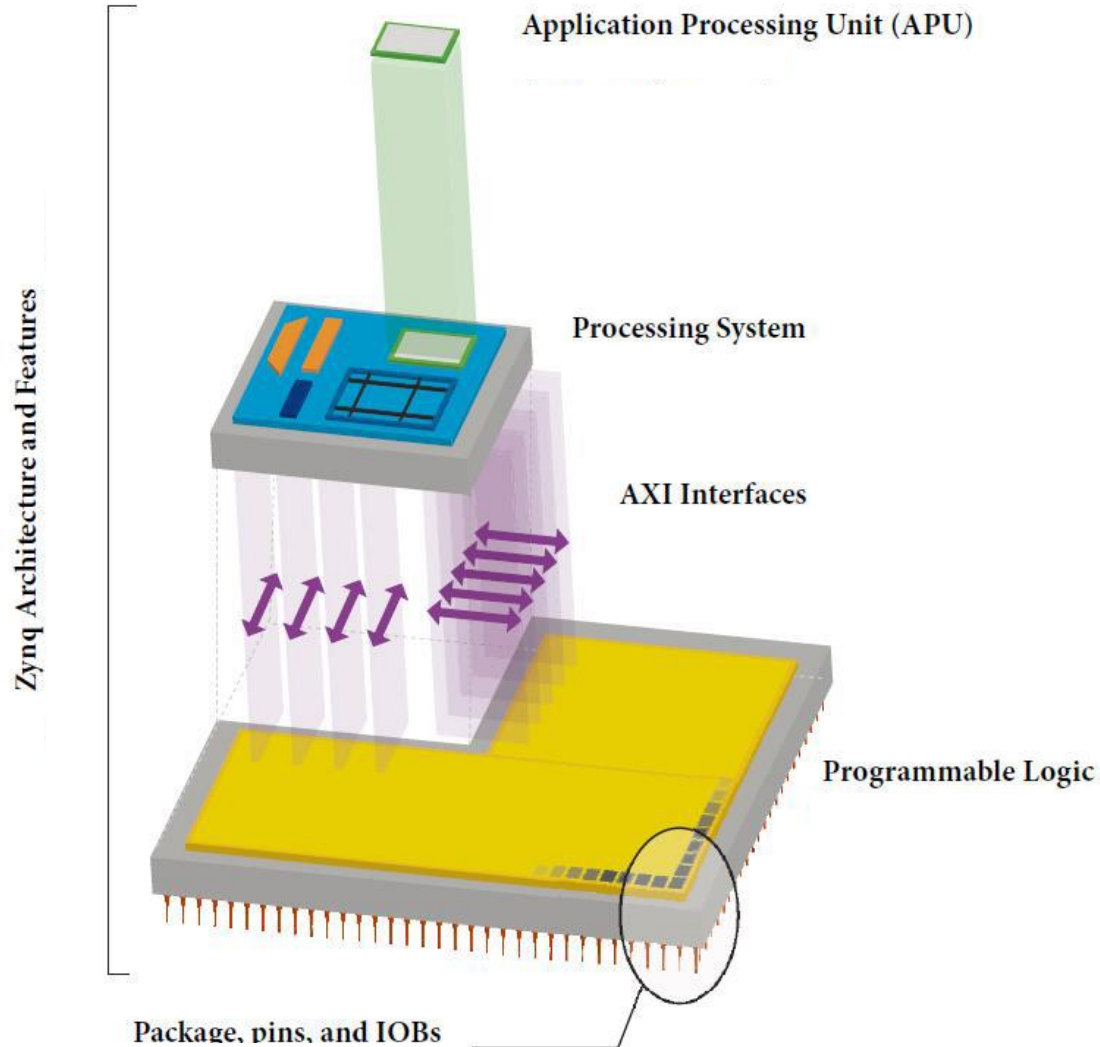
Zynq Architecture 7-Series FPGA Architecture

- 7-Series FPGA Families

Maximum Capability	ARTIX 7 — Lowest Power and Cost	KINTEX 7 — Industry's Best Price/Performance	VIRTEX 7 — Industry's Highest System Performance	ZYNQ — Extensible Processing Platform
Logic Cells	20K – 355K	70K – 480K	285K – 2,000K	30K – 350K
Block RAM	12 Mb	34 Mb	65 Mb	240KB – 2180KB
DSP Slices	40 – 700	240 – 1,920	700 – 3,960	80 – 900
Peak DSP Perf.	504 GMACS	2,450 GMACs	5,053 GMACS	1080 GMACS
Transceivers	4	32	88	16
Transceiver Performance	3.75Gbps	6.6Gbps and 12.5Gbps	12.5Gbps, 13.1Gbps and 28Gbps	6.6Gbps and 12.5Gbps
Memory Performance	1066Mbps	1866Mbps	1866Mbps	1333Mbps
I/O Pins	450	500	1,200	372
I/O Voltages	3.3V and below	3.3V and below 1.8V and below	3.3V and below 1.8V and below	3.3V and below 1.8V and below

7-Series Cost, Powerand Performance

- The different families in the 7-series provide solutions to address the different price/performance/power requirements of the FPGA market
  - Artix™-7 family: Lowest price and power for high volume and consumer applications
    - Battery powered devices, automotive, commercial digital cameras
  - Kintex™-7 family: Best price/performance
    - Wireless and wired communication, medical, broadcast
  - Virtex-7family: Highest performance and capacity
    - High-end wired communication, test and measurement, advanced RADAR, high-performance computing
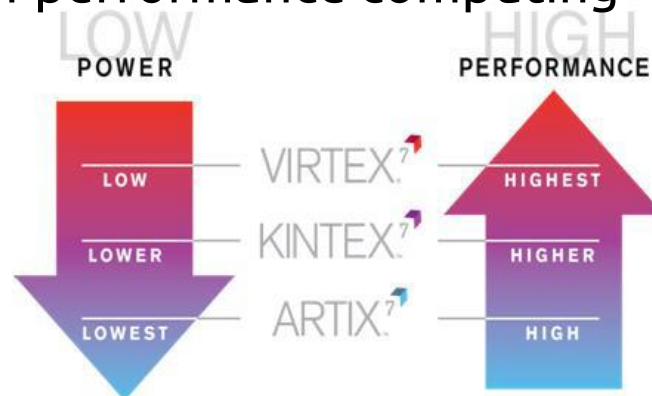
7-Series Architecture–Common Elements

- Common elements enable easy IP reuse for quick design portability across all 7-series families
  - Design scalability from low-cost to high-performance
  - Expanded eco-system support
  - Quickest time to market

Artix-7 FPGA

Kintex-7 FPGA

Virtex-7 FPGA

Logic Fabric
LUT-6 CLB

On-Chip Memory
36Kbit/18Kbit Block RAM

DSP Engines
DSP48E1 Slices

Hi-performance Serial I/O Connectivity
Transceiver Technology

Precise, Low Jitter Clocking
MMCMs

Enhanced Connectivity
PCIe® Interface Blocks
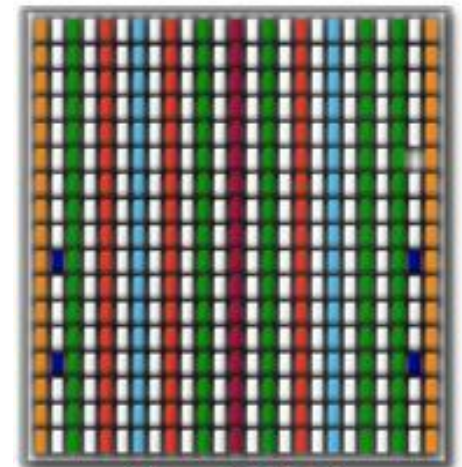
Example of 7-Series Architecture: Artix-7
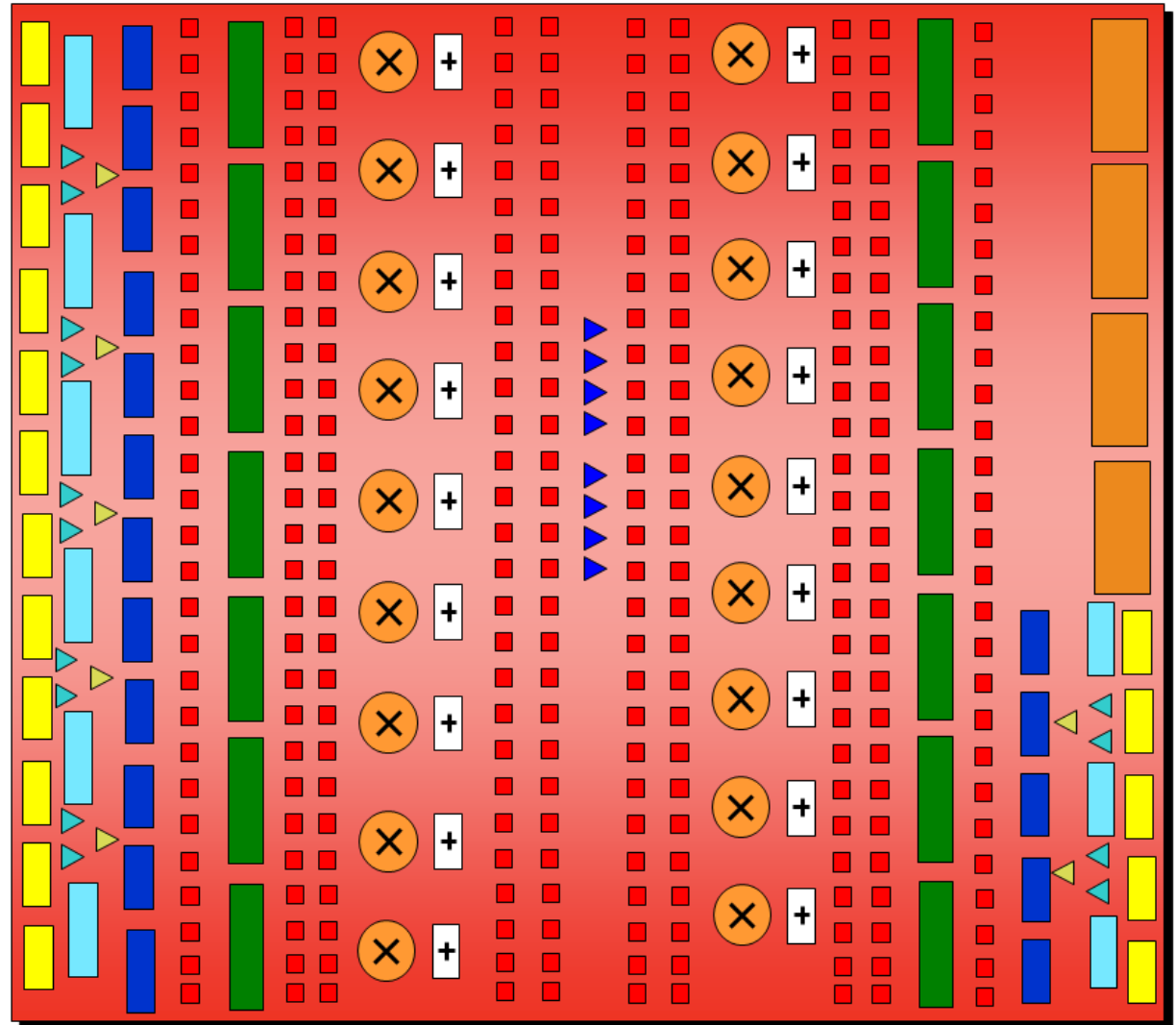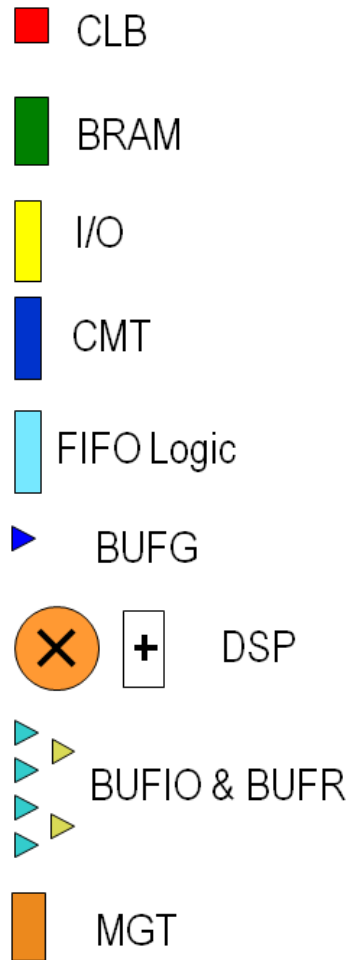
Logic Resources

- CLB – Primary resource for design
    - Combinatorial functions
    - Flip-flops

- CLB contains two slices

- Connected to switch matrix for routing to other FPGA resources

- Carry chain runs vertically in a column from one slice to the one above
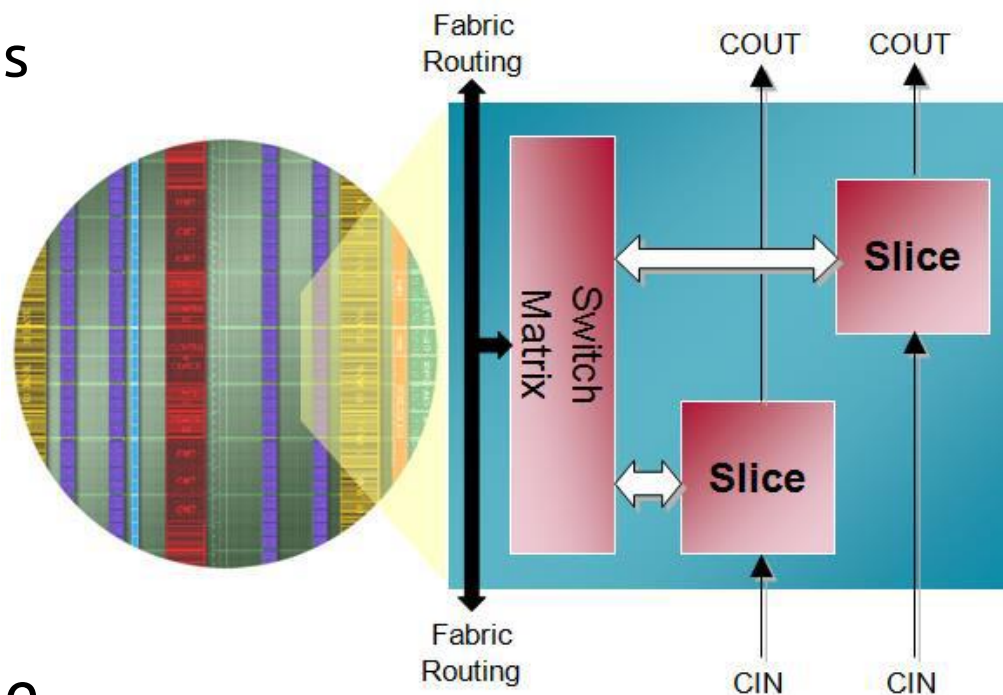
7-Series FPGA Inputs/Outputs

- Wide range of voltages
  - 1.2V to 3.3V operation

- Many different I/O standards
  - Single ended and differential
  - Referenced inputs
  - 3-state support

- Very high performance
  - Up to 1600 Mbps LVDS
  - Up to 1866 Mbps single-ended for DDR3

- Easy interfacing to standard memories
  - Hardware support for QDRII+ and DDR3

- Digitally controlled impedance

- Low power

Xilinx
7 Series
FPGA
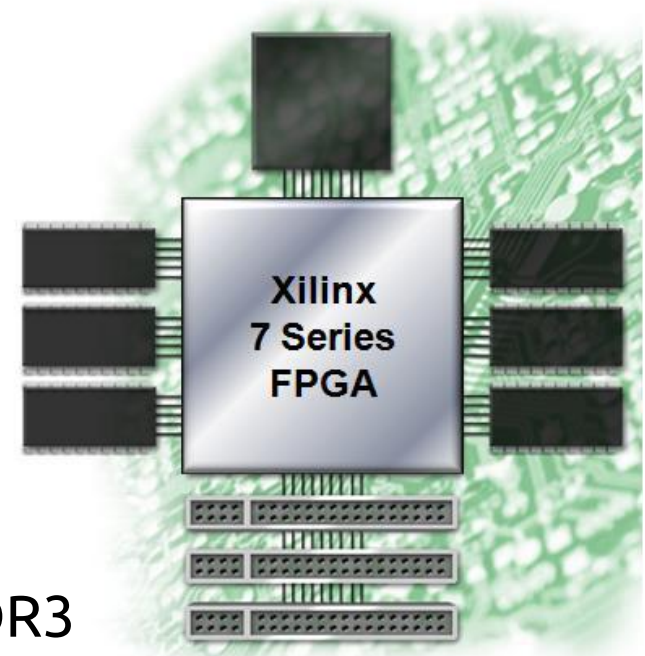
Input/Output Types

- Two different types of I/O in 7-series FPGAs
    - High Range (HR)
        - Supports I/O standards with Vccovoltages up to 3.3V
    - High Performance (HP)
        - Supports I/O standards with Vccovoltages up to 1.8V only
        - Designed for the highest performance
        - Has ODELAY (adjustable or fixed delays) and DCI (Digitally Controlled Impedance) capability

I/O Type	Artix-7 Family	Kintex-7 Family	Virtex-7 Family	Virtex-7 XT/HT/ Family
High Range	All	Most Some		
High Performance		Some	Most	All

7-Series Block RAM and FIFO

- All members of the 7-series families have the same Block RAM/FIFO

- Fully synchronous operation
  - All operations are synchronous; all outputs are latched

- Optional internal pipeline register for higher frequency operation

- Two independent ports access common data
  - Individual address, clock, write enable, clock enable
  - Independent data widths for each port

- Multiple configuration options
  - True dual-port, simple dual-port, single-port

- Integrated control for fast and efficient FIFOs

7-Series DSP48E1 Slice

- 25x18 signed multiplier
- 48-bit add/subtract/accumulate
- 48-bit logic operations
- Pipeline registers for high speed
- Pattern detector
- SIMD operations (12/24 bit)
- Cascade paths for wide functions
- Pre-adder
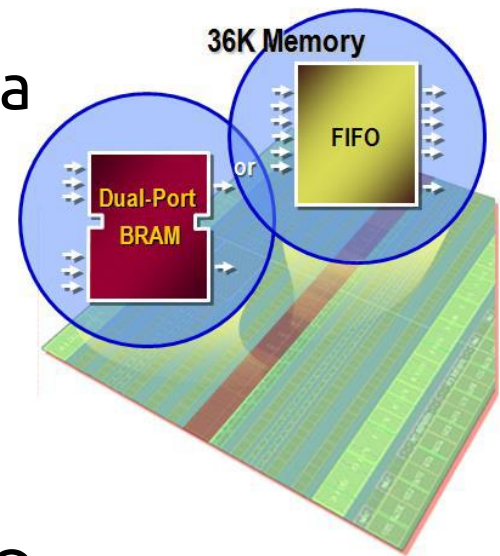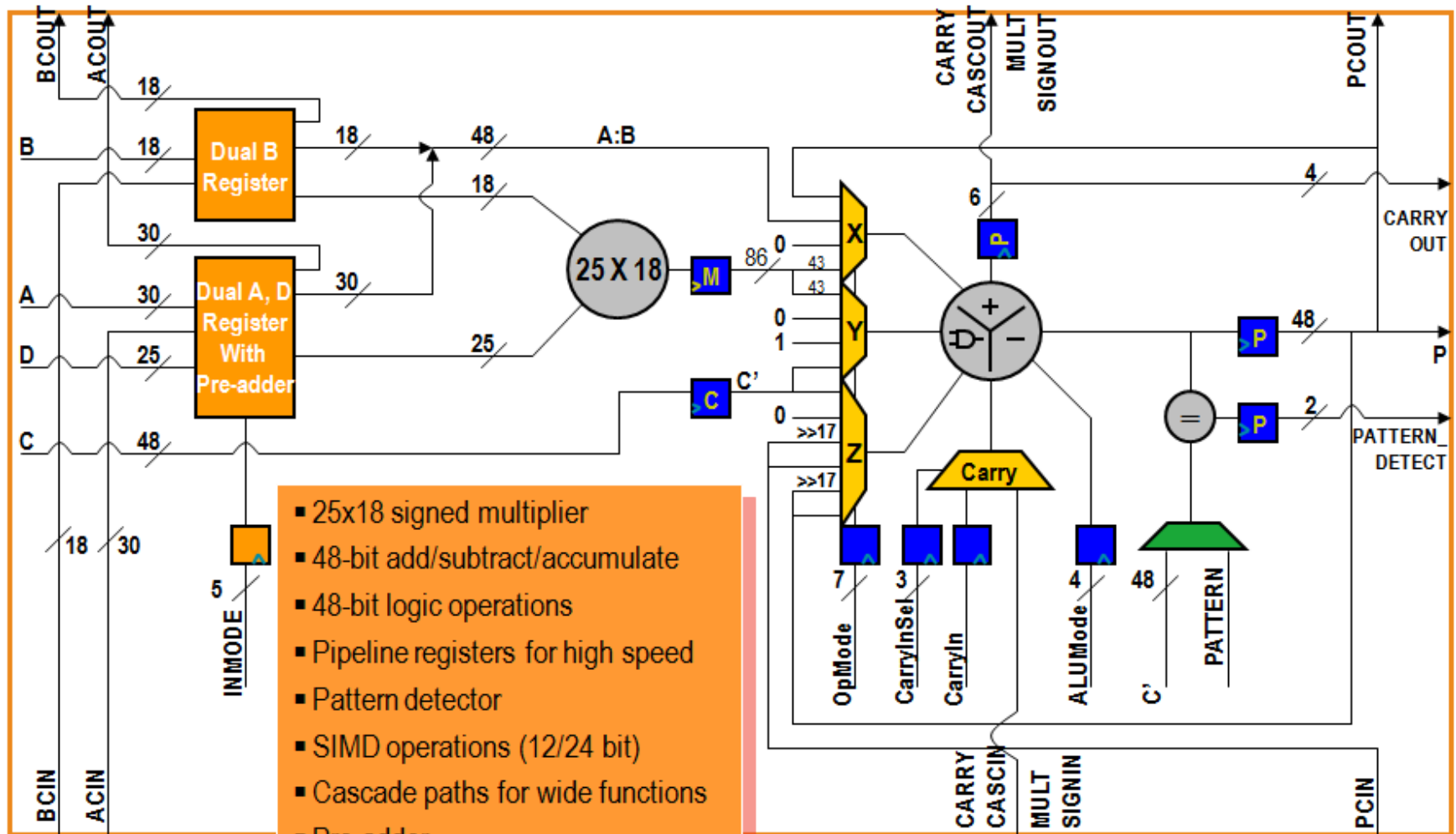
XADC and AnalogMixedSignals(AMS)

- XADC is a high quality and flexible analog interface new to the 7-series
  - Dual 12-bit 1Msps ADCs, on-chip sensors, 17 flexible analog inputs, and track & holds with programmable signal conditioning
  - 1V input range (unipolar, bipolar and differential)
  - 12-bit resolution conversion
  - Built in digital gain and offset calibration
  - On-chip thermal and Voltage sensors
  - Sample rate of 1 MSPS
- Analog Mixed Signal (AMS)
  - Using the FPGA programmable logic to customize the XADC and replace other external analog functions; for example, linearization, calibration, filtering, and DC balancing to improve data conversion resolution

Zynq-7000 Main Features
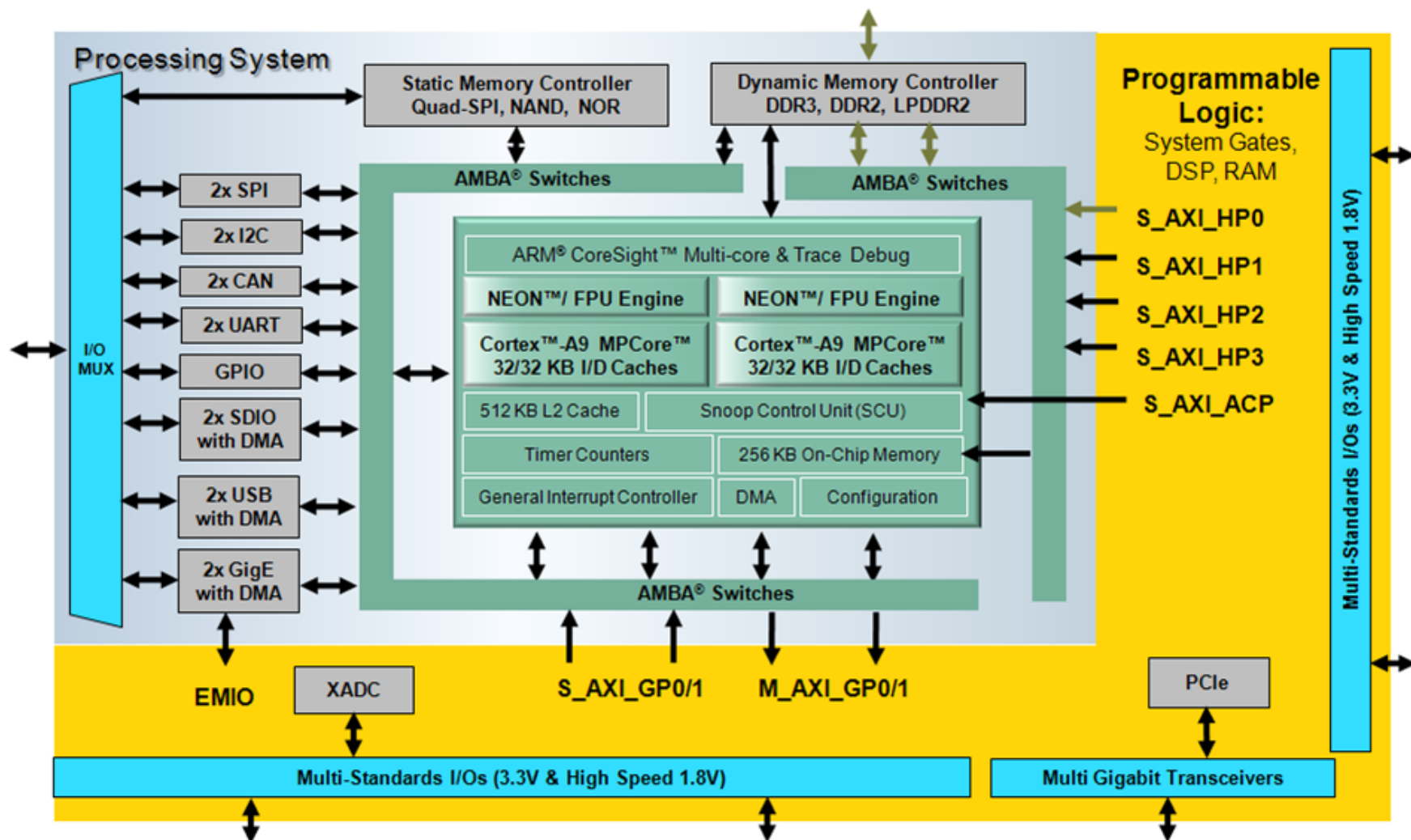
Zynq-7000 Main Features

- Complete ARM®-based processing system
  - Application Processor Unit (APU)
    - Dual ARM Cortex™-A9 processors
    - Caches and support blocks
  - Fully integrated memory controllers
  - I/O peripherals
- Tightly integrated programmable logic
  - Used to extend the processing system
  - Scalable density and performance
- Flexible array of I/O
  - Wide range of external multi-standard I/O
  - High-performance integrated serial transceivers
  - Analog-to-digital converter inputs

ARM Processor Architecture

- ARM Cortex-A9 processor implements the ARMv7-A architecture
  - ARMv7 is the ARM Instruction Set Architecture (ISA)
    - Thumb instructions: 16 bits; Thumb-2 instructions: 32 bits
    - NEON: ARM's Single Instruction Multiple Data (SIMD) instructions
  - ARMv7-A: Application set that includes support for a Memory Management Unit (MMU)

    - ARMv7-R: Real-time set that includes support for a Memory Protection Unit (MPU)
    - ARMv7-M: Microcontroller set that is the smallest set

- ARM Advanced Microcontroller Bus Architecture (AMBA®) protocol
  - AXI3: Third-generation ARM interface
  - AXI4: Adding to the existing AXI definition (extended bursts, subsets)

Zynq SoC Block Diagram
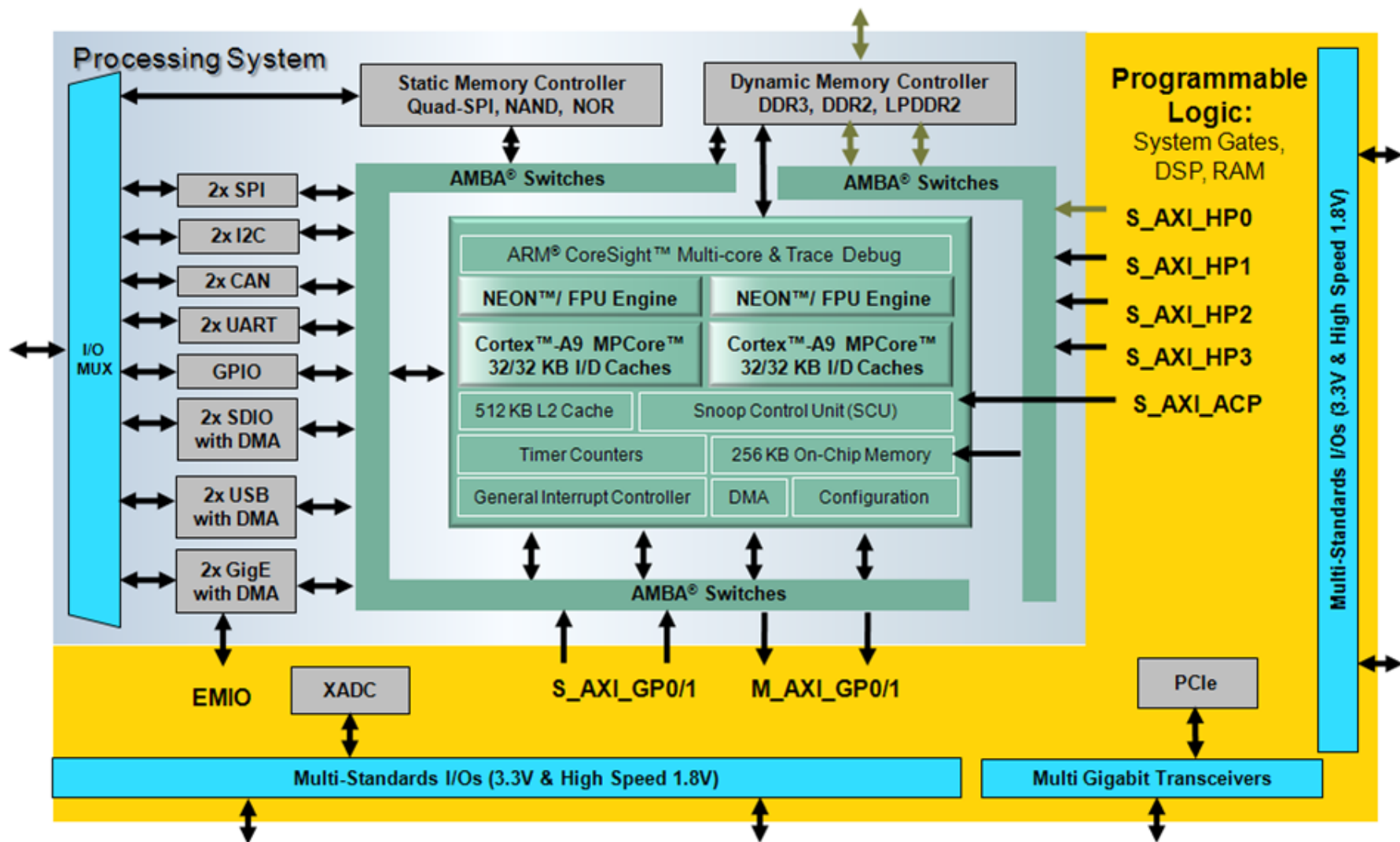
PS Main Components

- Application processing unit (APU)
- I/O peripherals (IOP)
  - Multiplexed I/O (MIO), extended multiplexed I/O (EMIO)
- Memory interfaces
- PS interconnect
- DMA
- Timers
  - Public and private
- General interrupt controller (GIC)
- On-chip memory (OCM): RAM
- Debug controller: CoreSight

PL Main Components

- Configurable logic blocks (CLB)
  - 6-input look-up tables (LUTs)
  - Memory capability within the LUT
  - Register and shift register functionality
- 36 Kb BRAM
- DSP48E1 Slice
- Clock management
- Configurable I/Os
- High Speed Serial Transceivers
- Integrated interface for PCI Express

Zynq	FPGA Based Fabric
7z010, 7z015, 7z020	Artix
7z030, 7z035, 7z045, 7z100	Kintex

PS-PL Interface

- AXI high-performance slave ports (HP0-HP3)
  - Configurable 32-bit or 64-bit data width
  - Access to OCM (On-Chip Memory) and DDR
  - Conversion to processing system clock domain
  - AXI FIFO Interface (AFI) are FIFOs (1KB) to smooth large data transfers

- AXI general-purpose ports (GP0-GP1)
  - Two masters from PS to PL
  - Two slaves from PL to PS
  - 32-bit data width
  - Conversation and sync to processing system clock domain

PS-PL Interface

- One 64-bit accelerator coherence port (ACP) AXI slave interface to CPU memory

- DMA, interrupts, events signals
  - Processor event bus for signaling event information to the CPU
  - PL peripheral IP interrupts to the PS general interrupt controller (GIC)
  - Four DMA channel RDY/ACK signals

- Extended multiplexed I/O (EMIO) allows PS peripheral ports access to PL logic and device I/O pins

- Clock and resets
  - Four PS clock outputs to the PL with enable control
  - Four PS reset outputs to the PL

PS-PL Interface

PS-PL Interface

*Zynq 7z030, 7x045 & 7z100 only
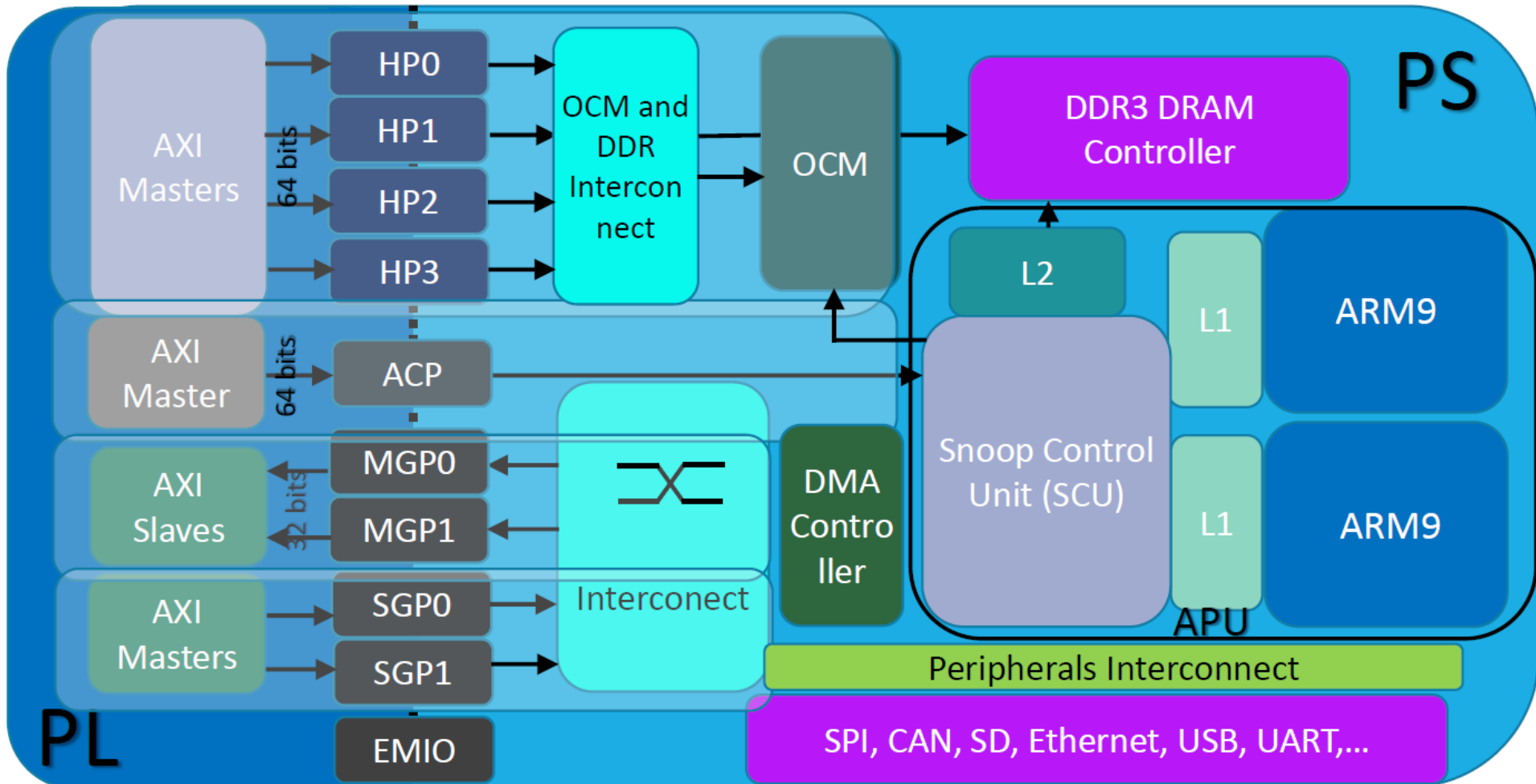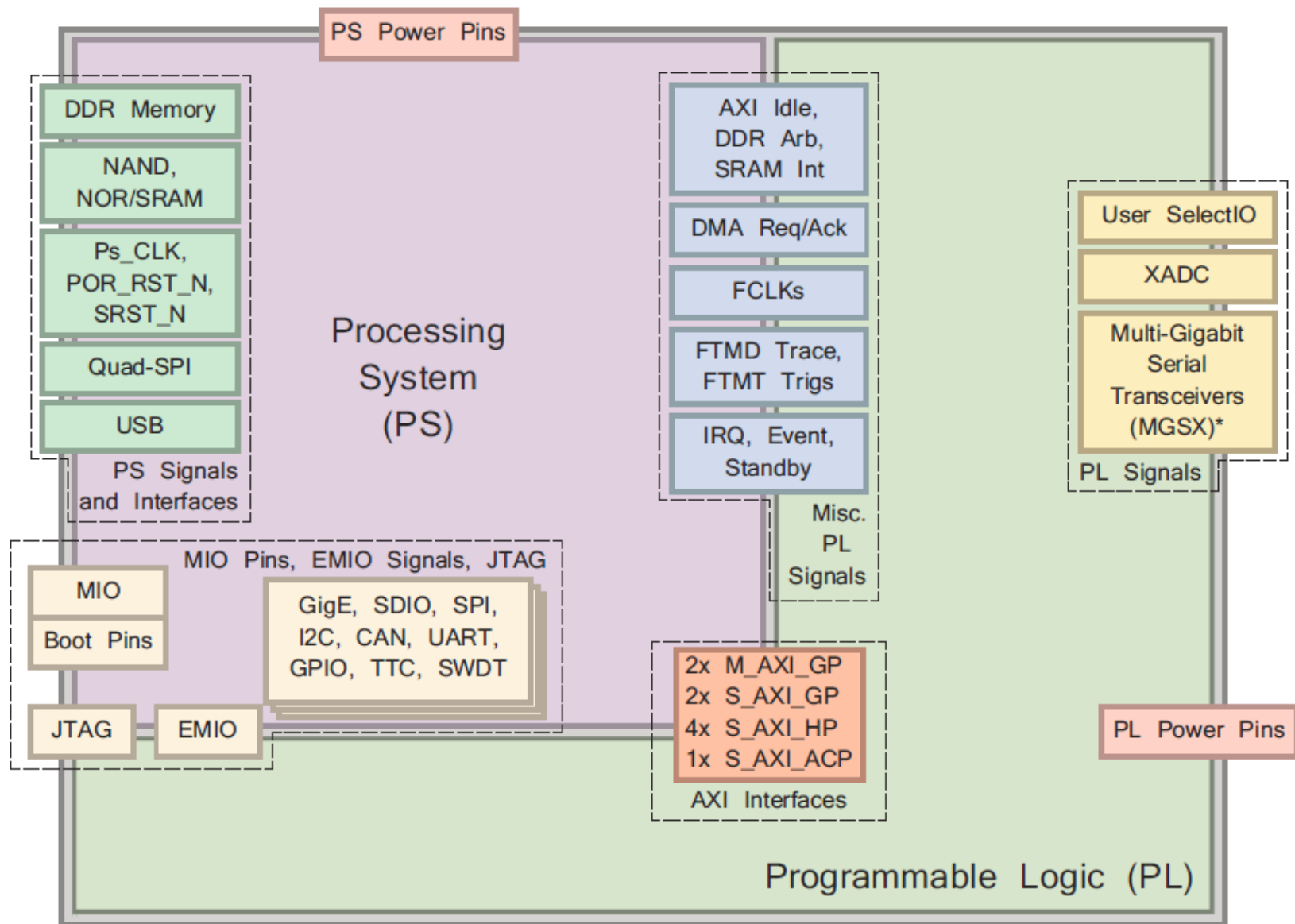
PS-PL Miscellaneous Signals

- PL Clocks and Resets

- PL Interrupts to PS

- IOP Interrupts to PL

- Events

- Idle AXI, DDR, ARB, SRAM Interrupt

- DMA Controller

- EMIO Signals

PS Peripherals and Connections

ZynqArchitecture – Build-In Devices

- Two USB 2.0 OTG/device/host
- Two tri-mode gigabit Ethernet (10/100/1000)
- Two SD/SDIO interfaces
  - Memory, I/O, and combo cards
- 2xCAN 2.0Bs, 2xSPIs, 2xI2Cs, 2x UARTs
- Four GPIO 32-bit blocks
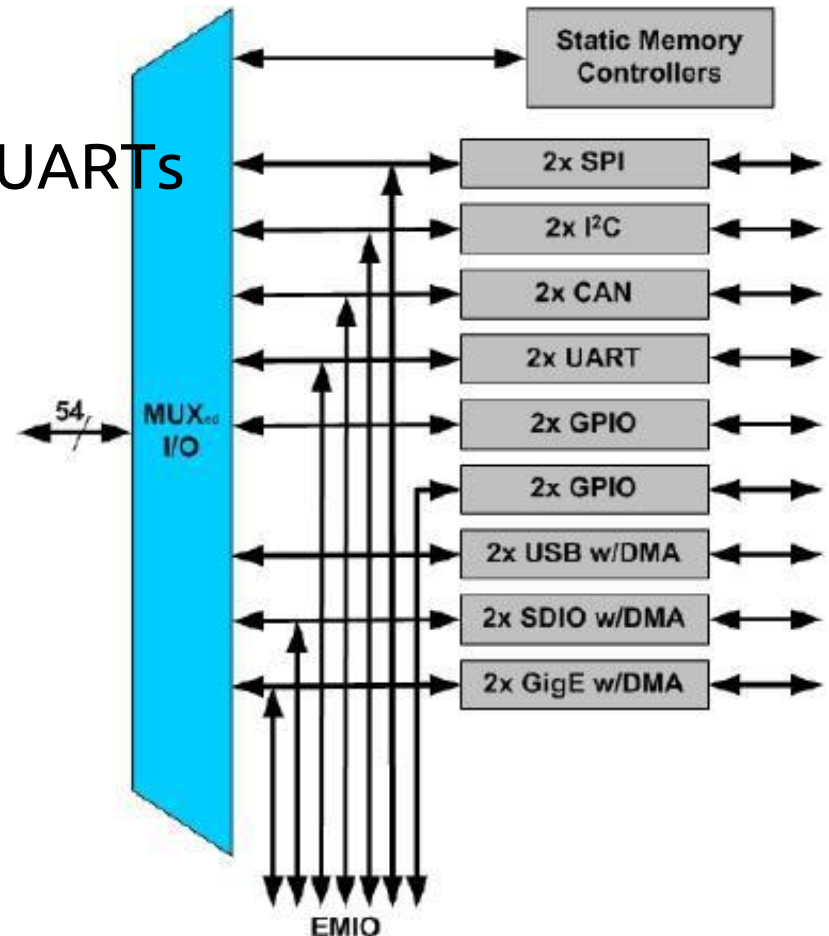
Multiplexed I/O –Internal / External

- Multiplexed input/output (MIO)
  - Multiplexed output of peripheral and static memories
  - Two I/O banks; each selectable: 1.8V, 2.5V, or 3.3V
  - Configured using configuration
  - Dedicated pins are used
    - User constraints (LOC) should not be present
      - The BitGenprocess will throw errors if LOC constraints are present

- Extended MIO
  - Enables use of the SelectIO™ interface with PS peripherals
  - User constraints must be present for the signals brought out to the SelectIO pins
    - The BitGenprocess will throw errors if LOC constraints are not present
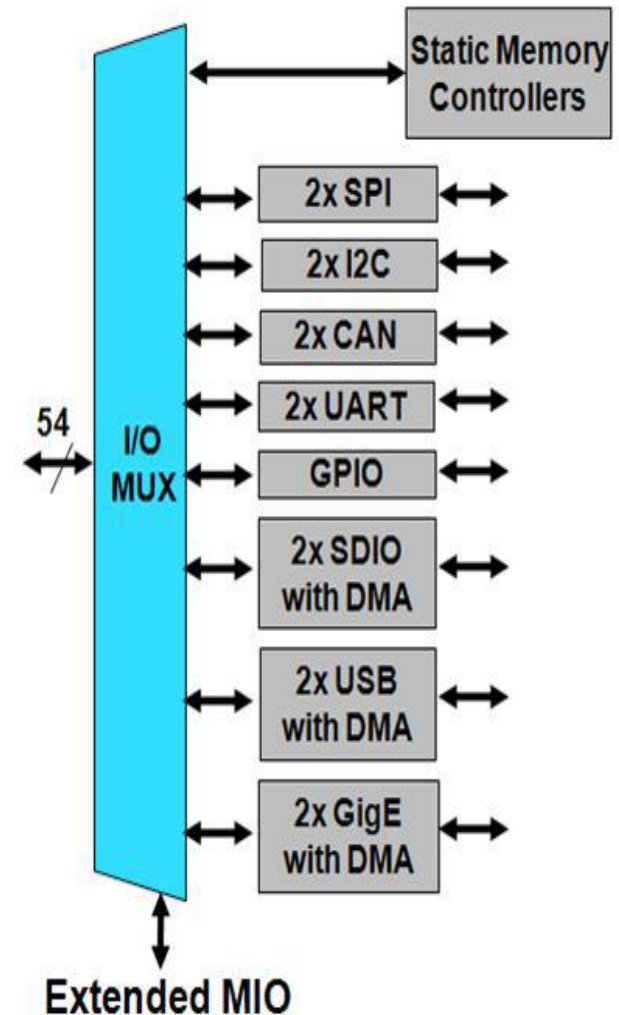
MIO Port Configuration
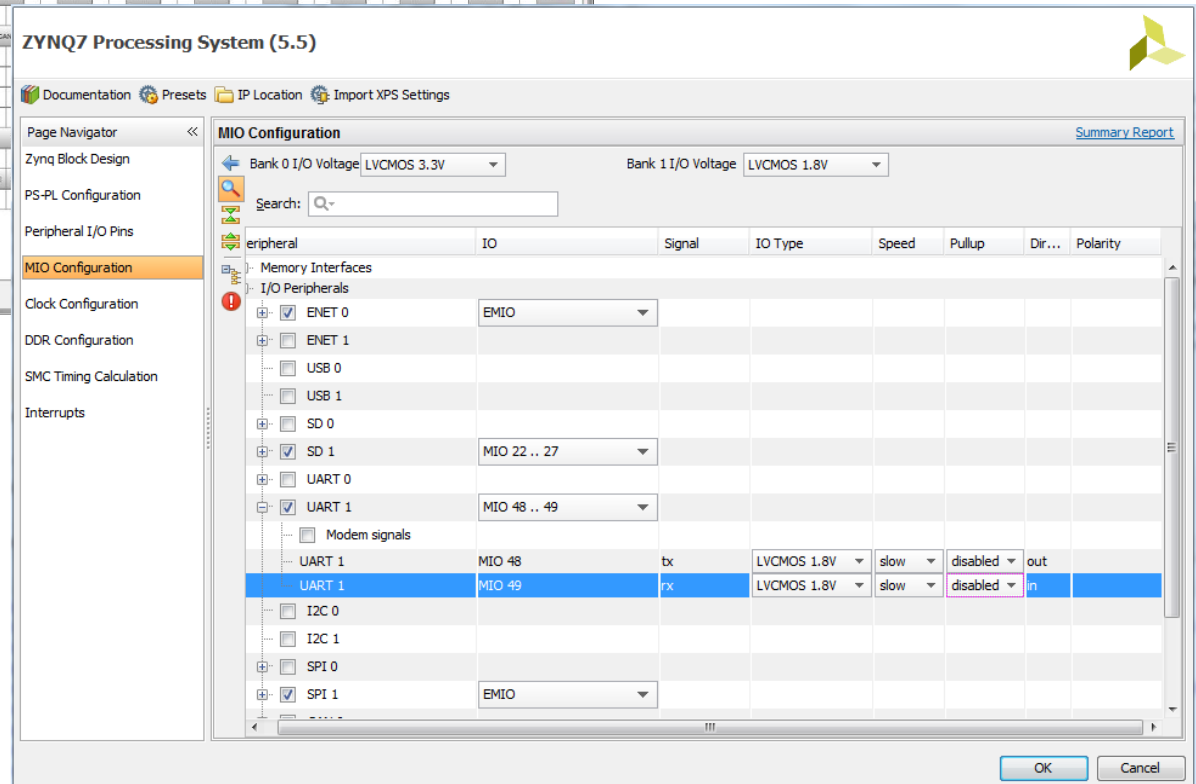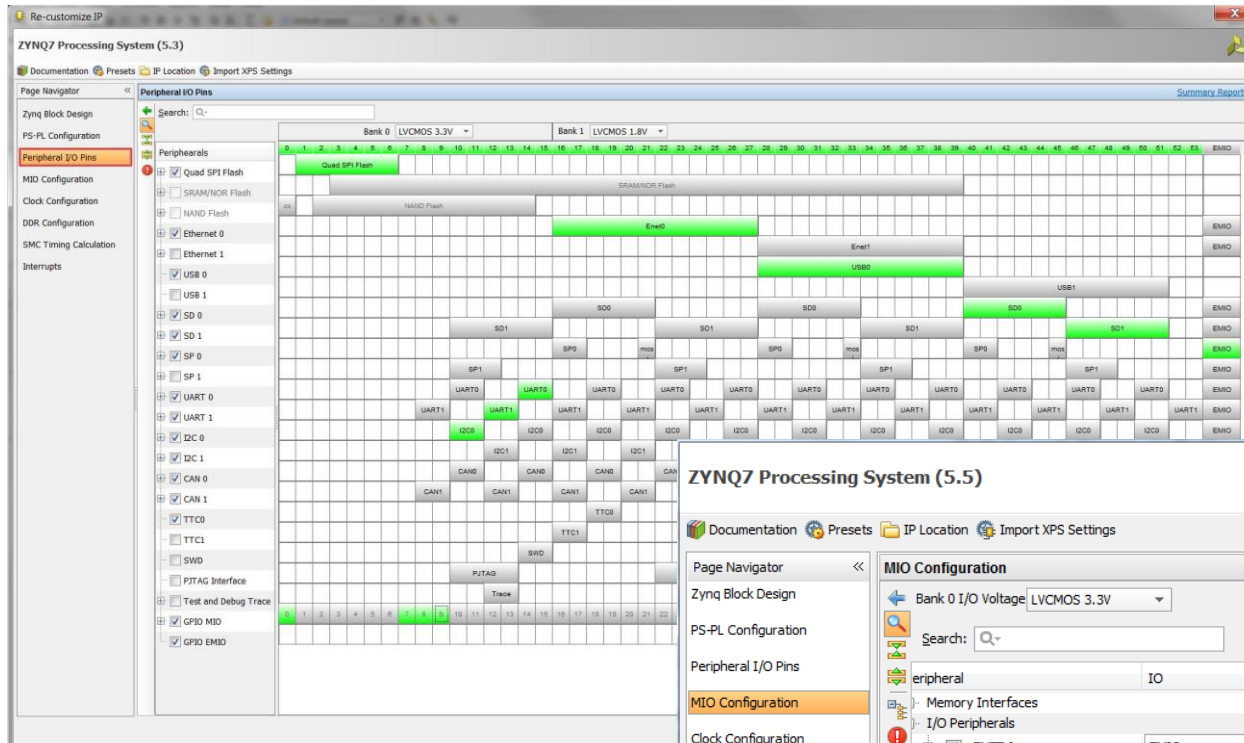
Extended Multiplexed I/O (EMIO)

- Extended interface to PS I/O peripheral ports
  - EMIO: Peripheral port to PL
  - Alternative to using MIO
  - Mandatory for some peripheral ports
  - Facilitates
    - Connection to peripheral in programmable logic
    - Use of general I/O pins to supplement MIO pin usage
    - Allows additional signals for many of the peripherals

Zynq Block Design

IO Peripherals
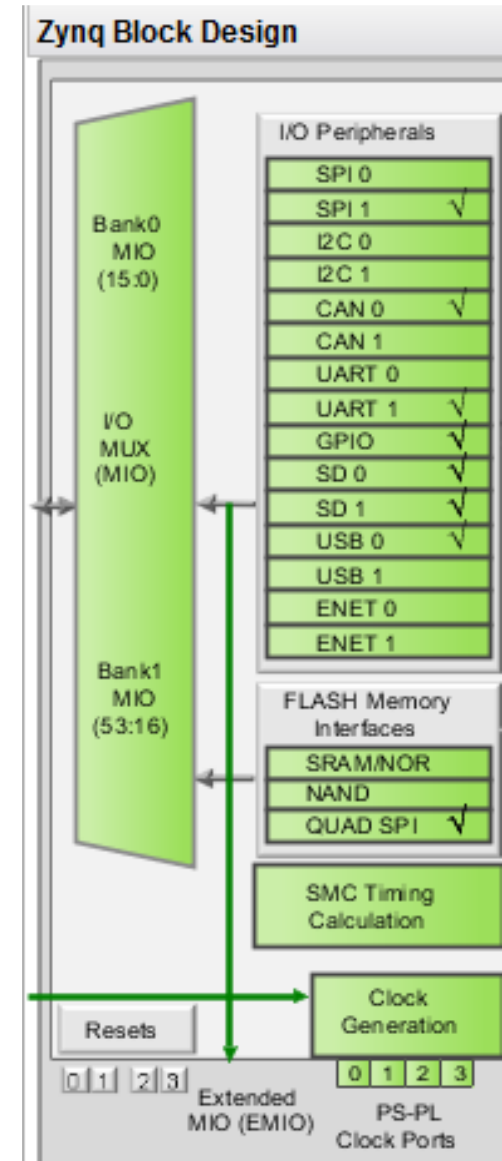
- I²C (Inter-Integrated Circuit)
  - I²C bus specification version 2
  - Programmable to use normal (7-bit) or extended (10-bit) addressing
  - Programmable rates: fast mode (400 kbit/s) , standard (10 0kbits/s), and low (10 kbits/s)
    - Rates higher than 400 kbits/sec are not supported
  - Programmable as either a master or slave interface
  - Capable of clock synchronization and bus arbitration
  - Fully programmable slave response address
  - Reversible FIFO operation supported
  - 16-byte buffer size
  - Slave monitor mode when set up as master

IO Peripherals

- CAN (Controller Area Network)
  - Up to 24-MHz CAN_REF clock as system clock
  - 64 message-deep receiver and transmitter buffer
  - Full CAN 2.0B compliant; conforms to ISO 11898-1
  - Maximum baud rate of 1 Mb/s
  - Four message filters required for buffer mode
  - Listen-only mode for test and debug
  - External PHY I/O
  - "Wake-on-message"
  - Time-stamping for receive messages
  - TX and RX FIFO watermarking
  - Exception: no power-down mode

IO Peripherals

- SD-SDIO
  - Support for version 2.0 of SD Specification
  - Full-speed (4 MB/s) and low-speed (2 MB/s) support
    - Low-speed clock (400 KHz) used until bandwidth negotiated
  - 1-bit and 4-bit data interface support
  - Host mode support only
  - Built-in DMA controller
  - Full-speed clock (0-50 MHz) with maximum throughput at 25 MB/s
  - 1 KB data FIFO interface
  - Support for MMC 3.31 card at 52 MHz
  - Support for memory, I/O, and combo cards
  - Support for power control modes and interrupts

IO Peripherals

- SPI (Serial Peripheral Interface)
  - Master or slave SPI mode
  - Four wire bus: MOSI, MISO, SCK, nSS
  - Supports up to three slave select lines
  - Supports multi-master environment
  - Identifies an error condition if more than one master detected
  - Software can poll for status or function as interrupt-driven device
  - Programmable interrupt generation
  - 50-MHz maximum external SPI clock rate
  - Selectable master clock reference
  - Integrated 128-byte deep read and write FIFOs
  - Full-duplex operation offers simultaneous receive and transmit

IO Peripherals

- UART
  - Two UARTs
  - Programmable baud rate generator
  - 64-byte receive and transmit FIFOs
  - 6, 7, or 8 data bits and 1, 1.5, or 2 stop bits
  - Odd, even, space, mark, or no parity with parity, framing, and overrun error detection
  - Normal, automatic echo, local loopback, and remote loopback channel modes
  - Interrupts generation
  - Support 8 Mb/s maximum baud rate with additional reference clock or up to 1.5 Mb/s with a 100-MHz peripheral bus clock
  - Modem control signals: CTS, RTS, DSR, DTR, RI, and DCD (through EMIO)
  - Simple UART: only two pins (TX and RX through MIO)

IO Peripherals

- USB
  - Two USB 2.0 hardened IP peripherals per Zynq device
    - Each independently controlled and configured
  - Supported interfaces
    - High-speed USB 2.0: 480 Mbit/s
    - Full-speed USB 1.1: 12 Mbit/s
    - Low-speed USB 1.0: 1.5 Mbit/s
    - Communication starts at USB 2.0 speed and drops until sync is achieved
  - Each block can be configured as host, device, or on-the-go (OTG)
  - 8-bit ULPI interface (USB 2.0 Transceiver Low Pin Interface)
  - All four transfer types supported: isochronous, interrupt, bulk, and control
  - Supports up to 12 endpoints per USB block in the Zynq device
    - Running in host mode
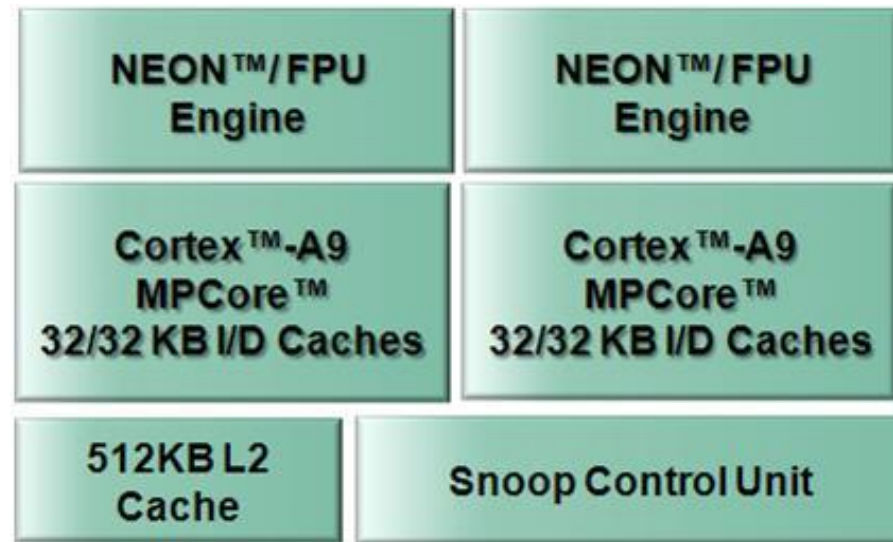 - Source-code drivers

IO Peripherals

- Gigabit Ethernet Controller
  - Tri-mode Ethernet MAC (10/100/1G) with native GMII (gigabit media-independent interface) interface
  - IEEE1588 rev 2.0
    - Time stamp support
    - 1 us resolution
  - IEEE802.3
  - TX/RX checksum offload for TCP and UDP
  - Internal DMA and wake on LAN

Application Processor Unit (APU)
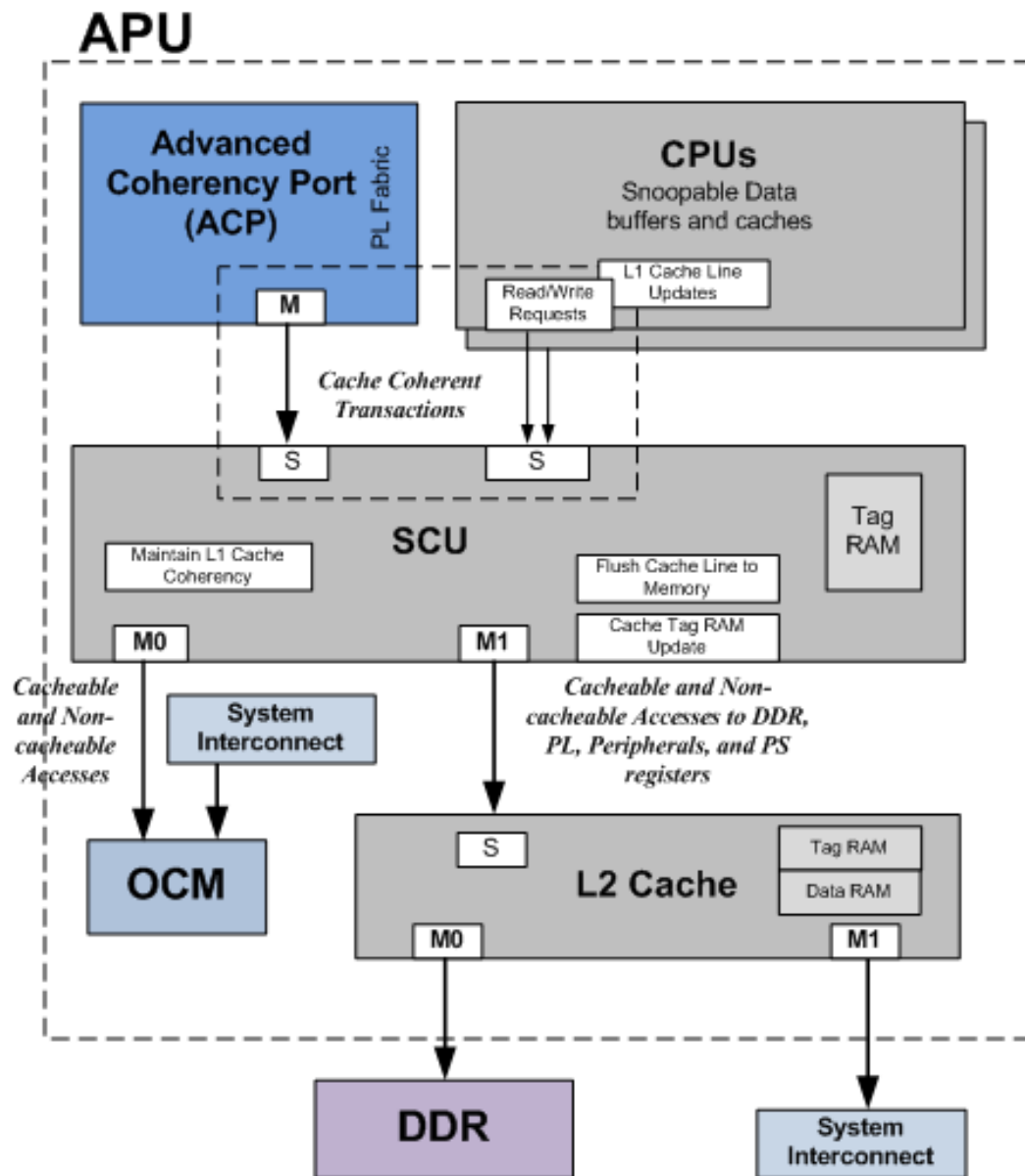
APU Components

- Dual ARM® Cortex™-A9 MPCorewith NEON extensions
  - Up to 800-MHz operation
  - 2.5 DMIPS/MHz per core
  - Separate 32KB instruction and data caches
- Snoop Control Unit (SCU)
  - L1 cache snoop control
    - Accelerator coherency port
- Level 2 cache and controller
  - Shared 512 KB cache with parity

NEON™/FPU Engine	NEON™/FPU Engine
Cortex™-A9 MPCore™ 32/32 KB I/D Caches	Cortex™-A9 MPCore™ 32/32 KB I/D Caches
512KB L2 Cache	Snoop Control Unit

APU Address Map

- All registers for both CPUs are grouped into two contiguous 4KB pages
  - Accessed through a dedicated internal bus
- Fixed at 0xF8F0_0000 with a register block size of 8 KB
  - Each CPU uses an offset into this base address

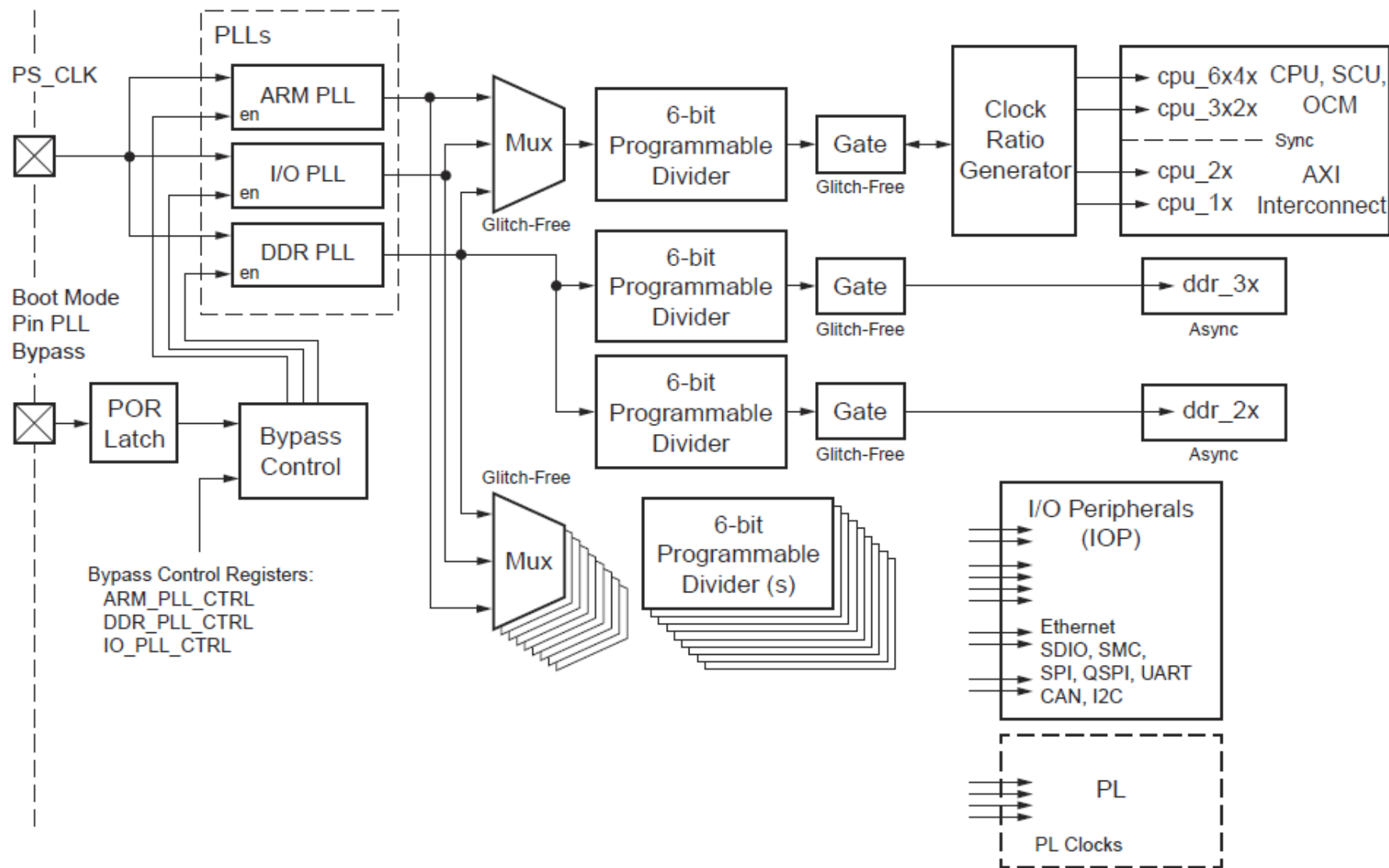|	
0x0000-0x00FC	SCU registers
0x0100-0x01FF	Interrupt controller interface
0x0200-0x02FF	Global timer
0x0600-0x06FF	Private timers and watchdog timers
0x1000-0x1FFF	Interrupt distributor

NEON Main Features

- NEON is the ARM codename for the vector processing unit
  - Provides multimedia and signal processing support
- FPU is the floating-point unit extension to NEON
  - Both NEON and FPU share a single set of registers
- NEON technology is a wide single instruction,multipl edata(SIMD) parallel and co-processing architecture
  - 32 registers, 64-bits wide (dual view as 16 registers, 128-bits wide)
  - Data types can be: signed/unsigned 8-bit, 16-bit, 32-bit, 64-bit, or 32-bit float

Cache Features

- L1
    - Separate instruction and data caches for each processor
    - Caches are four-way, set associative and are write-back
    - Non-lockable
    - Eight words cache length
    - On a cache miss, critical word first filling of the cache is performed followed by the next word in sequence

- L2
    - 512K bytes of RAM built into the SCU
        - Latency of 25 CPU cycles
        - Unified instruction and data cache
    - Fixed, 256-bit (32 words) cache line size
    - Support for per-master way lockdown between multiple CPUs
    - Eight-way, set associative
    - Two AXI interfaces
        - One to DDR controller
        - One to programmable logic master (to peripherals)

- Snoop Control Unit (SCU)
  - Data cache coherency between the processors
  - Initiates L2 AXI memory access
  - Arbitrates between the processors requesting L2 accesses
  - Manages ACP (Access Control Policy) accesses
  - A second master port with programmable address filtering between OCM and L2 memory support

- On-Chip Memory (OCM)
  - The on-chip memory (OCM) module contains 256 KB of RAM and 128 KB of ROM (BootROM).
  - The BootROM memory is used exclusively by the boot process and is not visible to the user.

Zynq Clocks

UG585_c25_01_102414

PL Clocks

UG585_c25_10_041612