VexiiRiscv :
Pushing FPGA softcore performances forward

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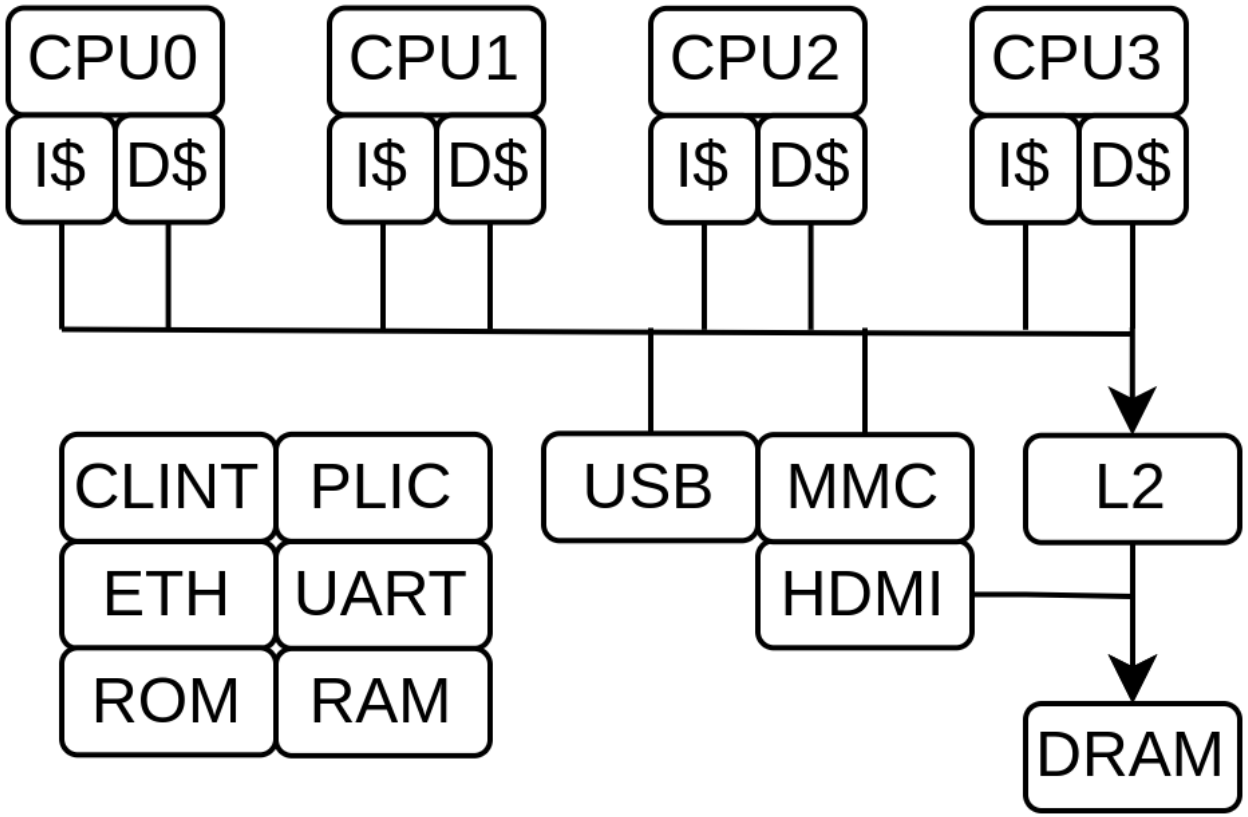
SoC in this demo

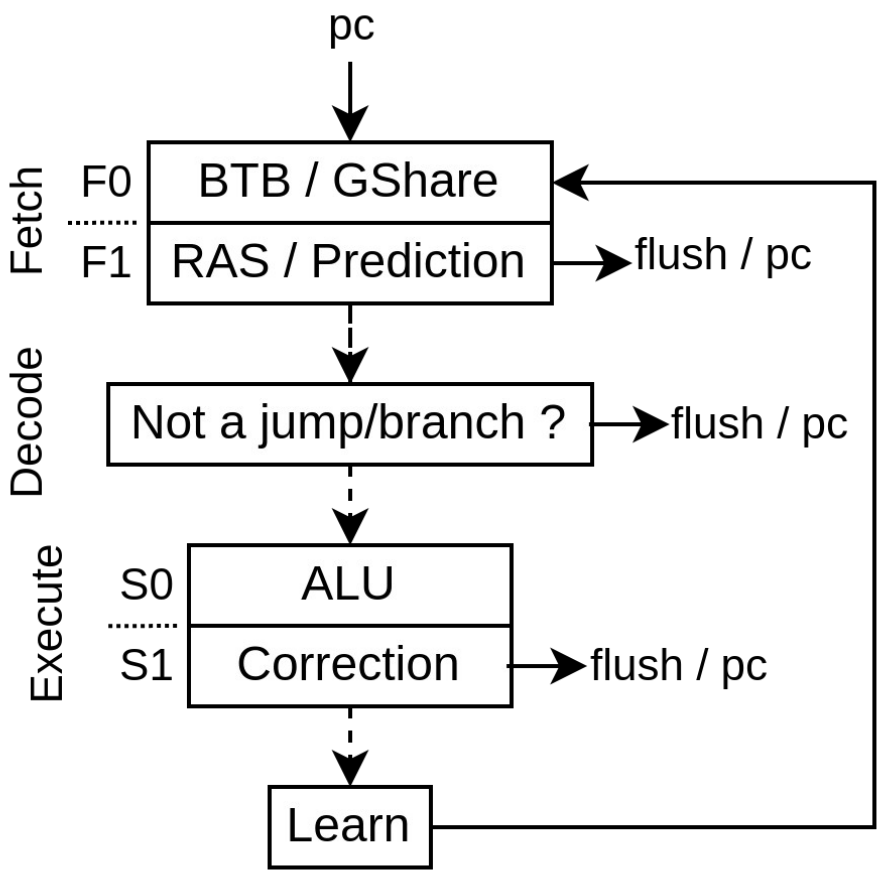
- Use litex infrastructure
- Tilelink based
- RV64GC x4
- 256 KB L2
- 16 KB I$
- 16 KB D$
- Artix A7-1
- ~65KLUT
- 100 Mhz



VexiiRiscv feature set

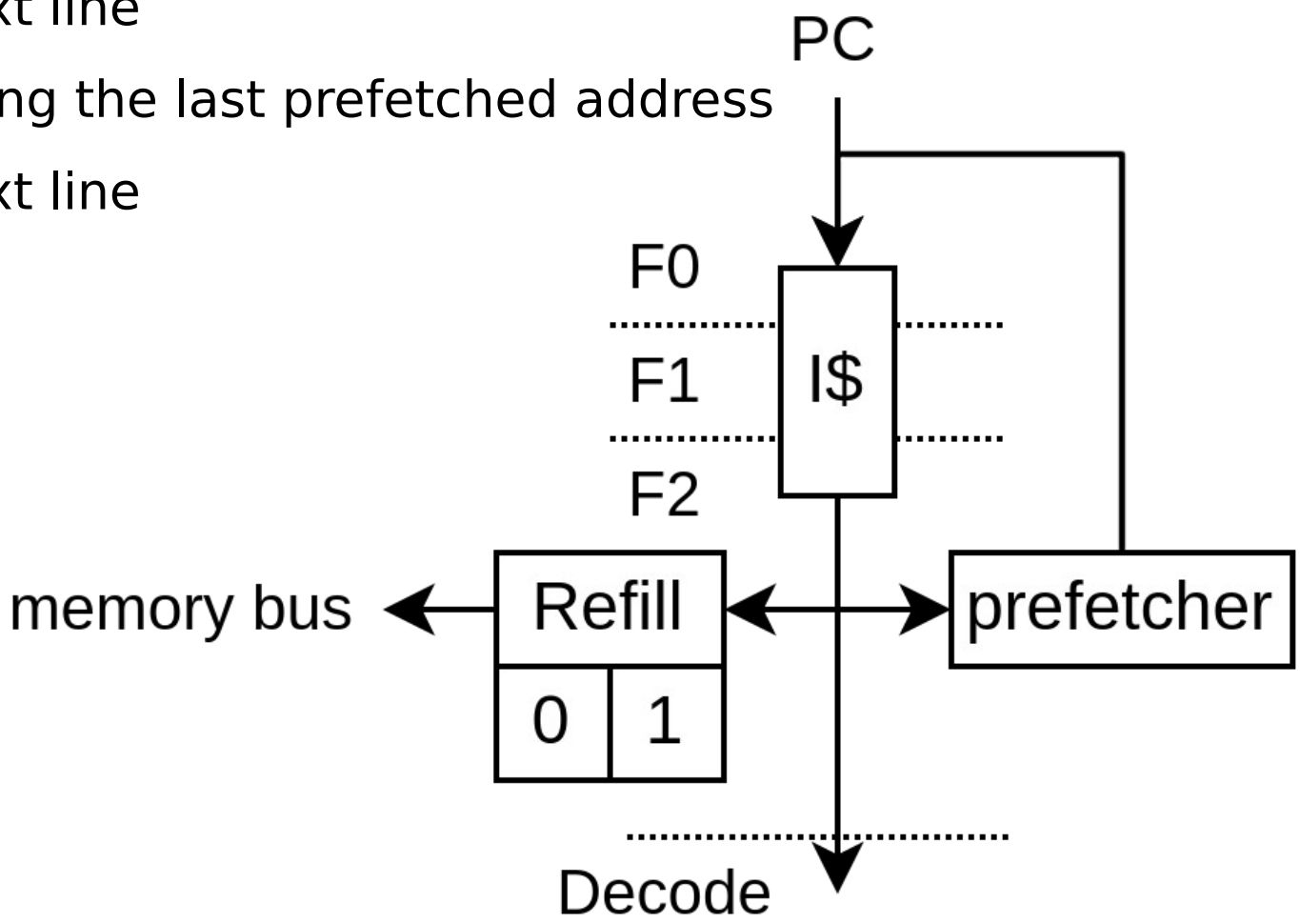
- Mainly :
  - RV32/RV64, optional MAFDCBSU
  - Can run linux / buildroot / Debian
  - Optional multi-issue
  - Optional late-ALU
  - Up to 5.24 coremark/Mhz 2.50 dhystone/Mhz
  - Free / open-source
  - RISC-V official jtag debug
  - Litex port

“Branch” prediction

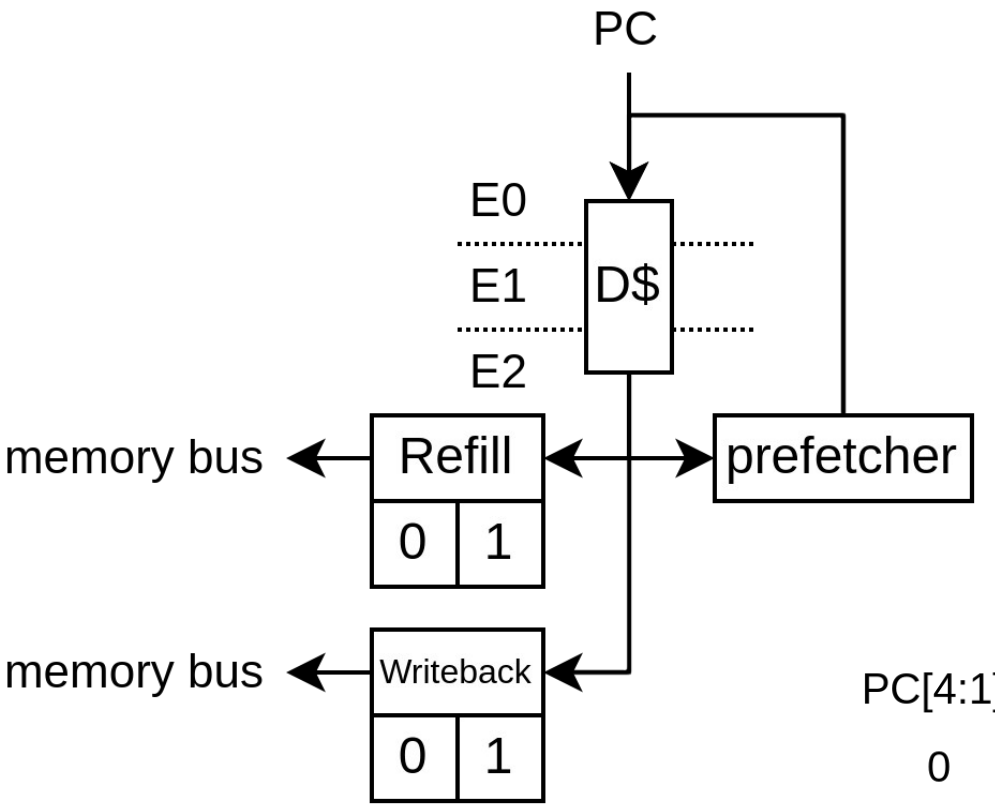


I$ prefetcher

- On I$ miss
- - prefetch next line
- On I$ accessing the last prefetched address
- - prefetch next line



D$ prefetcher



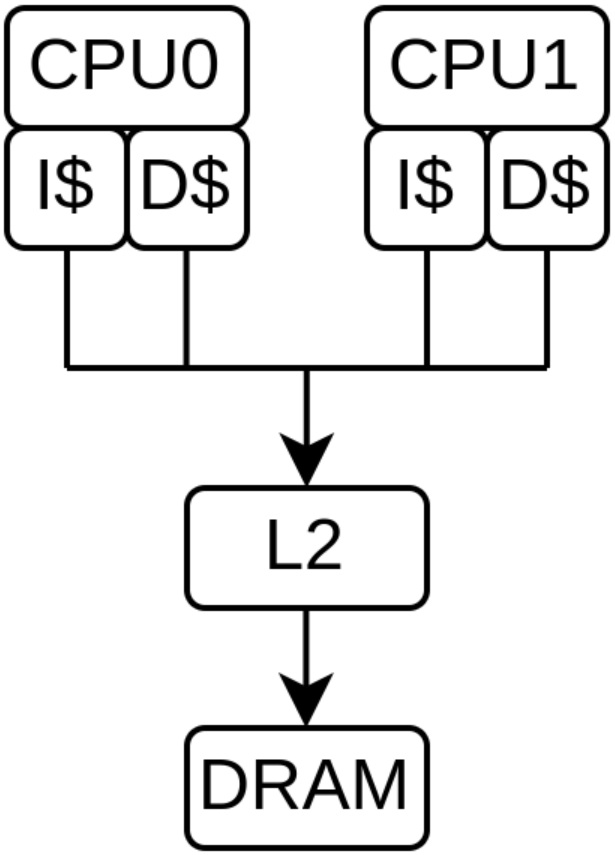
Write speed: 168.4MiB/s
Read speed: 113.3MiB/s

Write speed: 250.5MiB/s
Read speed: 422.9MiB/s

PC[4:1]	tag	address	stride	score	advance
0					
1					
2					
15					

Memory system

- Memory coherency
- Out of order
- Tilelink



Looking for contributions

- Already a few
  - RVB (Andreas Wallner)
  - Compact divider (Thomas Kramer)
- Looking for help
  - Features additions
  - Performance improvements
  - Testing
  - ASIC port
  - …
- https://github.com/SpinalHDL/VexiiRiscv
- https://github.com/SpinalHDL/VexiiRiscv/tree/dev/doc/litex/debian
- Thanks