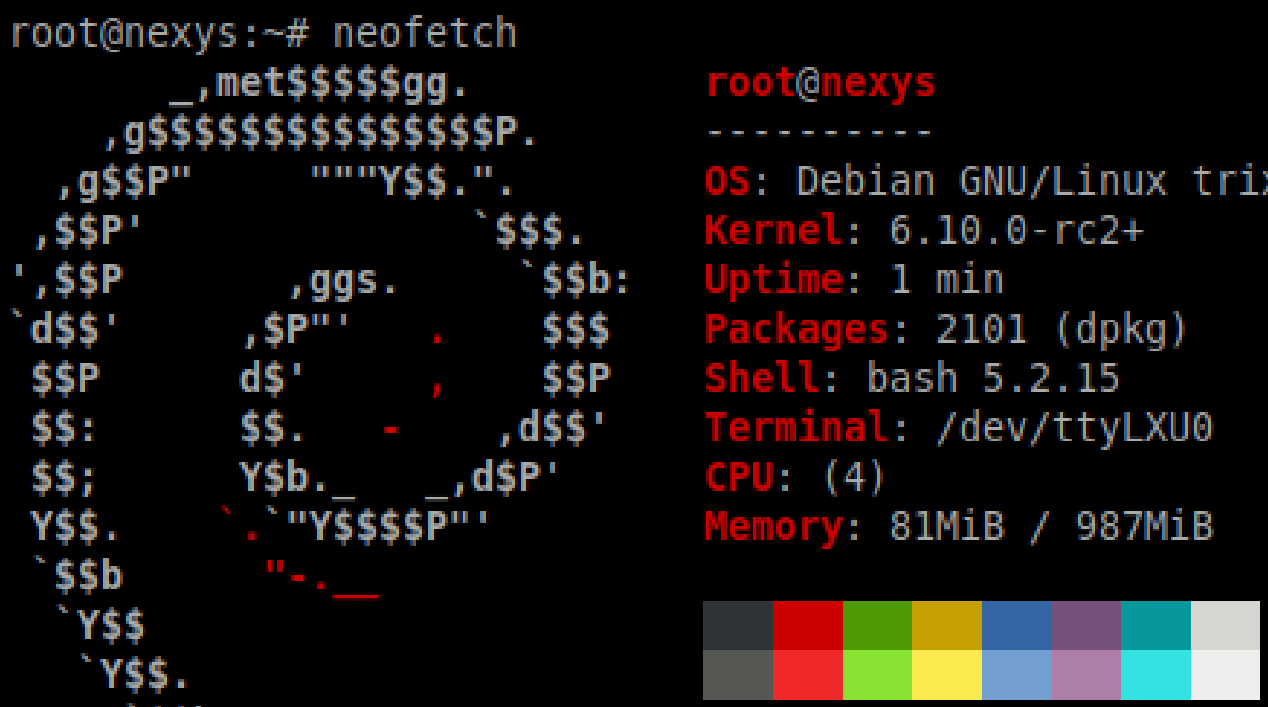
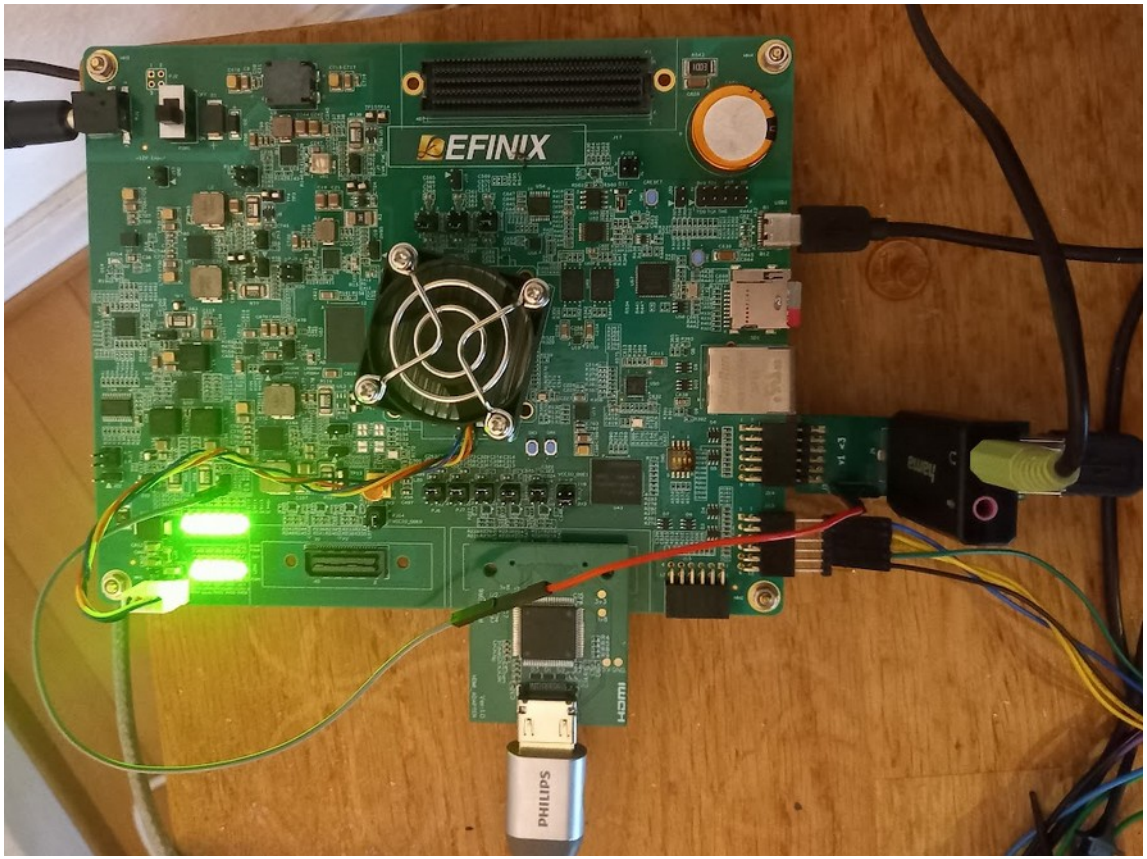
VexiiRiscv : A Debian demonstration



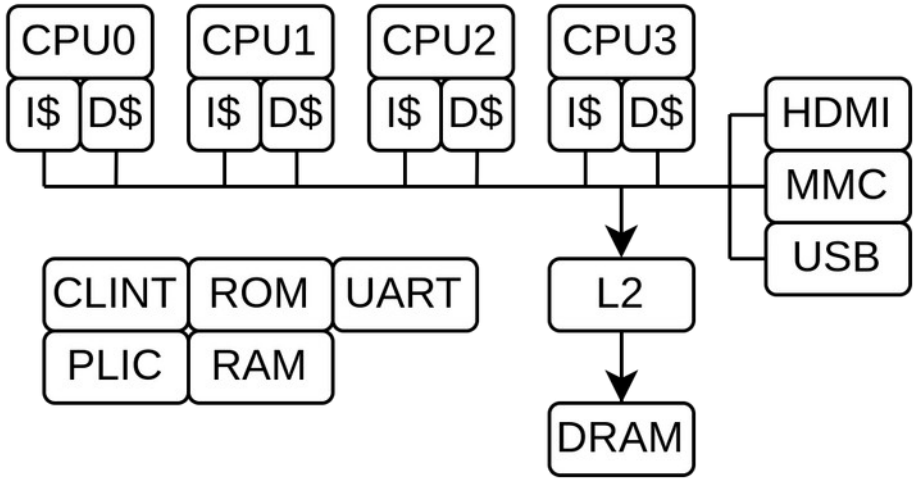
Whoami (FPGA + Board)

- Efinix Titanium Ti375 C529 Development Kit



https://github.com/SpinalHDL/VexiiRiscv/issues/24

Whoami (SoC)



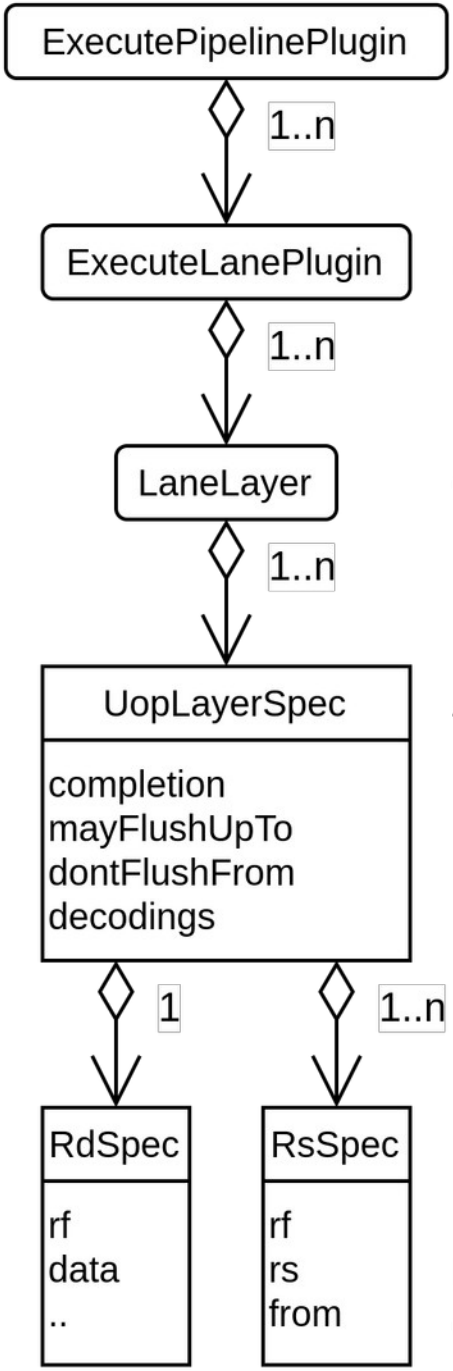
- 4x VexiiRiscv @ 200MHz
  - RV64GC...
  - Single issue / in-order
  - BTB / GShare / RAS
  - Store buffer
  - Hardware prefetcher / non-blocking caches (I$ D$)
  - 16KB I$, 16KB D$ (per core)
- L2 (512KB, non-blocking, out-of-order)
- Tilelink bus (128 bits, memory coherent)
- SpinalHDL + Litex → Verilog

```
EFX_ADD          :   8679
EFX_LUT4         :   87660
   1-2  Inputs   :   12009
   3    Inputs   :   34680
   4    Inputs   :   40971
EFX_DSP48        :   68
EFX_FF           :   56329
EFX_SRL8         :   106
EFX_RAM10        :   1284
```

VexiiRiscv feature set

- Mainly :
  - RV32/RV64, optional MAFDCBSU
  - Can run linux / buildroot / Debian
  - Optional multi-issue
  - Optional late-ALU
  - Up to 5.24 coremark/Mhz 2.50 dhystone/Mhz
  - Free / open-source
- Aswell :
  - Optional I$ D$
  - Optional BTB / RAS / Gshare branch prediction
  - RISC-V official jtag debug
  - ...

Hardware description



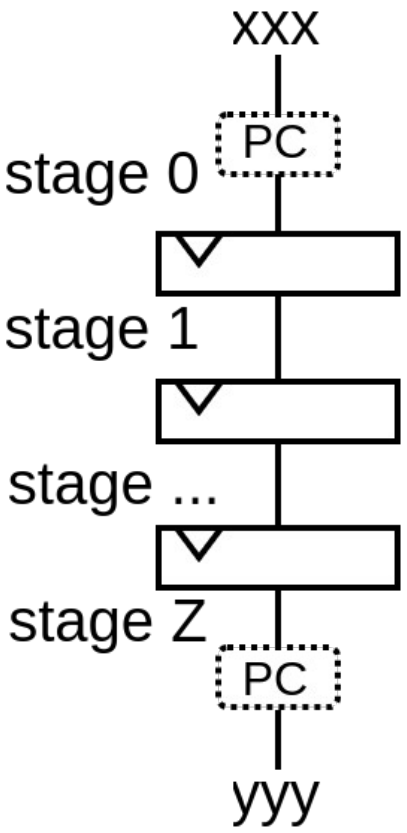
lane0 + lane1 (For a dual issue CPU)

earlyAlu0 + lateAlu0 (in lane 0)

ADD, OR, LW, SW, ...

IntRegFile
RS1
execute[0]

```
stage(0)(PC) := xxx
yyy := stage(Z)(PC)
```




```
plugins += new execute.fpu.FpuSqrtPlugin(early0)
```

Contributions

- Already a few
  - RVB (Andreas Wallner)
  - Compact divider (Thomas Kramer)
- Looking for help
  - Features additions
  - Alternative implementations
  - Performance improvements
  - Testing
  - targeted implementations (ASIC)
  - …
- https://github.com/SpinalHDL/VexiiRiscv
- Thanks NLnet