1.) Mips code snippet

a.) The hazards are in lines 2 and 3; 6@2.5

b.)

```
 loop:
addi $t0,$t0, 4
lw $s0, 60($t0)
lw $v0, 0($t0)
bne $s0, $0, loop
sw $v0, 20($t0)
```

c.)

it is faster for clock speeds to have all processes execute when there is an open spot available.
Makes sure the time through executions is proportional so there will be no interruptions
Decreases the access time of memory

d.)

	Instructions/Program	Cycles/Instruction	Seconds/Cycle
Reducing the number of registers in the ISA	- = **+**	- = **+**	**-** = +
Adding a branch delay slot	- = **+**	**-** = +	- **=** +
Merging the Execute and Mem stages (loads and stores use an additional adder to calculate base+offset)	**-** = +	- = **+**	- = **+**
Changing the implementation from a microcoded CISC machine to a RISC pipeline	- **=** +	**-** = +	- **=** +

2.)

a.)

2nd Cycle	lw r1,0(r1)	WB							
2nd Cycle	lw r1,0(r1)	EX	MEM	WB					
2nd Cycle	Beq r1,r0,loop	ID	X	EX	MEM	WB			

3rd Cycle	lw r1,0(r1)	IF	X	ID	EX	MEM	WB		
3rd Cycle	Add r1, r1, r2			IF	ID	X	EX	MEM	WB
3rd Cycle	lw r1,0(r1)				IF	X	ID	EX	MEM
3rd Cycle	lw r1,0(r1)						IF	ID	X
3rd Cycle	Beq r1,r0,loop							IF	X

b.)

8 clock cycles per loop

Can not use all stages or there are no clock cycles

3.)

a.)

Word Address	Binary Address	Tag	Index	Hit(H)/Miss(M)
3	0000 0011	0	3	M
180	1011 0100	11	4	M
43	0010 1011	2	11	M
2	0000 0010	0	2	M
191	1011 1111	11	15	M
88	0101 1000	5	8	M
190	1011 1110	11	14	M
14	0000 1110	0	14	M
181	1011 0101	11	5	M
44	0010 1100	2	12	M
186	1011 1010	11	10	M
253	1111 1101	15	13	M

b.)

Word Address	Binary Address	Tag	Index	Hit(H)/Miss(M)
3	0000 0011	0	1	M
180	1011 0100	11	2	M
43	0010 1011	2	5	M
2	0000 0010	0	1	H
191	1011 1111	11	7	M
88	0101 1000	5	4	M
190	1011 1110	11	7	H
14	0000 1110	0	7	M
181	1011 0101	11	2	H
44	0010 1100	2	6	M
186	1011 1010	11	5	M
253	1111 1101	15	6	M

c.)
C2 is the best (educated guess)
d.)

4.)
a.) $\frac{2^5}{2^2}$ = 8 words
b.) 2^5 = 32 entries
c.) data = 256 bits, tag is 22 bits, valid is 1 bit ~> cache per block is 279 ~> 279/256 = 1.09

d.)

Address	Index	Offset	Hit/Miss	Replace	Final Value
0	00000	00000	M	N	N
4	00000	00100	H	N	N
16	00000	10000	H	N	N
132	00100	00100	M	N	N
232	00111	01000	M	N	Y
160	00101	00000	M	N	Y
1024	00000	00000	M	Y	N
30	00000	11110	M	Y	N
140	00100	01100	H	N	N
3100	00000	11100	M	Y	Y
180	00101	10100	H	N	Y
2180	00100	00100	M	Y	Y

There are four replace blocks

e.)
References = 12
Hits = 4
4/12 = 0.33