Topic 14: Sequential logic devices

Thursday, January 31, 2019 4:27 PM

I. Sequential circuits

- **Combinational logic:** the present output is function of present inputs, but independent of the states of the circuit at previous moment.
  e.g. decoder, encoder, multiplexer, demultiplexer, magnitude comparator, parity generator/checker, Half adder, full adder…
- **Sequential circuit:** a digital circuit whose output depends not only on the present combination of inputs, but also on the history of the circuit.
  e.g. latches, flip-flops, counters, registers

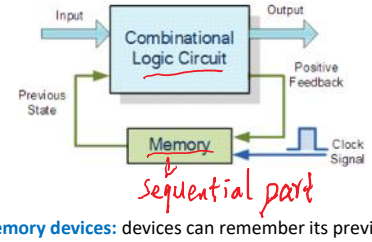
Q1: You are on the 3rd floor and want to go to the 6th floor:

a. **If the elevator is on the 1st floor, how will it operate?**
b. **If the elevator is on the 4th floor, how will it operate?**
c. **If the elevator is on the 5th floor, but someone on the 6th floor press down button before you did, how will it operate?**

Answer the questions and fill your results in the table below

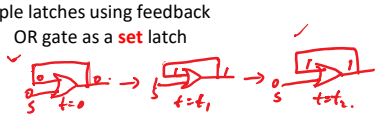
Input	present state	movement
Up	1	Up
Up	4	Down
Up	5	up

- Block diagram of a typical sequential circuit (state machine)

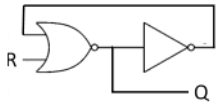


II. Basic latches

- **Main memory devices:** devices can remember its previous states
  e.g. latches and flip-flops
- **Latch:** a sequential circuit with two inputs: SET and RESET, which make the latch store a logic 0 (reset) or 1 (set) until actively changed.
- Simple latches using feedback
  - OR gate as a **set** latch



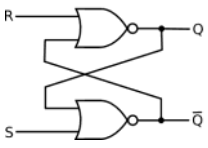
Q2: NOR--NOT gate as a reset latch

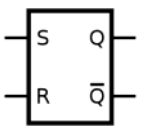


a. **When both inputs of NOR is 0, what is the value of Q?**
b. **What happens to Q if R=1?**
c. **What happens to Q if R=0 again?**

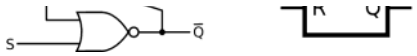
What is your conclusion?

- Set-reset (SR) latch: NOR gate latch (active-high latch)



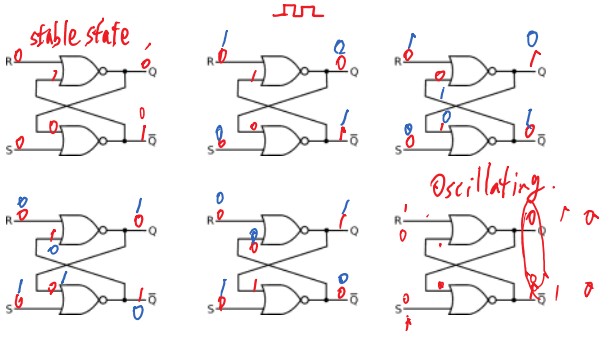


Generate the state excitation table of a SR latch

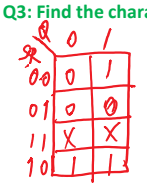


Generate the state excitation table of a SR latch

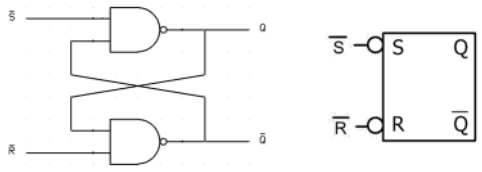
Q_n	S	R	Q_{n+1}	Comment
0	0	0	0	not change (NC)
0	0	1	0	reset
0	1	0	1	set
0	1	1	X	unused
1	0	0	1	NC
1	0	1	0	reset
1	1	0	1	set
1	1	1	X	unused



Q3: Find the characteristic equation for the next state using k-map.



- SR latch using NAND gate (active-low SR latch)



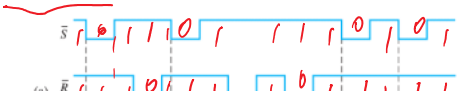
Q: Generate the state excitation table of a SR latch

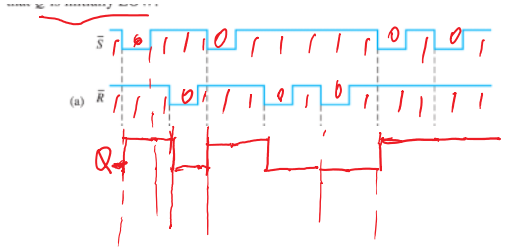
Q_n	$\bar{S}$	$\bar{R}$	Q_{n+1}	Comment
0	0	0	X	unused
0	0	1	1	set
0	1	0	0	reset
0	1	1	0	NC
1	0	0	X	unused
1	0	1	1	set
1	1	0	0	reset
1	1	1	1	NC

Q4: Find the characteristic equation for the next state using k-map.

Q5: The timing diagram of SR latch

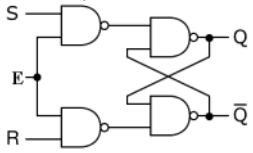
If the $\bar{S}$ and $\bar{R}$ waveforms in Figure 7–5(a) are applied to the inputs of the latch in Figure 7–4(b), determine the waveform that will be observed on the Q output. Assume that Q is initially LOW.

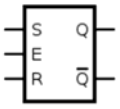




III. Gated latches

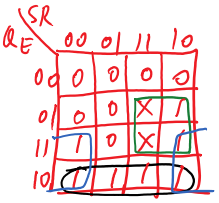
1. Gated SR latch (SR latch with **enable** function)





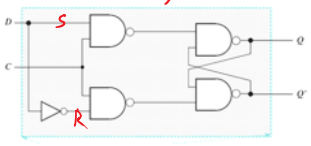
Generate the state excitation table of gated SR latch

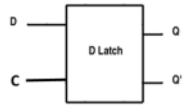
E	S	R	Q_{n+1}	Comment
0	X	X	Q_n	hold
1	0	0	Q_n	NC
1	0	1	0	reset
1	1	0	1	set
1	1	1	X	unused



Characteristic equation: $Q_{n+1} = Q(R' + E') + ES$

2. Gated D latch (D → delay)





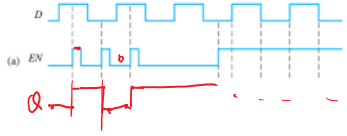
Generate the state excitation table of gated D latch

E	D	Q_{n+1}	Comment
0	X	Q_n	hold
1	0	0	reset
1	1	1	set

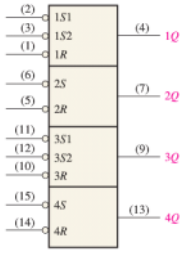
Characteristic equation: $Q_{n+1} = E'Q + ED$

Q6:

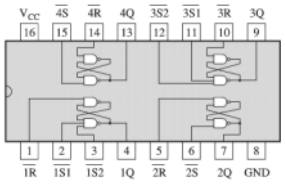
Determine the Q output waveform if the inputs shown in Figure 7–11(a) are applied to a gated D latch, which is initially RESET.



- Commercial products
  - Quad SR latch module -- 74HC279

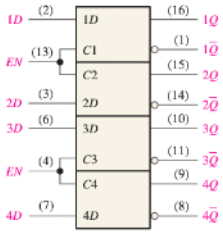


(a) Logic diagram



(b) Pin diagram

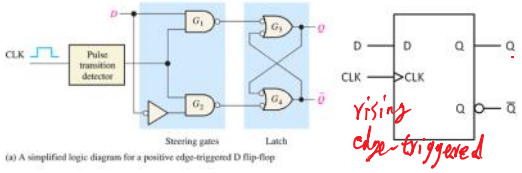
  - Quad D latch module -- 74HC75



IV. Basic flip-flops

- **Flip-flop:** an edge-triggered circuit, whose output changes when its **CLOCK** input receives an edge.
- **CLOCK (CLK):** an enabling input to a sequential circuit that is sensitive to the positive or negative-going edge of a waveform
  - Periodic
  - 50% duty cycle
  - Allow the FFs (flip-flops) to change state on its rising/falling edges.

- Enable of latch circuit: level sensitive;
- **Edge-triggered D flip-flop:**



(a) A simplified logic diagram for a positive edge-triggered D flip-flop

Operation I:

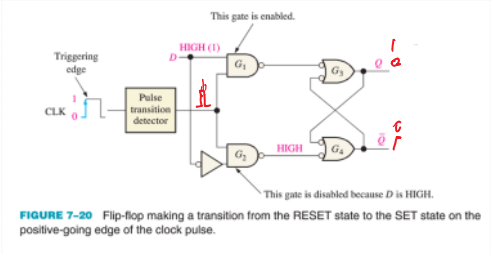


FIGURE 7–20 Flip-flop making a transition from the RESET state to the SET state on the positive-going edge of the clock pulse.

Operation II:

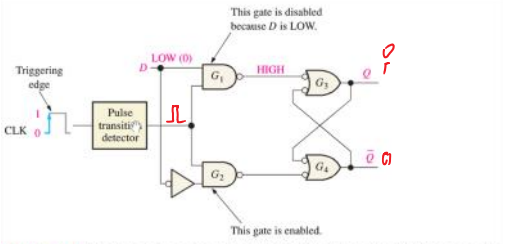
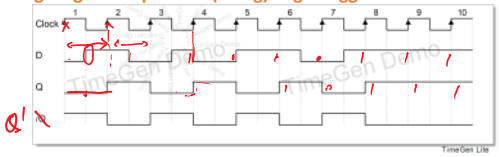


FIGURE 7–21 Flip-flop making a transition from the SET state to the RESET state on the positive-going edge of the clock pulse.

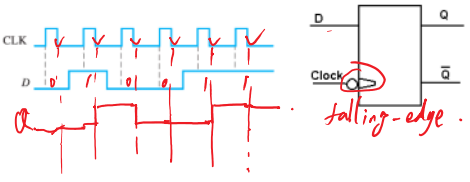
State excitation table

Clk	D	Q_{n+1}	comment
not↑	X	Q_n	hold
↑	0	0	reset
↑	1	1	set

Timing diagram of positive (rising) edge-triggered DFF:



Timing diagram of negative (falling) edge-triggered DFF (Q=0 initially):



- Commercial product: SN7474 dual positive-edge-triggered DFF

SN7474 dual positive-edge-triggered D Flip-Flop

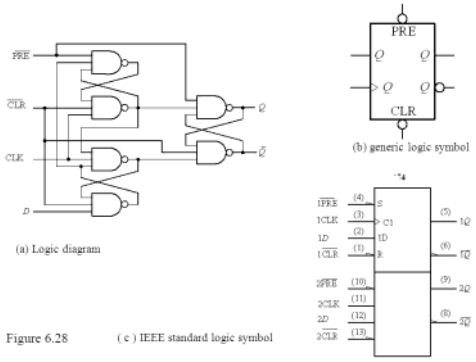
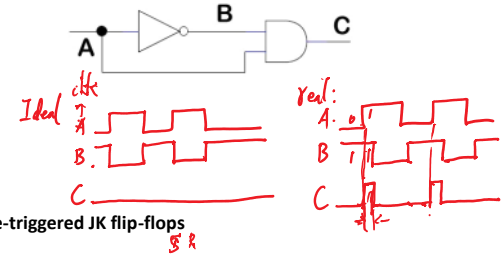
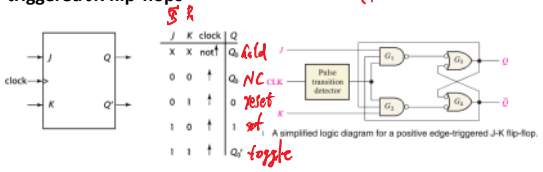


Figure 6.28

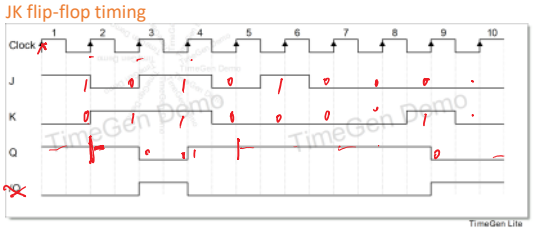
About pulse transition (edge) detector circuit:



- **Edge-triggered JK flip-flops**

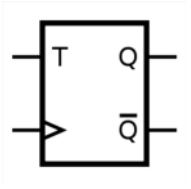


JK flip-flop timing



- **Edge-triggered T (toggle) flip-flop**

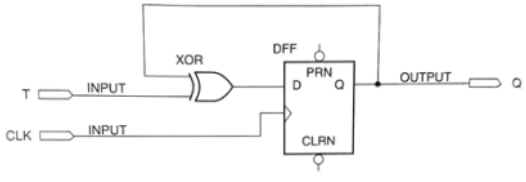
  Definition: a flip-flop whose output toggles between HIGH and LOW states on each applied clock pulse when the T input is active



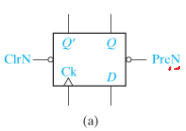
CLK	T	Q_{t+1}	Function
↑	0	Q_t	No change
↑	1	$\bar{Q}_t$	Toggle
0	X	Q_t	Inhibited
1	X	Q_t	Inhibited
↓	X	Q_t	Inhibited

hold

Realize T flip-flop using D flip-flop:



- **Flip-flops with additional inputs**
  - Asynchronous preset and clear

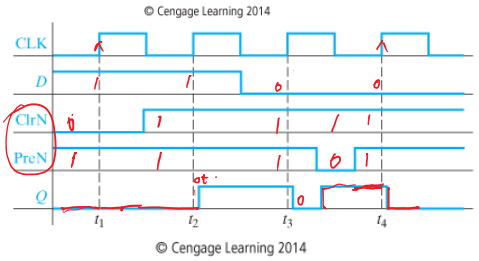


Ck	D	PreN	ClrN	Q^+
x	x	0	0	(not allowed)
x	x	0	1	1
x	x	1	0	0
↑	0	1	1	0
↑	1	1	1	1
0,1,↓	x	1	1	Q (no change)

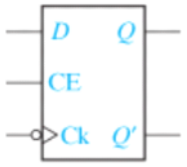
(b)

		0,1,↓	x	1	1	Q (no change)

(a) (b)



- Asynchronous clock enable



(b) D-CE symbol

ck	D	CE	Q^+	
X	x	0	Q_n	hold
↓	0	1	0	
↓	1	1	1	
Not↓	X	1	Q_n	NC

V. Latch vs. flip-flop

- Flip-flop is more favorable in sequential circuits
- Any unwanted change in the input could be passed to output in the latch
- e.g.