**Exam1**

**Name:YixinWang Class:34071901**

**CQUPT ID:2019214850 NAU ID:6010063**

**a. SV code without comments**

module dec3to8 (

input logic EN,

input logic [2:0] ABC,

output logic [7:0] Y

);

always\_comb begin

if(EN==0) Y=8'b 0;

else begin

case(ABC)

3'b 000: Y=8'b 0000\_0001;

3'b 001: Y=8'b 0000\_0010;

3'b 010: Y=8'b 0000\_0100;

3'b 011: Y=8'b 0000\_1000;

3'b 100: Y=8'b 0001\_0000;

3'b 101: Y=8'b 0010\_0000;

3'b 110: Y=8'b 0100\_0000;

3'b 111: Y=8'b 1000\_0000;

default: Y=8'b 0;

endcase

end

end

endmodule

module dec3to8\_tb(

input logic [3:0] SW,

output logic [7:0] LEDR

);

dec3to8 dec3to8\_u(

.EN (SW[3]),

.ABC (SW[2:0]),

.Y (LEDR[7:0])

);

endmodule

**b. Modelsim “do” file**

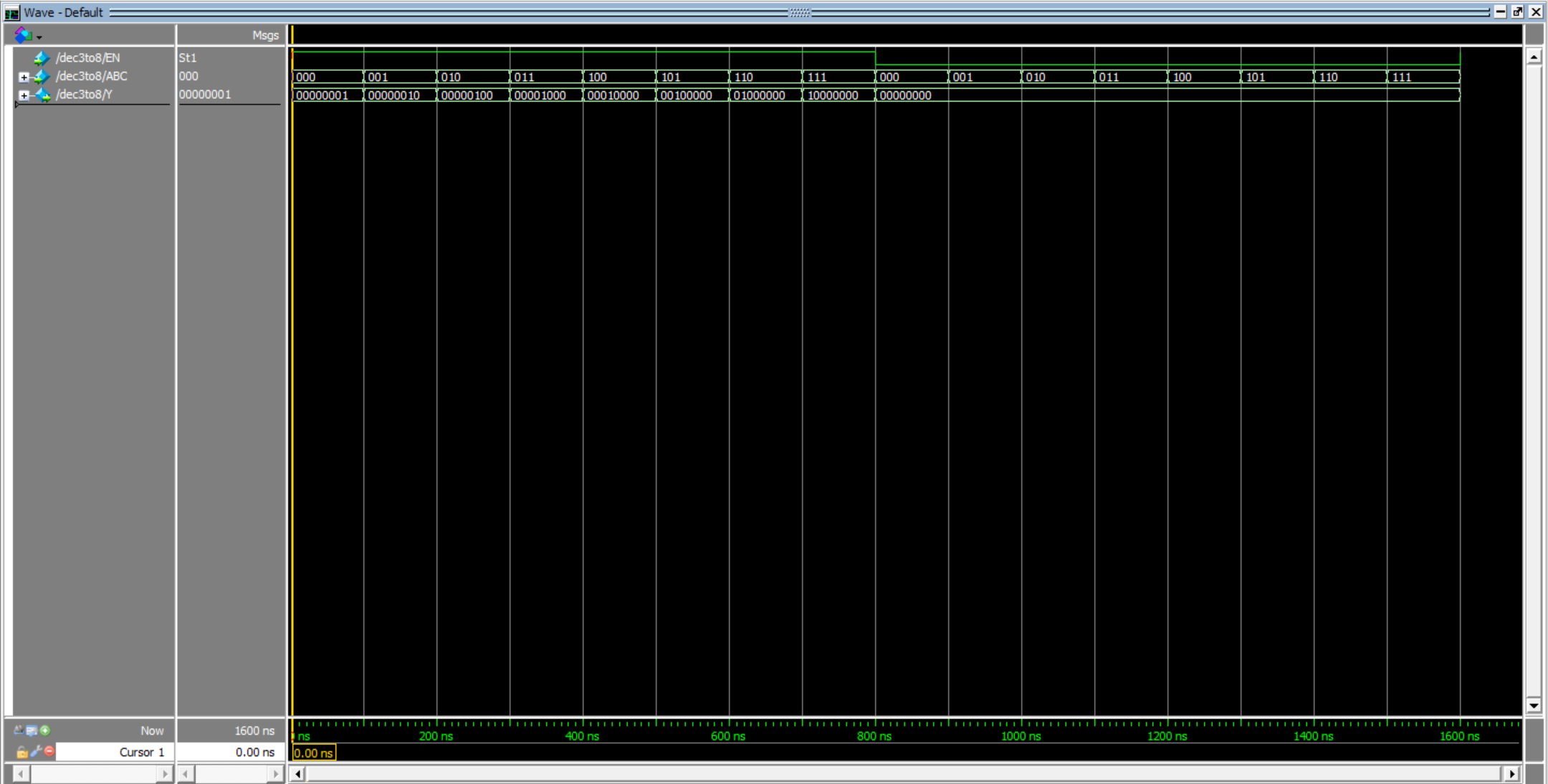
restart -f

force EN 1 0ns, 0 800ns -r 1600ns

force ABC 000 0ns, 001 100ns, 010 200ns, 011 300ns, 100 400ns, 101 500ns, 110 600ns, 111 700ns -r 800ns

run 1600ns

**c. Full simulation waveform**

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