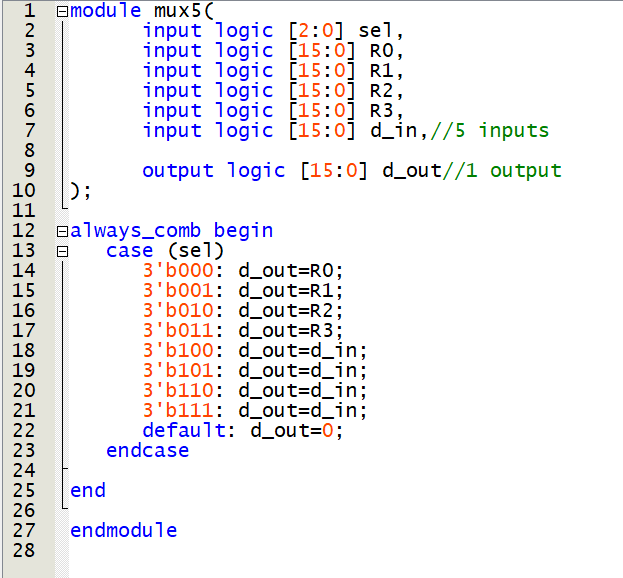
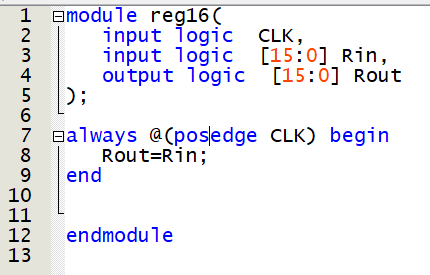
**Exam2**

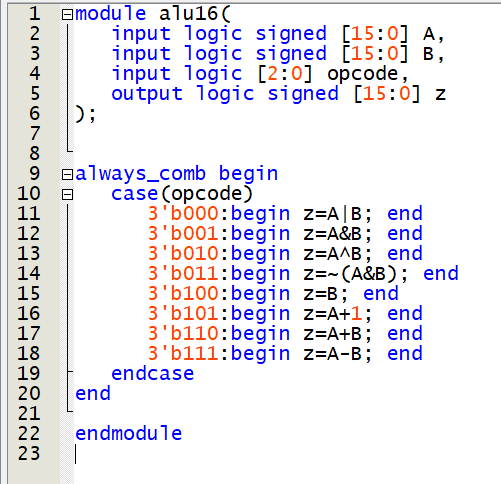
**1.SV for the 5-to-1 16-bit bus Mux**

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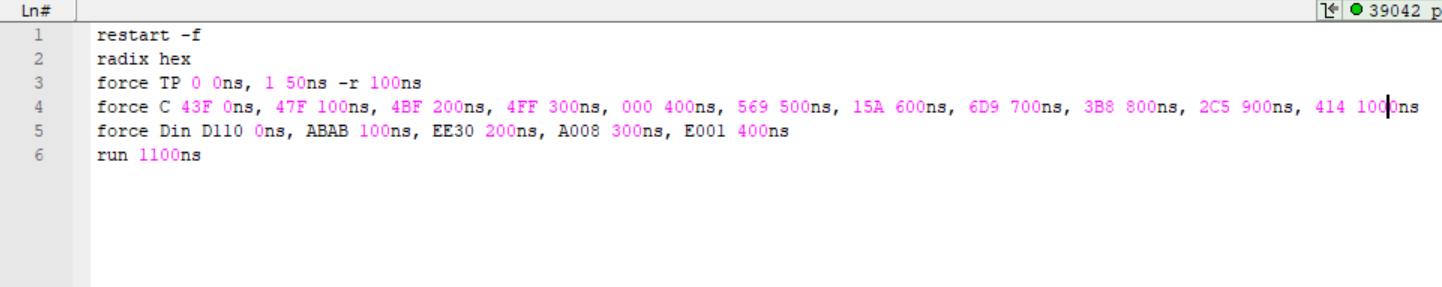
**2.SV code for the 16-bit register**

****

**3.SV code for the 16-bit ALU**

****

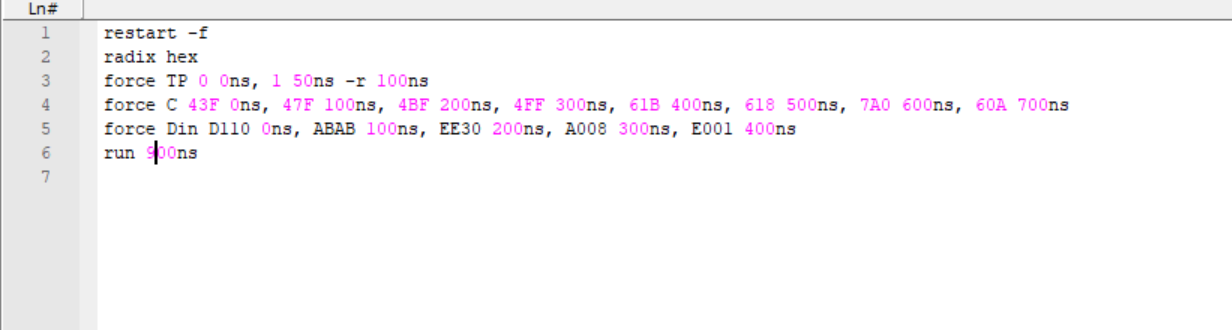
**4.ModelSim do file for part Ⅲ**

****

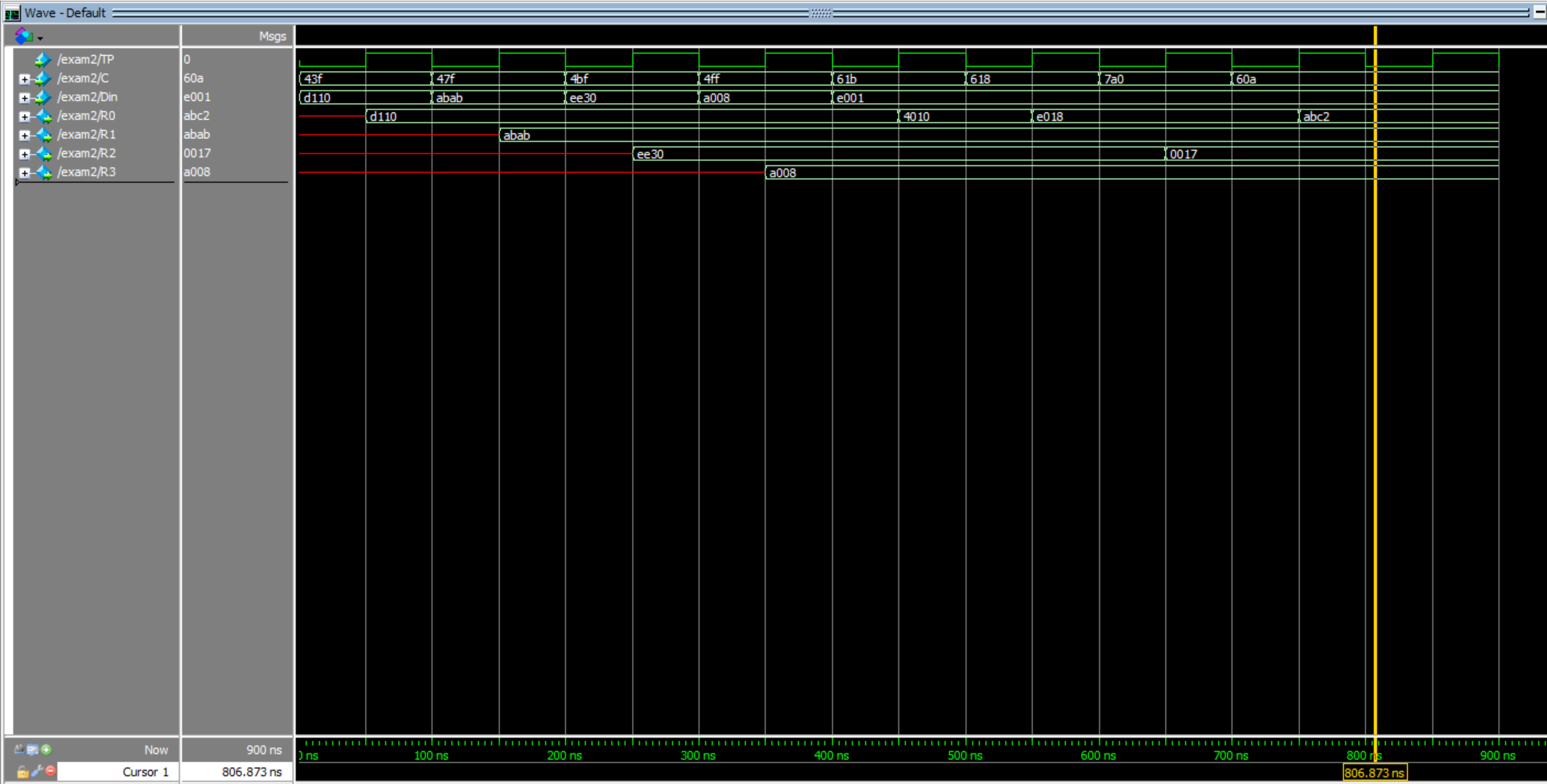
**5.Simulated waveform for part Ⅲ**

****

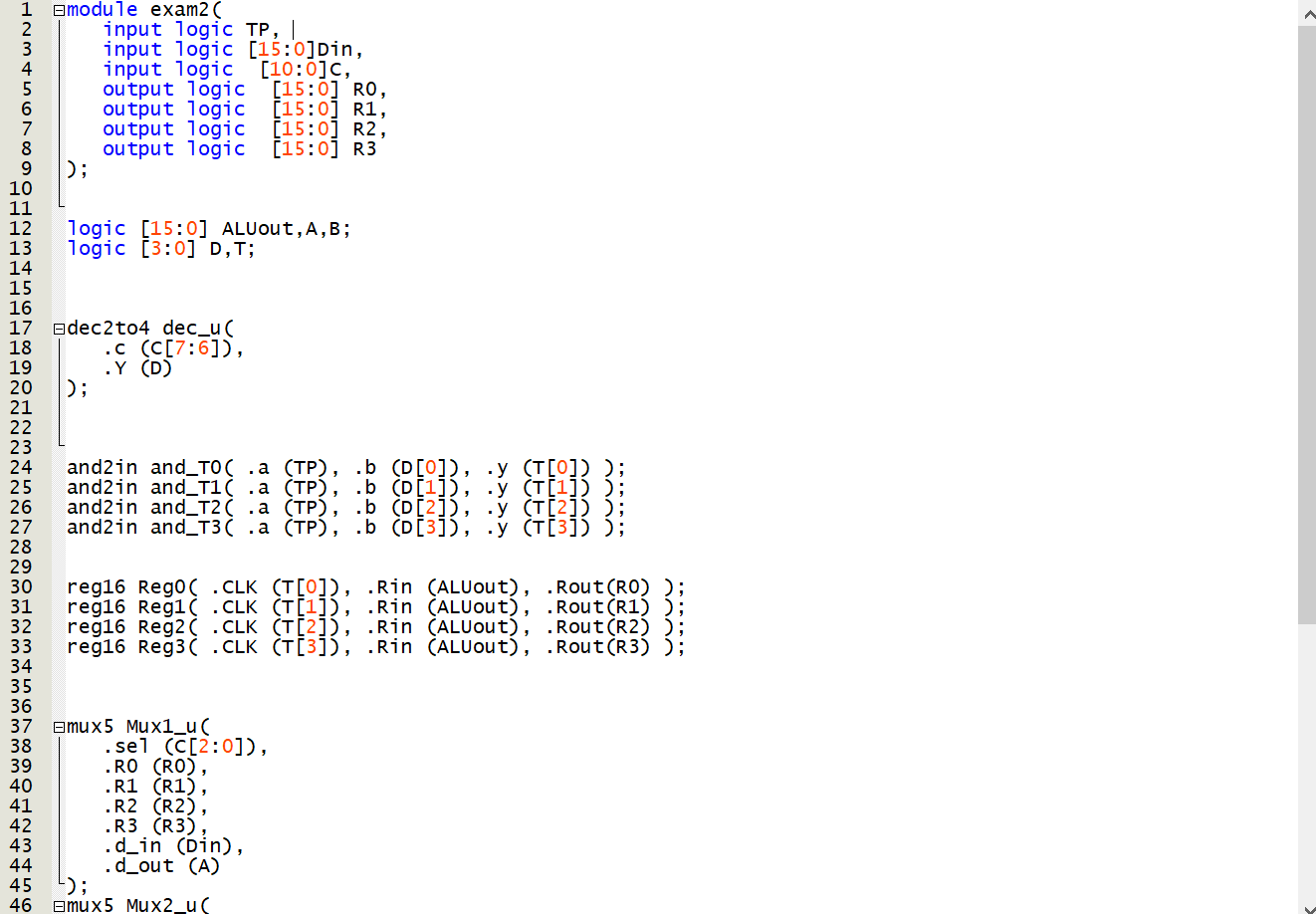
**6.ModelSim do file for part Ⅳ**

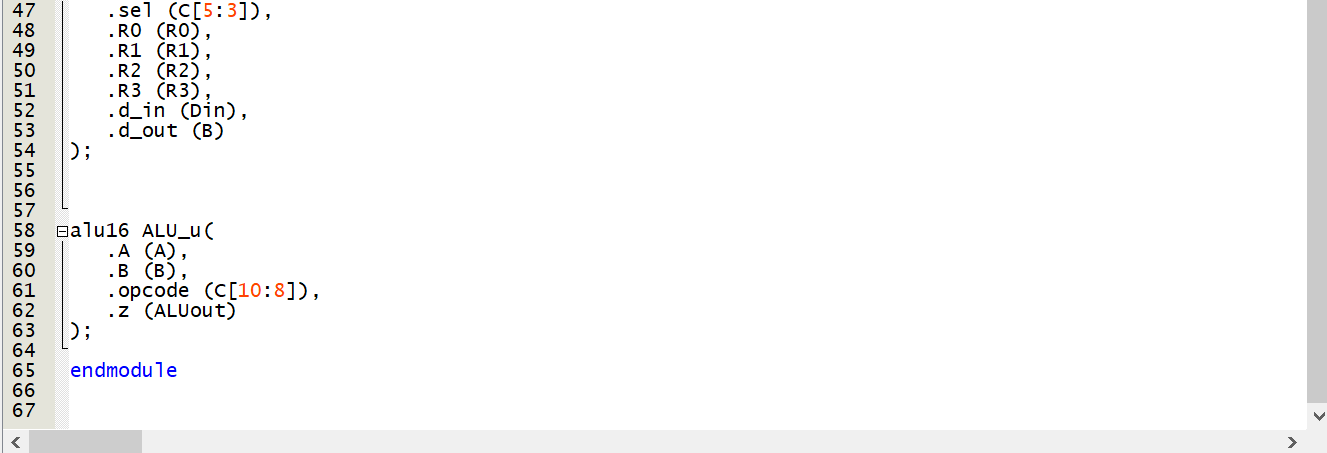
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**7.Simulated waveform for part Ⅳ**

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**The code of up3\_16.v (I named it exam2.v)**

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