**Exam 2 rules and tips:**

1. Read and understand everything in this pre-exam document.
2. On the exam day, bring only this file and lab report of lab4, 5 and 7. No other materials are allowed
3. You would like to rework every step from lab3-7 by yourself if you always let your partner to do the programming and simulation! (strongly recommended)
4. No cell phone, laptop or any electronic device during the exam.

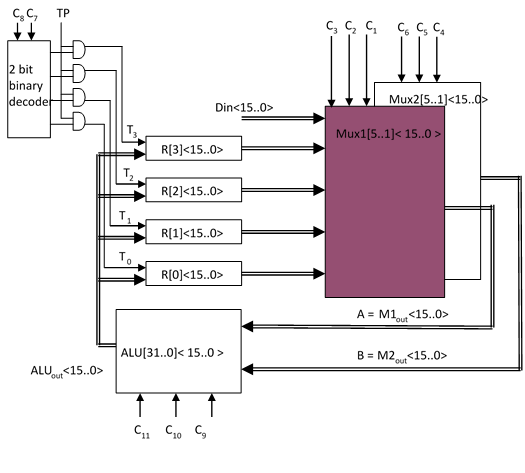
**Pre-exam 2 questions A:**

Below is a very simple microprocessor architecture. For the following control signals:

1. TP is the system clock signal connected to the registers through the **AND** gates;
2. are the clock input for each register, respectively, and all registers load the input data at the rising edge;
3. are the inputs for the 2-to-4 decoder which will enable only one AND gate at any time;
4. and are used to select source register R[0]-R[3], and is used for selection: If , MUX1 output is , if , MUX2 output is ;
5. are used for ALU selection, and the details are listed in the following table.

**Note: assume that the signals can pass all the components instantly.**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
| Operation | A AND B | A OR B | A XOR B |  | A+B | A-B | **2\*A** | B |
| Comment | Bitwise and | Bitwise or | Bitwise xor | Bitwise not AB | Addition | multiplication | 2 times data A | Pass data B |



**Operation examples:**

1. Load a data into one of the registers:

**Comments:** select the function B for ALU; will set the output of the decoder to 1 so that the TP signal can be passed to R[3]; means the output of MUX2 would be , which will pass the data on through the ALU. means don’t care value.

1. Add the data stored in one registers to the input data and store the result in the third register:

**Comments:** select the function A+B for ALU; will set the output of the decoder to 1 so that the TP signal can be passed to R[0]; means the output of MUX2 would be and means the output of MUX1 would be data from ; means don’t care value.

**Practice problems: What control signals should be used for the following operations? How many clock cycles will it take to complete the operation?**

100001XX001 1 clock cycle

101011XX011 1 clock cycle

110100XX000 1 clock cycle

111111XXXXX 1 clock cycle

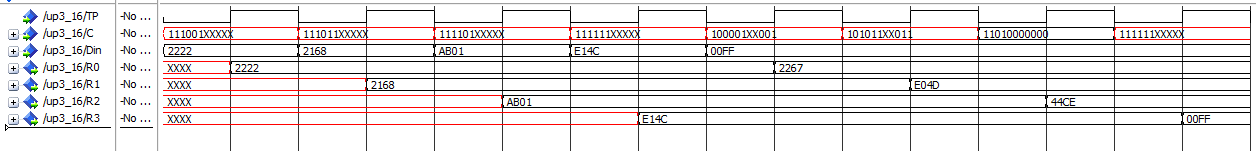
000001XX000 1 clock cycle

001011XX001 1 clock cycle

010101XX010 1 clock cycle

01111011000 1 clock cycle

**Practice problem: timing diagram**



Can you recognize the operation at each TP rising edge? (CX means the Xth clock cycle)

C1: C2: C3: C4:

C5: C6: C7: C8:

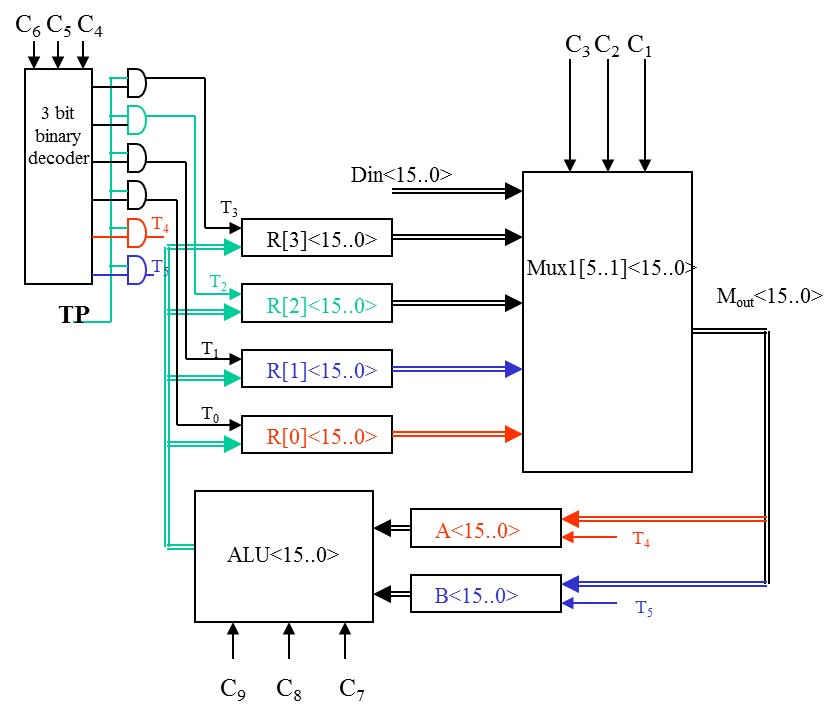
Check the data to verify your answers. (be aware that the operation would be successive, which means you should always use the updated data in the registers)

**Pre-exam 2 questions B:**

Below is a very simple 16-bit microprocessor architecture. For the following control signals:

1. TP is the system clock signal connected to the registers through the **AND** gates;
2. are the clock input for each register, respectively, and all registers load the input data at the rising edge;
3. are the inputs for the 3-to-6 decoder which will enable only one AND gate at any time;
4. are used to select source register R[0]-R[3], is used for selection: If , MUX1 output is .
5. are used for ALU selection, and the details are listed in the following table.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Control  signal | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
| Operation | A+B | A-B | 2\*A | A | A AND B | A OR B | A XOR B |  |
| Comment | Addition | multiplication | 2 times data A | Pass data A | Bitwise and | Bitwise or | Bitwise xor | Bitwise not AB |



**Operation examples:**

1. Load a data into one of the registers:

**Clock cycle 1** ---

**Comments:** will set the output of the decoder to 1, which will select the register A; selects as data source for MUX, and the data will be stored in register A at rising edge. means don’t care value.

**Clock cycle 2** ---

**Comments**: select the function A for ALU. At the 2nd rising edge, data stored in register A will pass ALU and be stored into .

1. Add the data stored in one registers to the input data and store the result in the third register:

**Clock cycle 1** ---

**Comments:** will set the output of the decoder to 1, which will select the register A; selects as data source for MUX, and the data will be stored in register A at rising edge.

**Clock cycle 2 ---**

**Comments:** select the function A+B for ALU; will set the output of the decoder to 1, which will select the register B; selects as data source for MUX, and the data will be stored in register B at rising edge. means don’t care value.

**Clock cycle 3** ---

**Comments:** select the function A+B for ALU; will set the output of the decoder to 1, which will select the register R[0]; means don’t care value.

**Practice problems: What control signals should be used for the following operations? How many clock cycles will it take to complete the operation?**

XXX100001 1 clock cycle

XXX1011XX 1 clock cycle

000000XXX 1 clock cycle total 3 clock cycles

XXX100011 1 clock cycle

XXX1011XX 1 clock cycle

001001XXX 1 clock cycle total 3 clock cycles

XXX100000 1 clock cycle

010010XXX 1 clock cycle total 2 clock cycles

XXX1001XX 1 clock cycle

011011XXX 1 clock cycle total 2 clock cycles

XXX100000 1 clock cycle

XXX1011XX 1 clock cycle

100000XXX 1 clock cycle total 3 clock cycles

XXX100001 1 clock cycle

XXX1011XX 1 clock cycle

101001XXX 1 clock cycle total 3 clock cycles

XXX100010 1 clock cycle

XXX1011XX 1 clock cycle

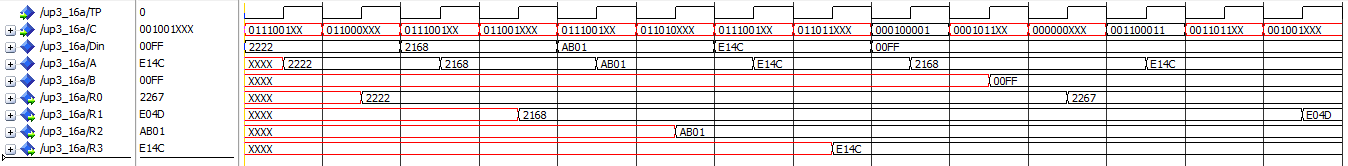
110010XXX 1 clock cycle total 3 clock cycles

XXX100000 1 clock cycle

XXX101011 1 clock cycle

111011XXX 1 clock cycle total 3 clock cycles

**Practice problem: timing diagram**



Can you recognize the operation at each TP rising edge? (CX means the Xth clock cycle)

C1: C2: C3: C4:

C5: C6: C7: C8:

C9: C10: C11:

C12: C13: C14:

Check the data to verify your answers. (be aware that the operation would be successive, which means you should always use the updated data in the registers)