EE 215 Homework 8

(3 problems, 60 pts total)

1. Communications definitions. (20 pts)
   Use sentences to describe the difference between:

   a. serial and parallel?
   b. synchronous and asynchronous?
   c. bus controller and contention?
   d. Duplex and half duplex?
   e. Master and slave?

Answers:

a. Serial communication employs a single wire to transmit data bits sequentially, while parallel communication utilizes multiple wires for simultaneous data transmission, enhancing efficiency.

b. Synchronous communication, leveraging a clock, ensures precisely timed data exchanges, whereas asynchronous communication operates without a clock, allowing for more flexible and unpredictable timing.

c. A bus controller serves as the authority determining communication access, whereas contention arises when multiple users independently vie for control without a centralized directing entity.

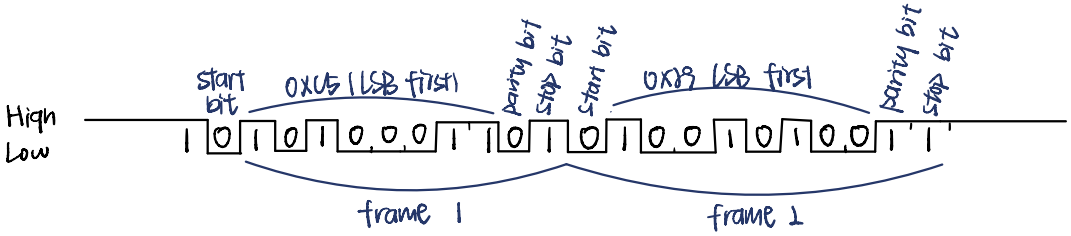
d. Duplex communication, or full duplex, facilitates simultaneous two-way communication , whereas half duplex supports one-way communication at a time on a singular medium, introducing a sequential aspect.

e. The master device orchestrates communication, supplying signals and a clock, while the slave device, especially in synchronous systems, reacts to the master's signals without necessitating its clock, establishing a hierarchical relationship.

2. UART (20 pts)

Draw the UART protocol data exchange for the data (0x C5, 0x 29) using 8E1 (8 bits of data, even parity, 1 stop bit). Label the frames. If the baud rate is 300 bps, what is the data rate? Why does the receiver have to sample this data?

	quantity of 1	parity bit
0xC5 = 1100 0101 (b).	4	0
0x29 = 0010 1001 (b).	3	1



baud rate = 300 bps

data rate = $300 \times \frac{8 \text{ (used bit)}}{11 \text{ (total bit)}} = 218$ bps

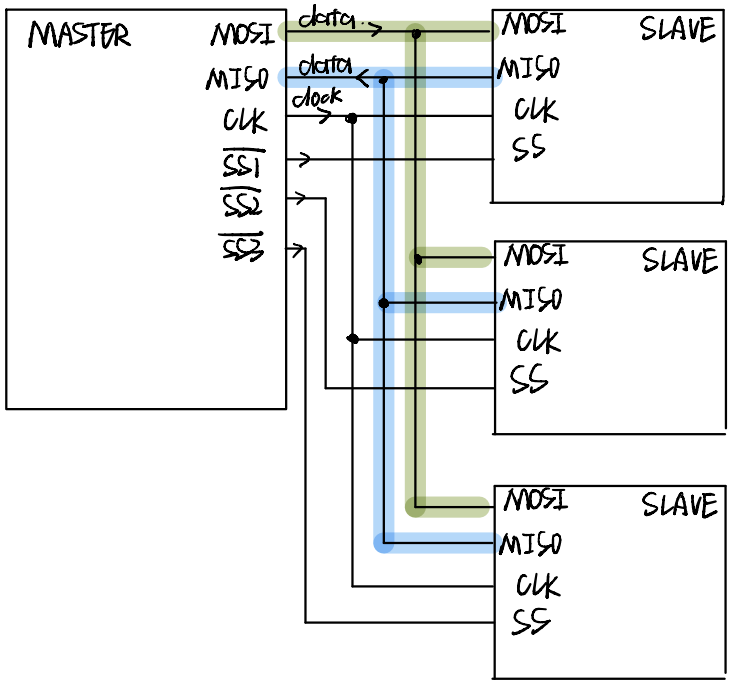
Answers:

Because the receiver doesn't have the clock to recognize the change of the signal. and it has to sample the signal to know when the signals start.

3. SPI (20 pts)

Draw the two possible configurations for one master device and 3 slave devices. Label all wire connections with their names.

① common bus, only selects one of three.



② data through all slaves, cascade, with one SS line at the master only.