Ispit vježba

2 | 2012/2013 TRENUTNI

① ORJ
   MAD

20	20
1	20

REFERENTNI BLOK

```
5  2  21  4  3  15  4  4
1  3  2  10  1  17  6  6
6  4  19  8  8  17  19  9
2  4  1  10  18  1  20  4
4  4  2  2  17  20  1  24
5  0  2  3  3  0  1  15
4  1  1  8  3  0  1  10
4  1  1  3  8  0  1  10
5  1  1  3  8  0  1  2
```

3) $\frac{1}{4}(19 + 10 + 3 + 8)$

$\frac{1}{4}(2 + 19 + 16 + 0)$

MAD_0

1) $MAD_0 = \frac{1}{4}(10 + 2 + 1 + 3) = 4$

$MAD_1 = \frac{1}{4}(16 + 19 + 3 + 16)$

$MAD_2 = \frac{1}{4}(19 + 0 + 17 + 19)$

2) $MAD_n = \frac{1}{4}(10 + 19 + 7 + 12)$

$MAD_2 = \frac{1}{4}(12 + 17 + 2 + 8)$

MAD_0

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② $t = 10s$
$t' = 6s$
$N = 4$

$U = \frac{t}{t'}$

$P = \frac{P}{Q}$

$U = 1,67$

$U = \frac{1}{(1-p) + \frac{P}{N}}$:

$\frac{10}{6} = \frac{1}{1 - p + \frac{P}{4}} = \frac{4}{4 - 3p}$

$5 = \frac{12}{4 - 3p} \Rightarrow 20 - 15p = 12$

$P = \frac{8}{15} = 0,53$

---

③ $N = 2000$ podataka

$t_{uč} = 120 ns$

obrada 1 podatka $t_{pod} = 2ns$

$t_{spr} = 150 ns$

$t_{oč}' = 120 ns$

$t_o = N \cdot t_{pod} = 4000 ns$

$t_u = t_{uč} + t_o + t_{spr} = 4270 ns$

$P(obrada) = \frac{4000}{4270} = 0,9367$

1) $N = 1$

$t_u = 4270, P = 0,9367$

$U = \frac{1}{1 - P + \frac{P}{N}} = 1$

$E = \frac{U}{N} = 1$

2) $N = 2$

$t_u = 4270, P = 0,9367$

$U = \frac{1}{1 - P + \frac{P}{2}} = 1,88$

$E = \frac{U}{N} = 0,94$

3) $N = 4$

(5)

$P_1 = 36\% \quad N = 5$

$P_2 = 65\% \quad N = 3$

$$U_1 = \frac{1}{1-p + \frac{p}{N}} = 1{,}38$$

$$\boxed{U_2 = \frac{1}{1-0{,}65 + \frac{0{,}65}{3}} = 1{,}7\sigma} \quad \bigg| O_2!$$

(6.)

```c
#include <xparameters.h>
#include <xiic.h>

#define I2C_CAMERA 0x40

void main (void){
    u8 readBuffer[1] = {0x00};
    u8 writeBuffer[1] = {0x00};
    u8 realWriteBuffer[2] = {0x00, 0x00};

    XIic i2cInstance;
    XIic_Config *cfgPointer;

    cfgPointer = XIic_LookupConfig(XPAR_CAMERA_IIC_DEVICE_ID); // Ova konstanta je nekakav njegov interni identifikator I2C IP-a

    XIic_CfgInitialize (&i2cInstance, cfgPointer , cfgPointer->BaseAddress);
    XIic_SetAddress (&i2cInstance, XII_ADDR_TO_SEND_TYPE , I2C_CAMERA);

    XIic_Start(&i2cInstance);

    writeBuffer[0] = 0x14;
    Xiic_MasterSend(&i2cInstance, writeBuffer, 1); // Pišemo adresu registra, prazan ciklus pisanja

    XIic_MasterRecv(&i2cInstance, readBuffer, 1); // Dohvaćamo s te adrese
    if(readBuffer[0] & 0x20){ // 176 x 144
        realWriteBuffer[1] = 0x10; // AEC ADRESA
        realWriteBuffer[0] = 0x56; // AEC = 0x56;
        Xiic_MasterSend(&i2cInstance, realWriteBuffer, 2);
    } else { // 352 x 258
        realWriteBuffer[1] = 0x10; // AEC ADRESA
        realWriteBuffer[0] = 0x42; // AEC = 0x56;
        Xiic_MasterSend(&i2cInstance, realWriteBuffer, 2);

        writeBuffer[0] = 0x11;
        Xiic_MasterSend(&i2cInstance, writeBuffer, 1);

        XIic_MasterRecv(&i2cInstance, readBuffer, 1);
        readBuffer[0] &= 0x1F;
        readBuffer[0] /= 2; // Takt /= 2

        realWriteBuffer[1] = 0x11;
        realWriteBuffer[0] = readBuffer[0];
        Xiic_MasterSend(&i2cInstance, realWriteBuffer, 2);
    }

    XIic_Stop(&iic);
    while(1){
    }
}
```
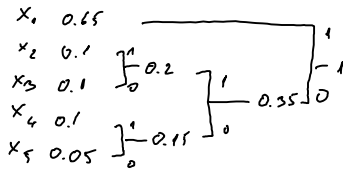
HUFFMAN

$p(x_1) = 0,65$

$p(x_2) = p(x_3) = p(x_4) = 0,1$

$p(x_5) = 0,05$

x_1	0.65
x_2	0.1
x_3	0.1
x_4	0.1
x_5	0.05

0.2, 0.15, 0.35, -1

x_1	1
x_2	011
x_3	010
x_4	001
x_5	000

AXI

Advanced eXtensible interface
- dio AMBA protokola
PS - PL ports (MAS 2-1/64)

AXI High perfomance slave ports (HP0 - HP3)
 - 32 & 64 bit
 - OCM i DDR pristup
 - AXI FIFO suzelje (AFI)
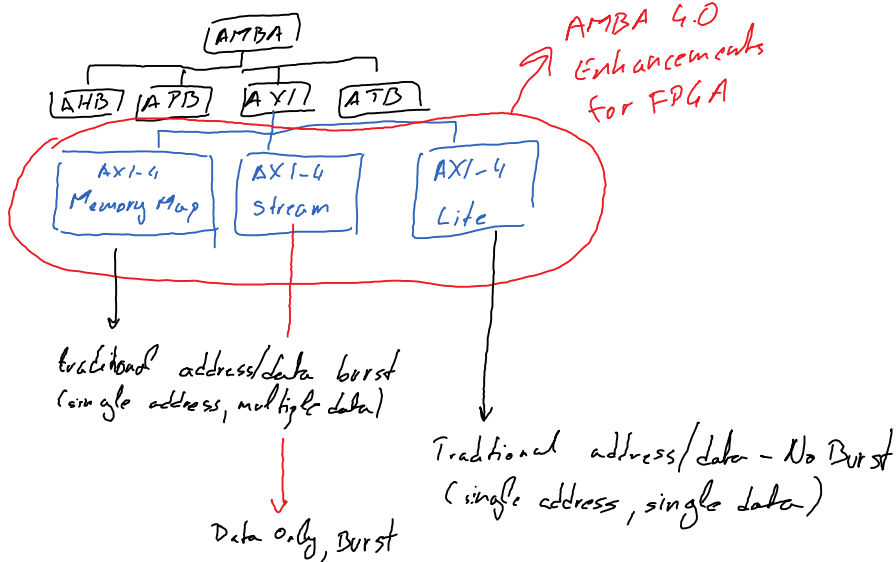
AXI general purpouse ports (GP0 - GP1)
 - dva „master" PS - PL
 - dva „slave" PL - PS
 - 32 bit

'''AXI''', the third generation of AMBA interface defined in the AMBA 3 specification, is targeted at high performance, high clock frequency system designs and includes features that make it suitable for high speed sub-micrometer interconnect:
* separate address/control and data phases
* support for unaligned data transfers using byte strobes
* burst based transactions with only start address issued
* issuing of multiple outstanding addresses with out of order responses
* easy addition of register stages to provide timing closure.

WIKIPEDIA

→ ZA FPGA (MAS 2-1/64)

AMBA
AHB APB AXI ATB

AXI-4 Memory Map
AXI-4 Stream
AXI-4 Lite

AMBA 4.0 Enhancements for FPGA

traditional address/data burst
(single address, multiple data)

Data Only, Burst

Traditional address/data – No Burst
(single address, single data)

IPP - integrated performance primitives (MAS 3-1/45)

Format zapisa - raspored komponenti slikovnih podataka

Channel data Layout - kanalni raspored (oznaka _C)

Planar data Layout - planarni raspored (oznaka _P)

_C3

R G B	R G B	R G B	R G B	R G B	R G B
R G B	R G B	R G B	R G B	R G B	R G B
R G B	R G B	R G B	R G B	R G B	R G B
R G B	R G B	R G B	R G B	R G B	R G B
R G B	R G B	R G B	R G B	R G B	R G B
R G B	R G B	R G B	R G B	R G B	R G B

_P3

R

G

B
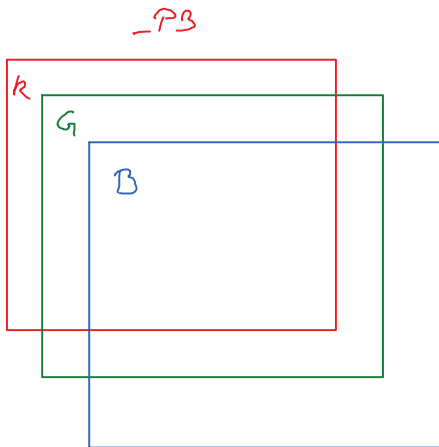
21 2010

①

$$X \rightarrow$$

y ↓

3	2	2	3	5	6	1	3
4	4	8	8	7	6	1	3
4	1	10	20	17	3	3	3
4	4	17	20	20	1	2	4
0	2	19	19	17	1	3	4
1	1	8	8	18	1	3	4
3	1	6	7	20	1	1	4
1	4	1	6	4	1	1	5

$$P(x,y) = P(x-1, y)$$

P(x,y)

$$\frac{1}{64}\begin{bmatrix} 10 & 5 & 5 & 10 & 2 & 4 & 15 & 10 \\ 10 & 10 & 4 & 4 & 2 & 4 & 15 & 10 \\ 10 & 15 & 4 & 4 & 2 & 10 & 10 & 10 \\ 10 & 10 & 2 & 4 & 4 & 15 & 5 & 10 \\ 1 & 5 & 2 & 2 & 2 & 15 & 20 & 10 \\ 15 & 15 & 4 & 4 & 1 & 15 & 10 & 10 \\ 10 & 15 & 4 & 2 & 1 & 15 & 15 & 10 \\ 15 & 10 & 15 & 4 & 10 & 15 & 15 & 2 \end{bmatrix}$$

P(3) = 10/64

P(2) = 5/64

P(5) = 2/64

P(6) = 4/64

P(1) = 15/64

P(4) = 10/64

P(8) = 4/64

P(7) = 2/64

P(20) = 4/64

P(17) = 2/64

P(19) = 2/64

P(18) = 1/64

P(10) = 1/64

P(0) = 1/64

P̂(x,y)

$$\frac{1}{64}\begin{bmatrix} 0 & 10 & 5 & 5 & 10 & 2 & 4 & 15 \\ 0 & 10 & 10 & 4 & 4 & 2 & 4 & 15 \\ 0 & 10 & 15 & 4 & 4 & 2 & 10 & 10 \\ 0 & 10 & 10 & 2 & 4 & 4 & 15 & 5 \\ 0 & 1 & 5 & 2 & 2 & 2 & 15 & 20 \\ 0 & 15 & 15 & 4 & 4 & 1 & 15 & 10 \\ 0 & 10 & 15 & 4 & 2 & 1 & 15 & 15 \\ 0 & 15 & 10 & 15 & 4 & 10 & 15 & 15 \end{bmatrix}$$

e(x,y)

$$\frac{1}{64}\begin{bmatrix} 10 & 5 & 0 & 5 & 8 & 2 & 11 & 5 \\ 10 & 0 & 6 & 0 & 2 & 2 & 11 & 5 \\ 10 & 5 & 11 & 8 & 2 & 8 & 0 & 0 \\ 10 & 0 & 8 & 2 & 0 & 11 & 10 & 5 \\ 1 & 4 & 3 & 0 & 0 & 13 & 5 & 0 \\ 15 & 0 & 11 & 0 & 3 & 14 & 5 & 0 \\ 10 & 5 & 11 & 2 & 1 & 17 & 0 & 5 \\ 15 & 5 & 5 & 11 & 6 & 5 & 0 & 13 \end{bmatrix}$$

Huffman za e

	1	10	5	0	8	2	11	6	4	3	13	14	15
pre	2	6	13	16	3	6	7	2	1	2	2	2	2
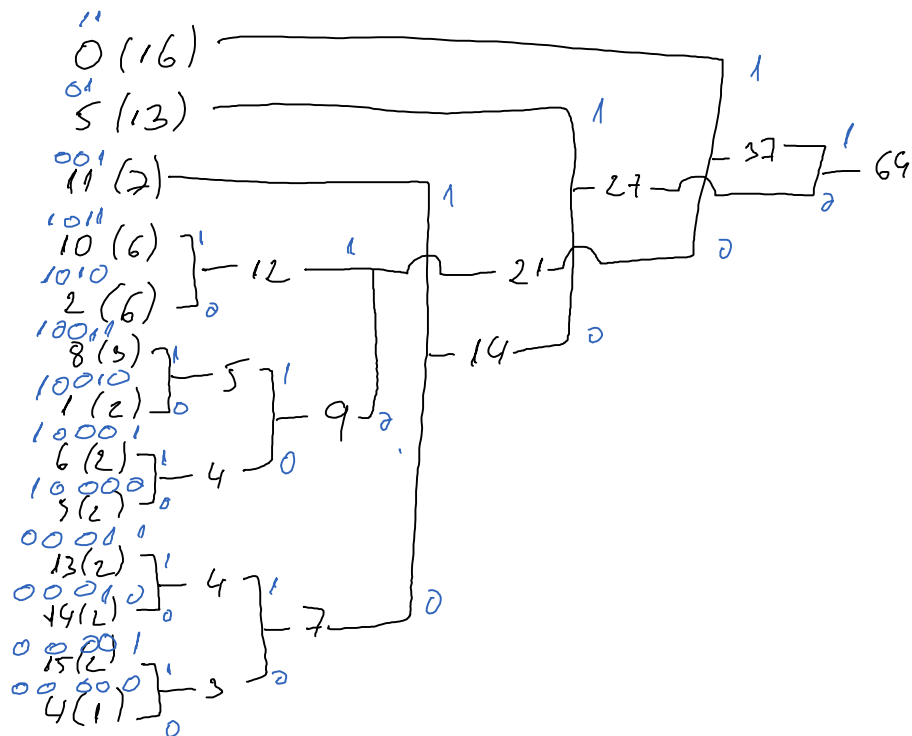
11
0 (16)
01
5 (13)
001
11 (7)
1011
10 (6)]1 — 12 1
1010
2 (6)]0
10011
8 (3)]1 — 5]1
10010
1 (2)]0 — 9]0
10001
6 (2)]1 — 4]0
10000
5 (2)]0
00011
13(2)]1 — 4]1
00010
14(2)]0 — 7
00001
15(2)]1 — 3]0
00000
4(1)]0

— 21 — 27 — 37]1 — 64
     1   1   1   ]2
— 14 0   0   0
  0

M1 2015/2016

①
15 2 -1 0   [-128, 127]
2   1 -1 0
1   1   0 0 =>   4·2³
0   0   0 0

DC | AC →
15 | 2 2 1 1 -1 0 -1 1 0 0 0 0 0 0 0 0
↓   2 2 1 1 1   1   1
kategorija 4

⟨101:1111⟩ ⟨01:10⟩ ⟨01:10⟩⟨00:1⟩ ⟨00:1⟩⟨00:0⟩

⟨1100:0⟩⟨00:1⟩ 1010

STUPANJ KOMPRESIJE $\frac{64}{36} = 1,77$

TEKUĆI
$$\begin{bmatrix} 20 & 20 \\ 1 & 20 \end{bmatrix}$$

REFERENTNI

1	5	2	21	4	3	15	4	4	4
1	5	2	21	4	3	15	4	4	4
1	1	3	2	10	1	17	6	6	4
1	1	4	19	8	8	1	19	9	4
1	2	4	1	19	18	17	3	4	4
1	4	4	4	17	2	20	1	24	4
1	5	0	2	19	19	0	1	15	3
1	4	1	1	3	8	0	1	10	3
1	4	1	1	3	8	0	1	10	3
1	4	1	1	3	8	0	1	1	4

ORT (uzimam prvi korak 4 => jer je to najveći koji mogu,
s obzirom da nije zadan)

TEKUĆI
$$\begin{bmatrix} 20 & 20 \\ 1 & 20 \end{bmatrix}$$
$$MSE = \sum_{i=0}^{N-1} \sum_{j=0}^{N-1} \left(x_{ij} - y_{ij} \right)^2$$

① $\boxed{MSE_G = 365}$ $MSE_L = 941$ $MSE_D = 1162$

BROJ PRETRAŽIVANJA: 13

② $MSE_G = 843$ $MSE_D = 581$ $\boxed{MSE_D}$

③ $MSE_L = 882$ $MSE_D = 1020$ $\boxed{MSE_0}$

④ $MSE_G = 654$ $\boxed{MSE_D = 150}$

⑤ $MSE_L = 614$ $MSE_D = 850$ $\boxed{MSE_0}$

⑥ $MSE_G = 658$ $MSE_D = 581$ $\boxed{MSE_0}$ $\Rightarrow$ vektor pomaka

$(0, 2)$

$$\begin{array}{cccccccccc}
1 & 5 & 2 & 21 & 4 & 3 & 15 & 4 & 4 & 4 \\
1 & 5 & 2 & 21 & 4 & 3 & 15 & 4 & 4 & 4 \\
1 & 4 & 3 & 2 & 10 & 1 & 17 & 6 & 6 & 4 \\
1 & 1 & 4 & 19 & 8 & 8 & 1 & 19 & 9 & 4 \\
1 & 2 & 4 & 1 & 19 & 18 & 17 & 3 & 9 & 4 \\
1 & 4 & 4 & 4 & 17 & 2 & 20 & 1 & 24 & 4 \\
1 & 5 & 2 & 2 & 19 & 19 & 0 & 1 & 15 & 3 \\
1 & 4 & 1 & 1 & 3 & 8 & 0 & 1 & 10 & 3 \\
1 & 4 & 1 & 1 & 3 & 8 & 0 & 1 & 10 & 3 \\
1 & 4 & 1 & 1 & 3 & 8 & 0 & 1 & 1 & 4 \\
\end{array}$$

BROJ PRETRAŽIVANJA

19

TEKUĆI

$$\begin{bmatrix} 20 & 20 \\ 1 & 20 \end{bmatrix}$$

LOG

(1) MSE_0

(2) $MSE_{DOWN} = 150$

(3) MSE_0

(4) MSE_0