

Ispit vježba

30. siječnja 2016. 19:21

2 | 2012/2013 TREKUTNI

① ORT
MAD

20	20
1	20

REFERENTNI BLOK

5	2	21	4	3	15	4	4
1	3	2	10	1	17	6	6
1	4	19	8	8	17	19	9
2	4	1	10	18	1	20	4
4	4	4	2	17	20	1	24
5	0	2	3	3	0	1	15
4	1	1	3	2	0	1	10
4	1	1	3	8	0	1	10
5	1	1	3	8	0	1	10
							2

$$3) \frac{1}{4} (19 + 10 + 3 + 8)$$

$$\frac{1}{4} (2 + 19 + 16 + 0)$$

MAD₀

$$1) MAD_0 = \frac{1}{4} (10 + 2 + 1 + 3) = 4 \quad 2) MAD_n = \frac{1}{4} (10 + 19 + 7 + 12)$$

$$MAD_1 = \frac{1}{4} (10 + 19 + 3 + 16)$$

$$MAD_2 = \frac{1}{4} (12 + 17 + 12 + 18)$$

MAD₀

$$MAD_2 = \frac{1}{4} (19 + 10 + 17 + 19)$$

② $t = 10s$ $U = 1,67$

$$U = \frac{t}{t'} \quad U = \frac{1}{(1-p) + \frac{p}{N}}$$

$$t' = 6s$$

$$N = 4 \quad p = \frac{P}{Q}$$

$$\frac{10}{6} = \frac{1}{1-p + \frac{p}{4}} = \frac{4^2}{4-3p}$$

$$5 = \frac{16}{4-3p} \Rightarrow 20 - 15p = 12$$

$$p = \frac{8}{15} = 0,53$$

③ $N = 2000$ podataka

$$t_{02} = 120 ns$$

$$\text{obrada 1 podatka } t_{pod} = 2ns$$

$$t_{spr} = 150 ns$$

$$t_{oc} = 120 ns$$

$$t_0 = N \cdot t_{pod} = 4000 ns$$

$$t_u = t_{02} + t_0 + t_{spr} = 4270 ns$$

$$p(\text{obrada}) = \frac{4000}{4270} = 0,9367$$

$$1) N = 1$$

$$2) N = 2$$

$$3) N = 4$$

$$t_u = 4270, p = 0,9367 \quad t_u = 4270, p = 0,9367$$

$$U = \frac{1}{n} = 1 \quad U = \frac{1}{n} = 1,27$$

$$U = \frac{1}{1-p + \frac{p}{N}} = 1 \quad U = \frac{1}{1-p + \frac{p}{2}} = 1,88$$

$$E = \frac{U}{N} = 1 \quad E = \frac{U}{N} = 0,94$$

⑤ $p_1 = 35\% \quad N = 5$
 $p_2 = 65\% \quad N = 3$

$$U_1 = \frac{1}{1-p + \frac{p}{N}} = 1,381$$

$$U_2 = \frac{1}{1-0,65 + \frac{0,65}{3}} = 1,75 \quad | \quad 0,21$$

6.

```
#include <xparameters.h>
#include <xiic.h>

#define I2C_CAMERA 0x40

void main (void){
    u8 readBuffer[1] = {0x00};
    u8 writeBuffer[1] = {0x00};
    u8 realWriteBuffer[2] = {0x00, 0x00};

    XIic i2cInstance;
    XIic_Config *cfgPointer;

    cfgPointer = XIic_LookupConfig(XPAR_CAMERA_IIC_DEVICE_ID); // Ova konstanta je nekakav njegov interni identifikator I2C IP-a

    XIic_CfgInitialize (&i2cInstance, cfgPointer, cfgPointer->BaseAddress);
    XIic_SetAddress (&i2cInstance, XII_ADDR_TO_SEND_TYPE, I2C_CAMERA);

    XIic_Start(&i2cInstance);

    writeBuffer[0] = 0x14;
    XIic_MasterSend(&i2cInstance, writeBuffer, 1); // Pišemo adresu registra, prazan ciklus pisanja

    XIic_MasterRecv(&i2cInstance, readBuffer, 1); // Dohvaćamo s te adrese
    if(readBuffer[0] & 0x20){ // 176 x 144
        realWriteBuffer[1] = 0x10; // AEC ADRESA
        realWriteBuffer[0] = 0x56; // AEC = 0x56;
        XIic_MasterSend(&i2cInstance, realWriteBuffer, 2);
    } else { // 352 x 258
        realWriteBuffer[1] = 0x10; // AEC ADRESA
        realWriteBuffer[0] = 0x42; // AEC = 0x56;
        XIic_MasterSend(&i2cInstance, realWriteBuffer, 2);

        writeBuffer[0] = 0x11;
        XIic_MasterSend(&i2cInstance, writeBuffer, 1);

        XIic_MasterRecv(&i2cInstance, readBuffer, 1);
        readBuffer[0] &= 0x1F;
        readBuffer[0] /= 2; // Takt /= 2

        realWriteBuffer[1] = 0x11;
        realWriteBuffer[0] = readBuffer[0];
        XIic_MasterSend(&i2cInstance, realWriteBuffer, 2);
    }

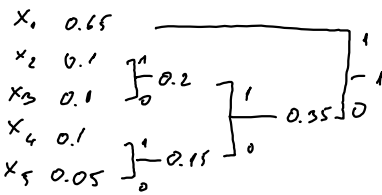
    XIic_Stop(&iic);
    while(1){
    }
}
```

HUFFMAN

$$p(x_1) = 0,65$$

$$p(x_2) = p(x_3) = p(x_4) = 0,1$$

$$p(x_5) = 0,05$$



x_1	1
x_2	011
x_3	010
x_4	001
x_5	000

AXI

Advanced eXtensible interface

- *also AMBA protocols*

PS-PL ports (MAS 2-1/61)

AXI High performance slave ports (HP0-HP3)

- 32 & 64 bit
- OCM i DDR pristup
- AXI FIFO suzeenje (AFI)

AXI general purpose ports (GP0-GP1)

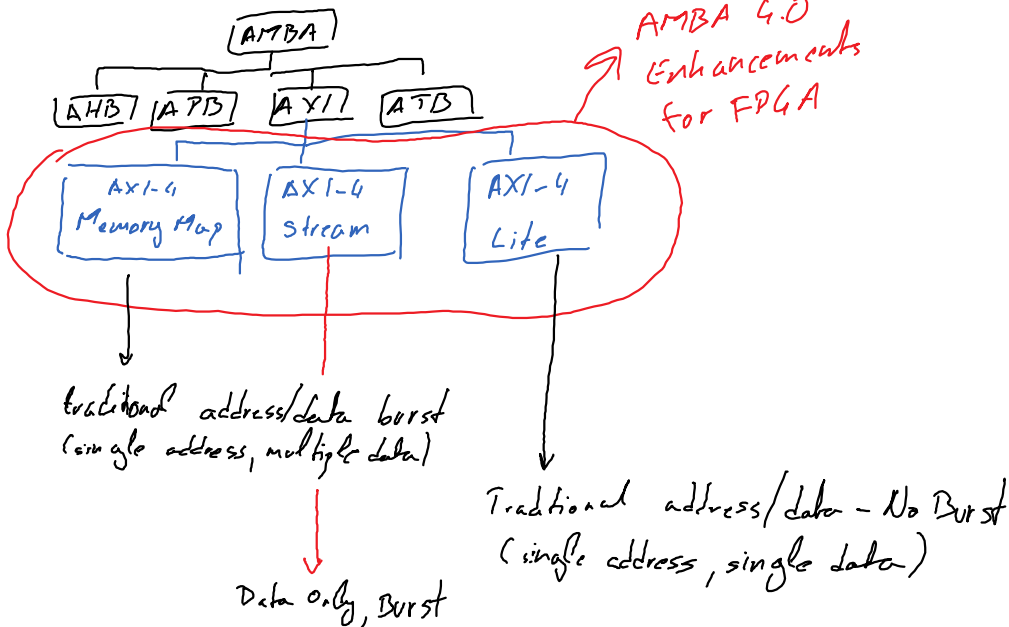
- dva "master" PS-PL
- dva "slave" PL-PS
- 32 bit

"AXI", the third generation of AMBA interface defined in the AMBA 3 specification, is targeted at high performance, high clock frequency system designs and includes features that make it suitable for high speed sub-micrometer interconnect:

- * separate address/control and data phases
- * support for unaligned data transfers using byte strobes
- * burst based transactions with only start address issued
- * issuing of multiple outstanding addresses with out of order responses
- * easy addition of register stages to provide timing closure.

WIKIPEDIA

→ ZA FPGA (MAS 2-1/64)



IPP - integrated performance primitives (MAS 3-1/45)

Format zapisa - raspored komponenti sklopnih podataka

Channel data Layout - kanalni raspored (oznaka - C)

Planar data Layout - planarni raspored (oznaka - P)

-C3

R G B	R G B	R G B	R G B	R G B	R G B
R G B	R G B	R G B	R G B	R G B	R G B
R G B	R G B	R G B	R G B	R G B	R G B
R G B	R G B	R G B	R G B	R G B	R G B
R G B	R G B	R G B	R G B	R G B	R G B
R G B	R G B	R G B	R G B	R G B	R G B

