Note: These are the schematics for the PRODUCTION version (black silkscreen).

Sheet: FPGA

File: FPGA.sch

Sheet: Power

File: power.sch

Sheet: Outputs

File: outputs.sch

Sheet: /
File: hadbadge2019.sch

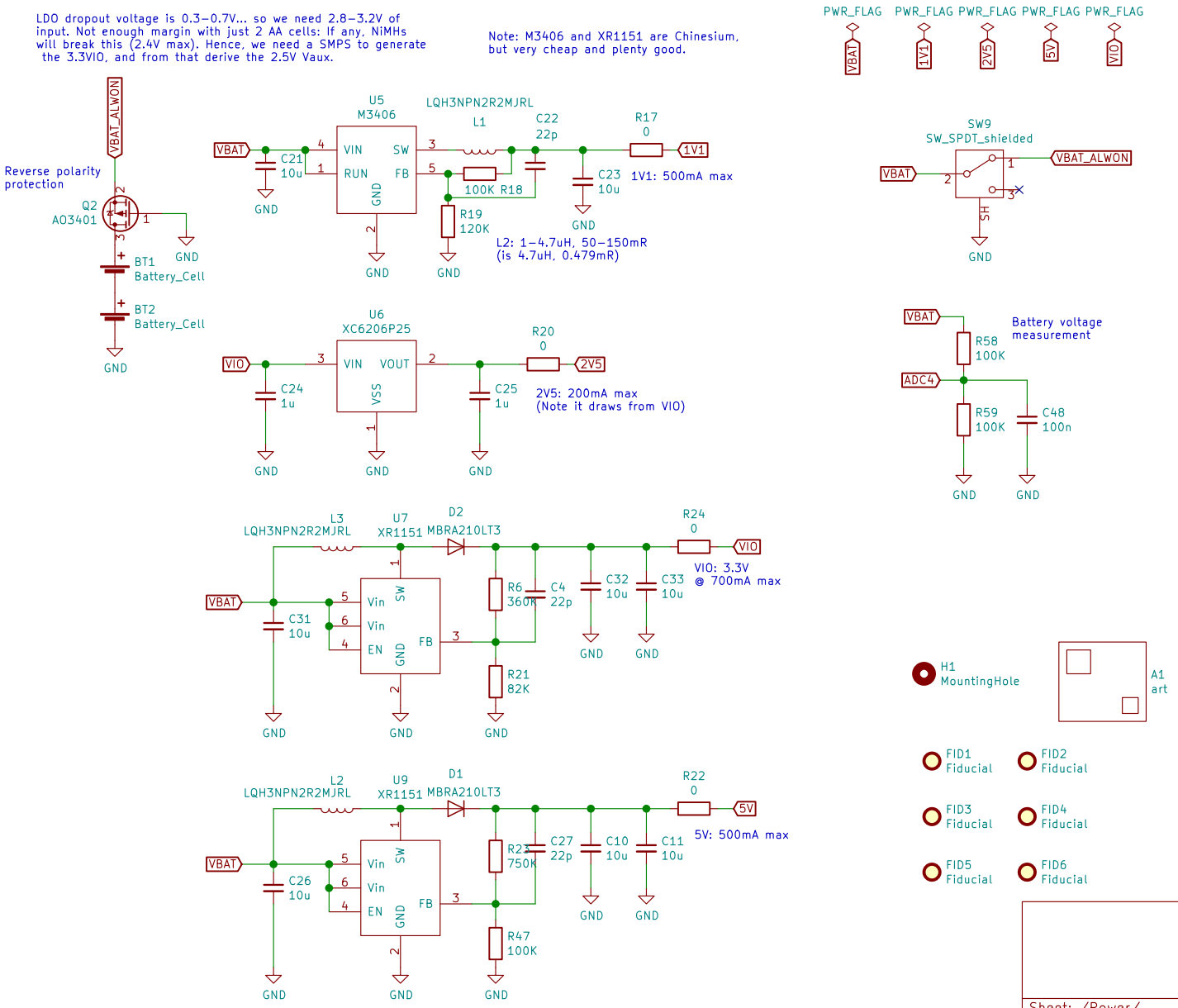
Title: Hackaday Badge 2019

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.4+dfsg1-2		Id: 1/4

U1I
LFE5Ux-45F
GND[85]
VCC[20]
VCCAUX[4]
VCCA0[2]
VCCA1[2]
VCCAUXA0[2]
VCCAUXA1[2]
U1J
LFE5Ux-45F
HDTXP0_D0CH0
VCCHTX0_D0CH0
HDTXN0_D0CH0
HDRXP0_D0CH0
VCCHRX0_D0CH0
HDRXN0_D0CH0
HDRXP0_D0CH1
VCCHRX1_D0CH1
HDRXN0_D0CH1
HDTXP0_D0CH1
VCCHTX1_D0CH1
HDTXN0_D0CH1
RESERVED
RESERVED
REFCLKP_D0
REFCLKN_D0
U1K
LFE5Ux-45F
HDTXP0_D1CH0
VCCHTX0_D1CH0
HDTXN0_D1CH0
HDRXP0_D1CH0
VCCHRX0_D1CH0
HDRXN0_D1CH0
HDRXP0_D1CH1
VCCHRX1_D1CH1
HDRXN0_D1CH1
HDTXP0_D1CH1
VCCHTX1_D1CH1
HDTXN0_D1CH1
REFCLKP_D1
REFCLKN_D1
J1
Conn_02x05_Odd_Even
VBAT_ALWON
VIO
DBGTX
DBGRX
R1 4K7
R2 4K7
R3 4K7
R4 4K7
U1H
LFE5Ux-45F
TDO
TCK
TDI
TMS
C1 100n
U2
LY68L6400SLIT
RAM1_CE
RAM1_SCLK
CE
SCLK
VCC
Vss
SI/SIO0
SO/SIO1
SIO2
SIO3
RAM1_SIO0
RAM1_SIO1
RAM1_SIO2
RAM1_SIO3
U3
LY68L6400SLIT
RAM2_CE
RAM2_SCLK
RAM2_SIO0
RAM2_SIO1
RAM2_SIO2
RAM2_SIO3
C2 100n
Note: All LEDs indeed are RGB LEDs, but normally, only CATA is powered so all LEDs will only light up in whatever color is connected to that. Good luck getting full RGB!
U1C
LFE5Ux-45F
PR32D/PCLKC2_0
PR32B/PCLKC2_1
PR32C/PCLKT2_0
PR32A/PCLKT2_1
PR29D
PR29B
PR29C/GR_PCLK2_0
PR29A/GR_PCLK2_1
PR26D
PR26B
PR26C
PR26A
PR23D
PR23B
PR23C/VREF1_2
PR23A
PR20D
PR20B
PR20C
PR20A
PR17D
PR17B
PR17C
PR17A
PR14D
PR14B
PR14C
PR14A
PR11D
PR11C
PR11B/URC_GPLL0C_IN
PR11A/URC_GPLL0T_IN
VCCIO2[3]
PL35A/PCLKT6_1
PL35C/PCLKT6_0
PL35B/PCLKC6_1
PL35D/PCLKC6_0
PL38A/GR_PCLK6_0
PL38C/GR_PCLK6_1
PL38B
PL38D
PL41A
PL41C
PL41B
PL41D
PL44A
PL44C
PL44B/VREF1_6
PL44D
PL53A
PL59A
PL59C
PL59B
PL59D
PL62A
PL62C
PL62B
PL62D
PL65A
PL65C
PL65B
PL65D
PL68A
PL68B
PL68C/LLC_GPLL0T_IN
PL68D/LLC_GPLL0C_IN
VCCIO6[3]
U1E
LFE5Ux-45F
PL11A/ULC_GPLL0T_IN
PL11B/ULC_GPLL0C_IN
PL11C
PL11D
PL14A
PL14C
PL14B
PL14D
PL17A
PL17C
PL17B
PL17D
PL20A
PL20C
PL20B
PL20D
PL23A
PL23C/VREF1_7
PL23B
PL23D
PL26A
PL26C
PL26B
PL26D
PL29A/GR_PCLK7_1
PL29C/GR_PCLK7_0
PL29B
PL29D
PL32A/PCLKT7_1
PL32C/PCLKT7_0
PL32B/PCLKC7_1
PL32D/PCLKC7_0
VCCIO7[3]
CLK
TP2 TestPoint
U1F
LFE5Ux-45F
PR68D/LRC_GPLL0C_IN
PR68C/LRC_GPLL0T_IN
PR68B
PR68A
PR65D
PR65B
PR65C
PR65A
PR62D
PR62B
PR62C
PR62A
PR59D
PR59B
PR59C
PR59A
PR53A
PR44D
PR44B/VREF1_3
PR44C
PR44A
PR41D
PR41B
PR41C
PR41A
PR38D
PR38B
PR38C/GR_PCLK3_1
PR38A/GR_PCLK3_0
PR35D/PCLKC3_0
PR35B/PCLKC3_1
PR35C/PCLKT3_0
PR35A/PCLKT3_1
VCCIO3[3]
TestPoint TP1
TestPoint TP5
TestPoint TP3
TestPoint TP4
U1D
LFE5Ux-45F
PT85B/URC_GPLL1C_IN
PT83B
PT85A/URC_GPLL1T_IN
PT83A
PT80B
PT78B
PT80A
PT78A
PT76B
PT74B
PT76A
PT74A
PT71B
PT69B
PT71A
PT69A
PT67A
PT58B
PT56B
PT58A
PT56A
PT53B
PT51B
PT53A
PT51A
PT49B
PT47B/GR_PCLK1_1
PT49A
PT47A/GR_PCLK1_0
PT44B/PCLKC1_0
PT42B/PCLKC1_1
PT44A/PCLKT1_0
PT42A/PCLKT1_1
VCCIO1[2]
TestPoint TP6
U1B
LFE5Ux-45F
PT38B/PCLKC0_0
PT36B/PCLKC0_1
PT38A/PCLKT0_0
PT36A/PCLKT0_1
PT33B/GR_PCLK0_0
PT31B
PT33A/GR_PCLK0_1
PT31A
PT29B
PT29A
PT27A
PT20B
PT18B
PT20A
PT18A
PT15B
PT13B
PT15A
PT13A
PT11B
PT9B
PT11A
PT9A
PT6B
PT4B/ULC_GPLL1C_IN
PT6A
PT4A/ULC_GPLL1T_IN
VCCIO0[2]
U1A
LFE5Ux-45F
Bridge pads of R60 (or use 0R resistor) for extra hack-o-meter creds
R60 NS
R61 220R
R62 220R
R63 220R
R64 220R
R65 220R
R72 1K
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
FC-B1010RGBT-HG
R5 1K 15KHz'ish cutoff
PWMOUT
SNDOUT
C3 10n
U8
74LVC1G3157
FLASH_CS
FLASH_CS_EXT
FLASH_CS_INT
U4
74LVC1G175
FSEL_D
FSEL_C
R66 4K7
R67 4K7
R55 4K7
C28 100n
C29 100n
R56 4K7
R7 4K7
Rec: min 32MBit for '45F FPGA (bitstream is 10MBit with max blockram)
U4
W25Q128JVSIQ
FLASH_WP
FLASH_HOLD
FLASH_SCK
FLASH_MOSI
FLASH_MISO
C12 100n
X1
X1G004481001400
C5 100n
R57 1K
ADCREFOUT
ADCREF
C30 10n
R54 100
Lattice LFE5U-45F-8BG381C or LFE5UM-45F-8BG381C
PB4A/D7/IO7
PB6A/D5/MISO2/IO5
PB4B/D6/IO6
PB6B/D4/MOSI2/IO4
PB9A/D3/IO3
PB11A/D1/MISO/IO1
PB9B/D2/IO2
PB11B/D0/MOSI/IO0
PB13A/SN/CSN
PB15A/HOLDN/DI/BUSY/CSSPIN/CEN
PB13B/CS1N
PB15B/DOUT/CSON
PB18A/WRITEN
INITN
CCLK/MCLK/SCK
PROGRAMN
DONE
CFG_1
CFG_2
CFG_0
VCCIO8[2]
U1G
LFE5Ux-45F
R8 NS
R9 NS
R10 4K7
R11 4K7
R12 1K
R13 4K7
TP11
TestPoint
R14 0
R15 0
R16 NS
C6 100n
C7 100n
C8 100n
C9 100n
C13 100n
C14 100n
C15 100n
C16 100n
C17 100n
C18 100n
C19 100n
C20 100n
R69 10K
R70 10K
R71 10K
Q3 AO3400
Q4 AO3400
Q5 AO3400
Spritesmods
Sheet: /FPGA/
File: FPGA.sch
Title: Hackaday Badge 2019
Size: A3
Date: 2019-02-09
Rev: 1
KiCad E.D.A. kicad 5.1.4+dfsg1-2
Id: 2/4

LDO dropout voltage is 0.3–0.7V... so we need 2.8–3.2V of input. Not enough margin with just 2 AA cells: If any, NiMHs will break this (2.4V max). Hence, we need a SMPS to generate the 3.3VIO, and from that derive the 2.5V Vaux.

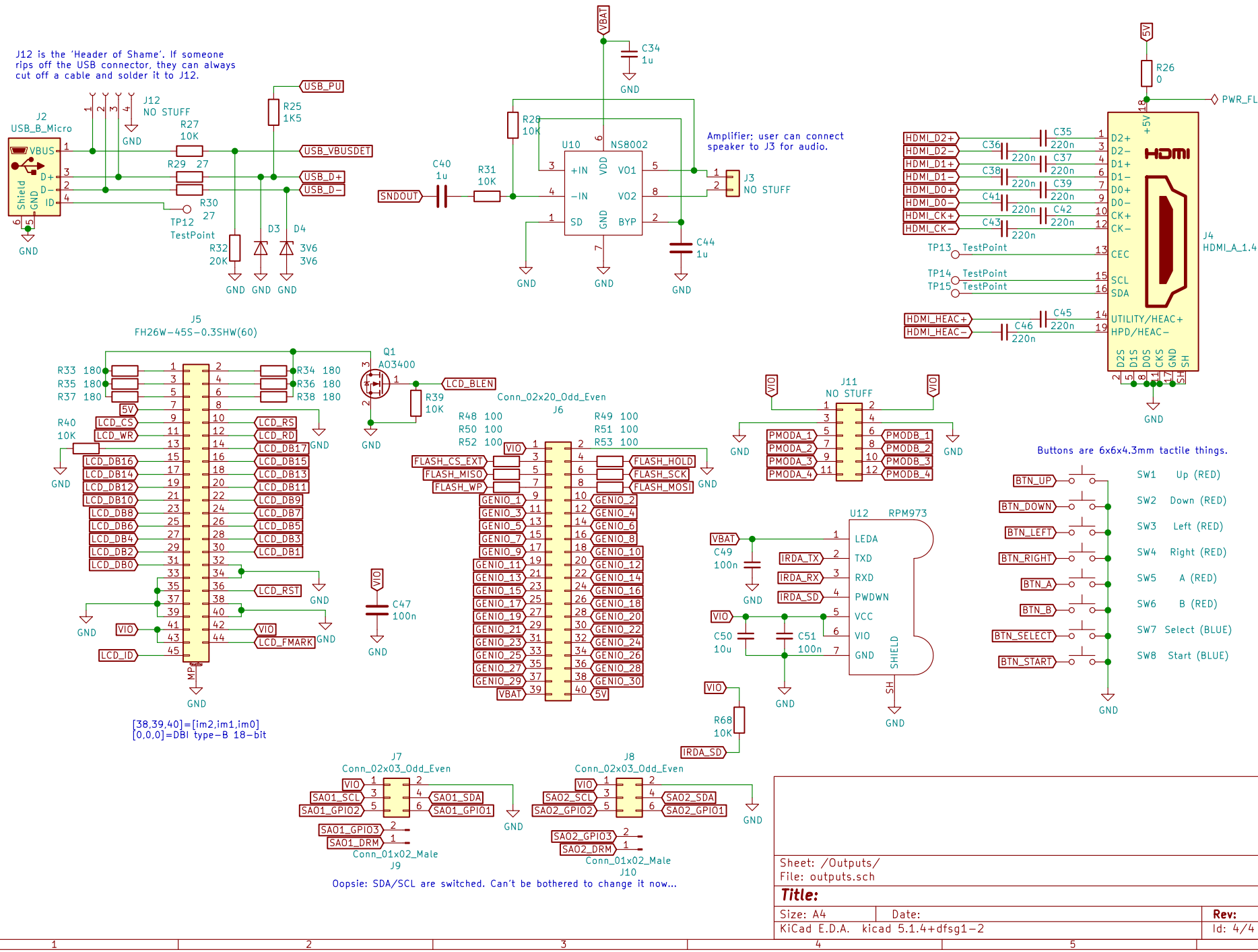
Note: M3406 and XR1151 are Chinesium, but very cheap and plenty good.



Sheet: /Power/
File: power.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.4+dfsg1-2		Id: 3/4


J12 is the 'Header of Shame'. If someone rips off the USB connector, they can always cut off a cable and solder it to J12.
J2
USB_B_Micro
J12
NO STUFF
R25
1K5
R27
10K
R29 27
R30
27
TP12
TestPoint
R32
20K
D3
D4
3V6
3V6
USB_PU
USB_VBUSDET
USB_D+
USB_D-
VBUS
D+
D-
ID
Shield
GND
Amplifier; user can connect speaker to J3 for audio.
U10
NS8002
+IN
-IN
SD
GND
VDD
VO1
VO2
BYP
C34
1u
C40
1u
R31
10K
R28
10K
C44
1u
SNDOUT
J3
NO STUFF
VBAT
R26
0
PWR_FLAG
+5V
J4
HDMI_A_1.4
HDMI_D2+
HDMI_D2-
HDMI_D1+
HDMI_D1-
HDMI_D0+
HDMI_D0-
HDMI_CK+
HDMI_CK-
HDMI_HEAC+
HDMI_HEAC-
C35
C36
C37
C38
C39
C41
C42
C43
C45
C46
220n
TP13
TP14
TP15
CEC
SCL
SDA
UTILITY/HEAC+
HPD/HEAC-
J5
FH26W-45S-0.3SHW(60)
Q1
AO3400
R39
10K
LCD_BLEN
R33 180
R35 180
R37 180
R34 180
R36 180
R38 180
R40
10K
LCD_CS
LCD_WR
LCD_RS
LCD_RD
LCD_DB17
LCD_DB15
LCD_DB13
LCD_DB11
LCD_DB9
LCD_DB7
LCD_DB5
LCD_DB3
LCD_DB1
LCD_DB16
LCD_DB14
LCD_DB12
LCD_DB10
LCD_DB8
LCD_DB6
LCD_DB4
LCD_DB2
LCD_DB0
LCD_RST
LCD_FMARK
LCD_ID
[38,39,40]=[im2,im1,im0]
[0,0,0]=DBI type-B 18-bit
Conn_02x20_Odd_Even
J6
R48 100
R50 100
R52 100
R49 100
R51 100
R53 100
FLASH_CS_EXT
FLASH_MISO
FLASH_WP
FLASH_HOLD
FLASH_SCK
FLASH_MOSI
GENIO_1
GENIO_2
GENIO_3
GENIO_4
GENIO_5
GENIO_6
GENIO_7
GENIO_8
GENIO_9
GENIO_10
GENIO_11
GENIO_12
GENIO_13
GENIO_14
GENIO_15
GENIO_16
GENIO_17
GENIO_18
GENIO_19
GENIO_20
GENIO_21
GENIO_22
GENIO_23
GENIO_24
GENIO_25
GENIO_26
GENIO_27
GENIO_28
GENIO_29
GENIO_30
C47
100n
J11
NO STUFF
PMODA_1
PMODA_2
PMODA_3
PMODA_4
PMODB_1
PMODB_2
PMODB_3
PMODB_4
U12
RPM973
LEDA
TXD
RXD
PWDWN
VCC
VIO
GND
SHIELD
IRDA_TX
IRDA_RX
IRDA_SD
C49
100n
C50
10u
C51
100n
R68
10K
Buttons are 6x6x4.3mm tactile things.
BTN_UP
BTN_DOWN
BTN_LEFT
BTN_RIGHT
BTN_A
BTN_B
BTN_SELECT
BTN_START
SW1 Up (RED)
SW2 Down (RED)
SW3 Left (RED)
SW4 Right (RED)
SW5 A (RED)
SW6 B (RED)
SW7 Select (BLUE)
SW8 Start (BLUE)
J7
Conn_02x03_Odd_Even
SA01_SCL
SA01_GPIO2
SA01_SDA
SA01_GPIO1
SA01_GPIO3
SA01_DRM
J9
Conn_01x02_Male
J8
Conn_02x03_Odd_Even
SA02_SCL
SA02_GPIO2
SA02_SDA
SA02_GPIO1
SA02_GPIO3
SA02_DRM
J10
Conn_01x02_Male
Oopsie: SDA/SCL are switched. Can't be bothered to change it now...
Sheet: /Outputs/
File: outputs.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad 5.1.4+dfsg1-2
Id: 4/4