32 -bit microcontroller

ADVANCED_TIMER module

Suitable

series	Product number	series	Product number
HC32L110	HC32L110C6UA HC32L110C6PA HC32L110C4UA HC32L110C4PA HC32L110B6PA HC32L110B4PA	**HC32F030**	HC32F030E8PA HC32F030F8UA HC32F030F8TA HC32F030J8TA HC32F030K8TA
HC32F003	HC32F003C4UA HC32F003C4PA	**HC32L136**	HC32L136J8TA HC32L136K8TA
HC32F005	HC32F005C6UA HC32F005C6PA HC32F005D6UA	**HC32L130**	HC32L130E8PA HC32L130F8UA HC32L130J8TA

content

1 Summary... 3

2 Features.. 3

3 ADVANCED TIMER MODULE 4

3.1 Independent channel PWM output... 4

3.2 Software Complementary PWM Output 8

3.3 Hardware Setting Complementary PWM Output - Hardware Dead Time Function 9

3.4 Level inversion action of CHA and CHB..................................... .... .11

3.4.1 Ramp up count mode.. 11

3.4.2 Ramp wave countdown mode.. 11

3.4.3 Triangle wave mode... 12

3.5 Protection mechanism... 15

3.6 Internal Interconnects... 16

4 Reference samples and drivers 17

5Summary 17

6 Additional Information 18

7Version Information **&** Contact **19**

1 Summary

This application note mainly introduces the multi-function PWM generator of the Advanced Timer module of Huada Semiconductor MCU*.

This application note mainly includes:

ÿ Introduction of Advanced Timer module

ÿ Independent channel PWM output

ÿ Software complementary PWM output

ÿ Hardware set complementary PWM output - hardware dead time function

ÿ Level inversion action of CHA and CHB

ÿ Protection mechanism

ÿ Internal interconnection

Notice:

- This application note is the application supplementary material of Huada Semiconductor MCU*, and cannot replace the user manual.

Please refer to the user manual for the operation of the device and other related matters.

2 Function introduction

The Advanced Timer module (ADT for short) contains three high-performance timers TIM4/5/6 with the same function, a single timer

It can generate single or 2 independent PWM outputs, it can also generate a pair of complementary PWM outputs, and it can also be used to capture

Obtain the external input waveform for pulse width or period measurement.

* See the cover for supported models.

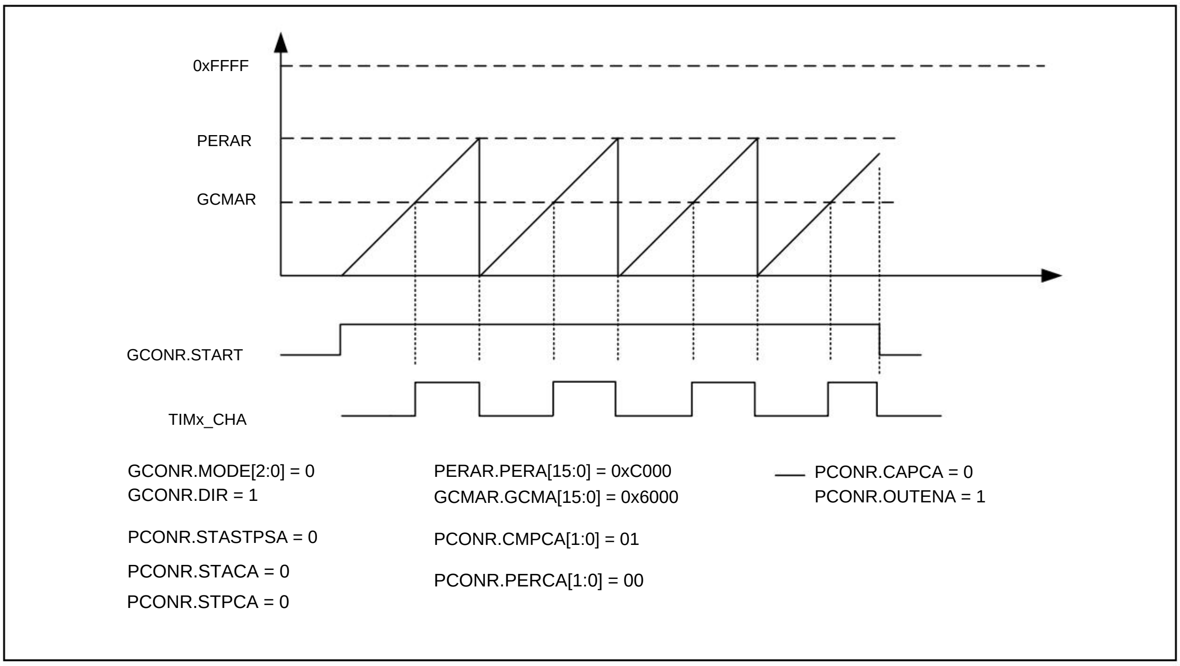
3 ADVANCED TIMER module

3.1 Independent channel PWM output

TIM4/5/6 have two output ports TIMx_CHA and TIMx_CHB, which can output two independent channels independently or at the same time.

PWM wave.

The TIM4/5/6 has two basic counting waveforms (carriers): Ramp mode and Triangle mode.



GCONR.MODE[2:0] = 0
GCONR.DIR = 1

PCONR.STASTPSA = 0

PCONR.STACA = 0

PCONR.STPCA = 0

PERAR.PERA[15:0] = 0xC000
GCMAR.GCMA[15:0] = 0x6000

PCONR.CMPCA[1:0] = 01

PCONR.PERCA[1:0] = 00

PCONR.CAPCA = 0
PCONR.OUTENA = 1

Figure 1. Ramp Up Counting Mode

As shown in Figure 1, when the CHA port is set to output and enabled, the timer counts up to the compare reference value register GCMAR

value, the output level will act accordingly according to the setting of PCONR.CMPCA, when the timer counts to PERAR

The output level will act accordingly according to the setting of PCONR.PRECA.

When GCONR.START is set to 1, the corresponding CNTER of ADT starts to run. GCONR.START write 0 again, CNTER

The counting will stop, but CNTER will not be cleared. When clearing, you need to write 0 to CNTER

The level state of the CHA port at start and stop is determined by the registers PCONR.STASTPSA, PCONR.STACA,

PCONR.STPCA to decide jointly.

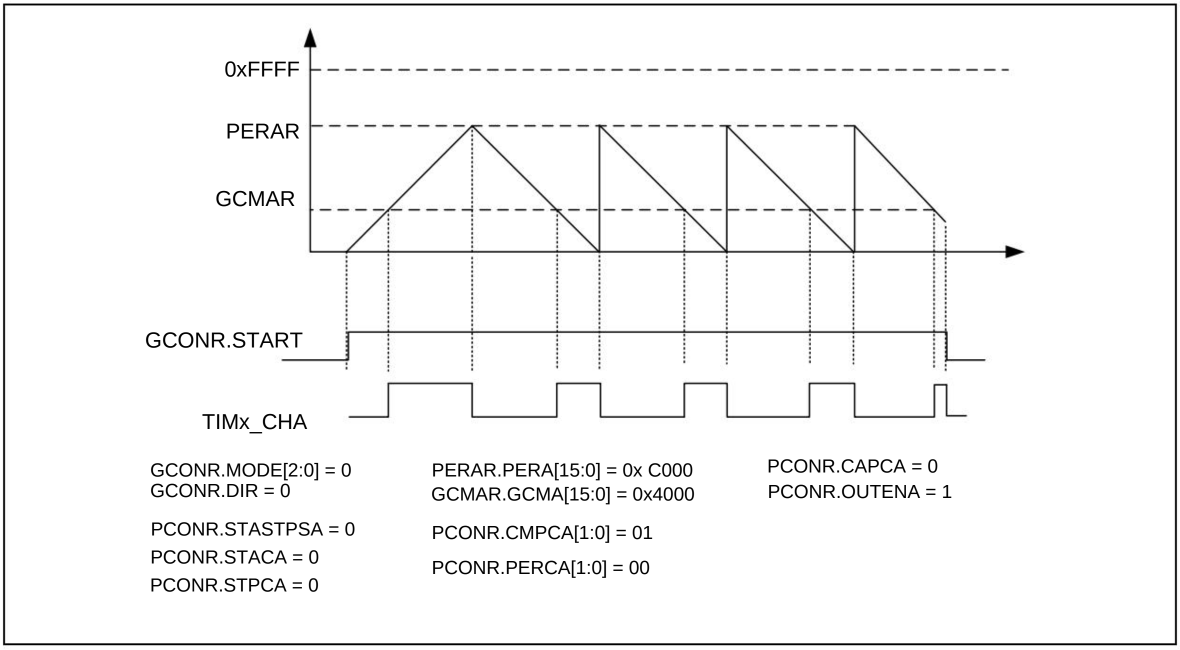


Figure 2. Ramp Down Counting Mode

As shown in Figure 2, the sawtooth wave counts down mode, if CTER is not set to the initial value, it is still 0, then when the counting starts,

CNTER will still count up from 0 to the value of PERAR, then count down to 0, and then start from PERAR's value.

The value counts down to 0. Therefore, in the first cycle, the duty cycle of the CHA output is not consistent with the subsequent ones.

Therefore, when ADT is in the sawtooth wave countdown mode, before enabling, the initial value of CNT should be set to the value of PERAR first.

Avoid inconsistencies in the first cycle output duty cycle.

The CHB output principle is the same as CHA.

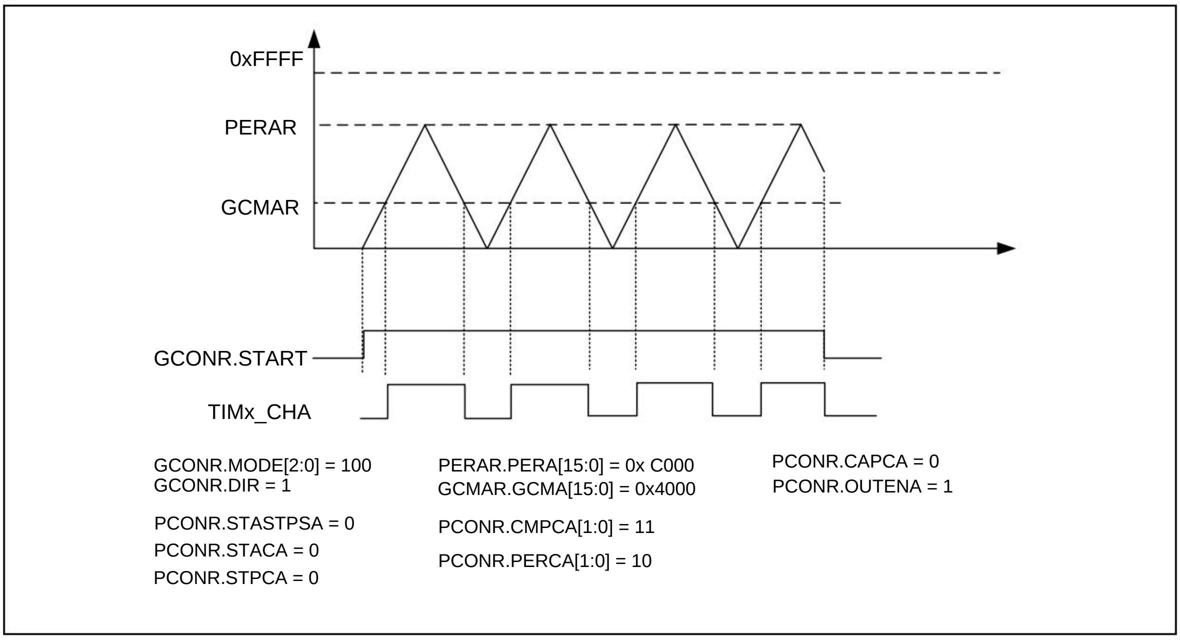


Figure 3. Triangle Wave Up Counting Mode

When the counting waveform is a triangle wave, the output principle of CHA/CHB is the same as above, but there are some differences:

The value of PERAR is 1/2 of the actual period count value.

When the value of the comparison reference value register GCMAR is between 0 and the period value (PERAR), CNTER in one cycle

Will go through GCMAR twice.

The level action of the PCONR.PERCA setting is valley response.

The buffer transmission time point is different from the sawtooth wave.

The counting direction of CNTER starts from 0 and counts upwards, and the countdown setting has no meaning for triangular wave mode.

When the buffer transfer function is enabled, the user can write the comparison reference value into the buffer transfer at any time in the interrupt or main loop.

Only when the transfer time point is reached, the value of the cache register will be transferred to the corresponding register.

If the user uses a timer with two or three ADTs and needs to keep a synchronous count, then all periodic update values are written

The incoming PERBR must ensure that they are all before the same cache transfer point (to ensure that the cache transfer update at the same time), otherwise it will cause

The count is out of sync.

Delivery time:

Sawtooth wave: up-count overflow point or down-count underflow point

Triangle wave A: count valley points (wave valleys)

Triangle wave B: count valleys (valleys) and count peaks (peaks)

Related cache register transfer path:

PERBR	ÿ PERAR;
GCMCR	ÿ GCMAR;
GCMDR	ÿ GCMBR.

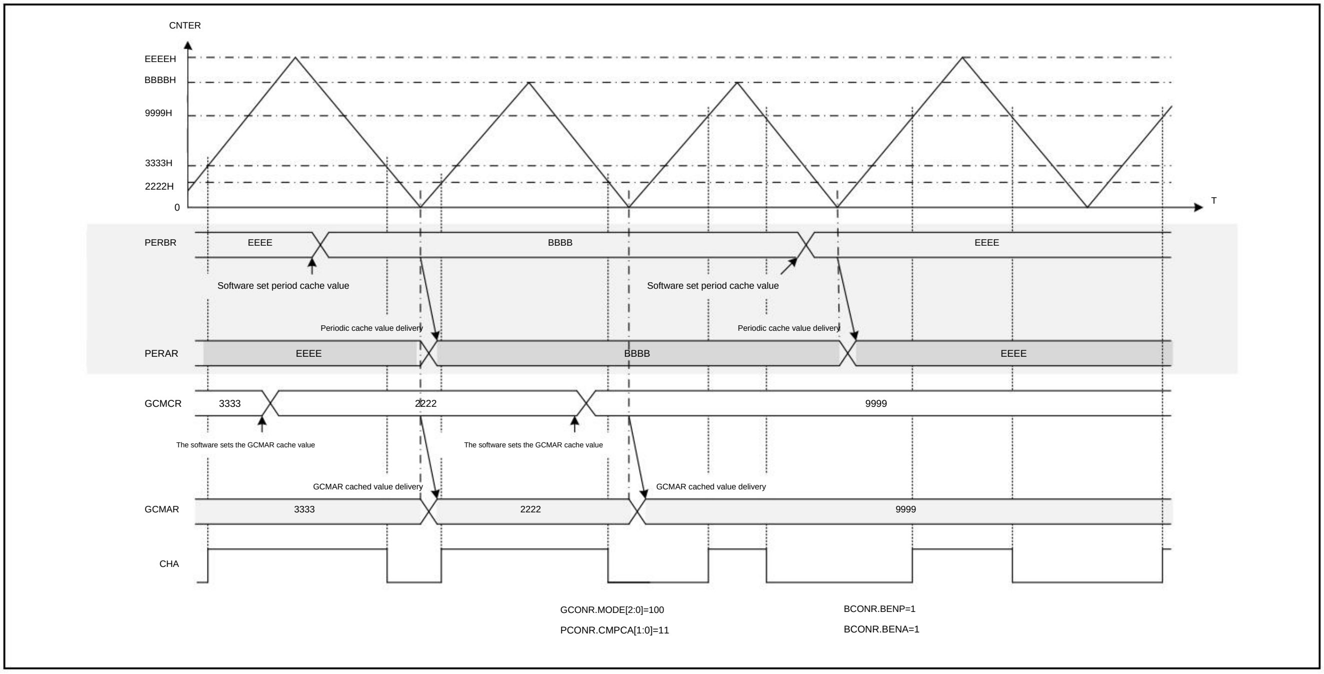

CNTER
EEEEH
BBBBH
9999H
3333H
2222H
0
T
PERBR
EEEE
BBBB
EEEE
Software set period cache value
Software set period cache value
Periodic cache value delivery
Periodic cache value delivery
PERAR
EEEE
BBBB
EEEE
GCMCR
3333
2222
9999
The software sets the GCMAR cache value
The software sets the GCMAR cache value
GCMAR cached value delivery
GCMAR cached value delivery
GCMAR
3333
2222
9999
CHA
GCONR.MODE[2:0]=100
PCONR.CMPCA[1:0]=11
BCONR.BENP=1
BCONR.BENA=1

Figure 4. Schematic diagram of buffer transmission in triangular wave A mode

3.2 Software Complementary PWM Output

A timer unit of ADT, when using triangular wave as carrier, CHA and CHB can output two complementary PWM

waveform. The configuration method is similar to the independent output, with the following additional notices:

When setting the compare reference register of CHB, the calculation dead time needs to be considered.

As shown in Figure 5, GCMDR is the comparison reference value buffer register of CHB:

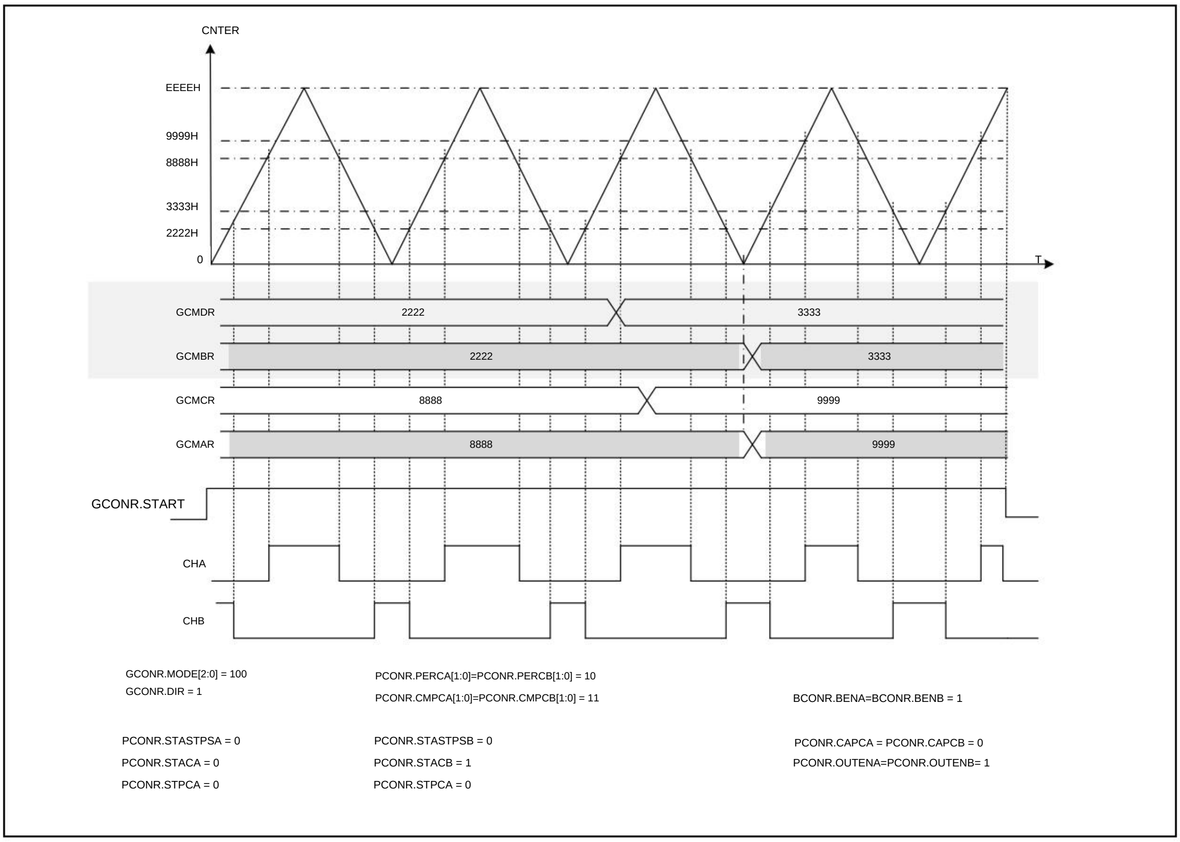
GCMDR = GCMCR – Dead Time

When starting to count, the start level of CHB should be set to a high level, that is, PCONR.STACB=1, in order to achieve the same

CHA outputs complementary purposes.

When complementary output, it is recommended to use the buffer transfer function to achieve the purpose of updating GCMAR and GCMBR at a specific time,

There will be no abnormal situation in which the CHA and CHB levels are abnormally reversed, and the effective switching level signal is output at the same time.



GCONR.MODE[2:0] = 100
GCONR.DIR = 1

PCONR.STASTPSA = 0
PCONR.STACA = 0
PCONR.STPCA = 0

PCONR.PERCA[1:0]=PCONR.PERCB[1:0] = 10
PCONR.CMPCA[1:0]=PCONR.CMPCB[1:0] = 11

PCONR.STASTPSB = 0
PCONR.STACB = 1
PCONR.STPCA = 0

BCONR.BENA=BCONR.BENB = 1

PCONR.CAPCA = PCONR.CAPCB = 0
PCONR.OUTENA=PCONR.OUTENB= 1

Figure 5. Software Complementary PWM Output in Triangle A Mode

3.3 Hardware set complementary PWM output - hardware dead time function

When the dead time function is enabled, the comparison reference value register GCMBR that determines the level of the CHB port is registered by the comparison reference value.

It is determined by the value operation of the register (GCMAR) and the dead time reference value register (DTUAR, DTDAR).

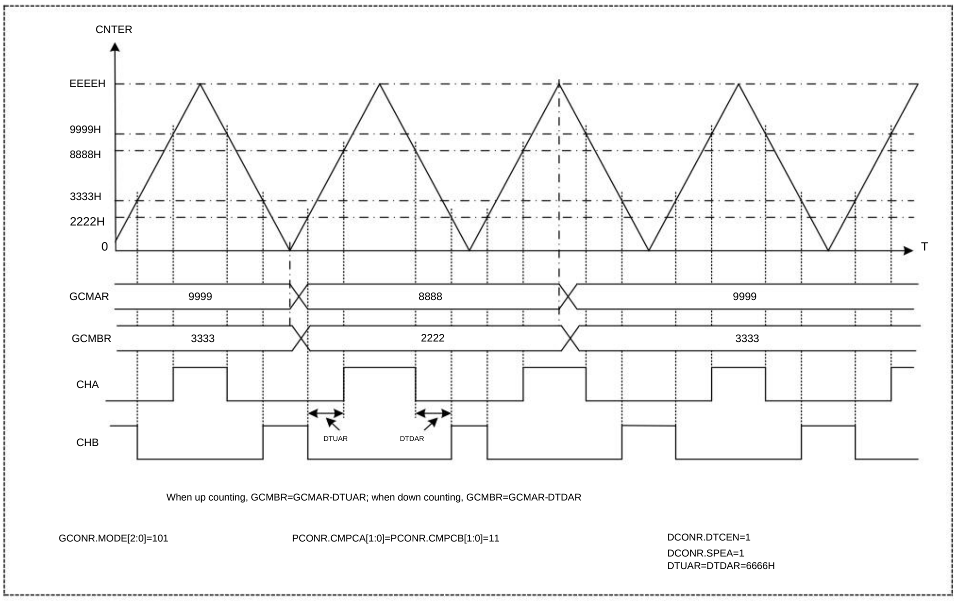


Figure 6. Schematic diagram of hardware dead zone function setting GCMBA

As shown in Figure 6:

When Up counting: GCMBR = GCMAR - DTUAR

During down counting: GCMBR = GCMAR – DTDAR

(DCONR.SEPA = 1, the value of DTDAR is automatically equal to the value of DTUAR)

When the buffer transfer function is enabled, the PWM duty cycle of the complementary output can be controlled by changing the value of GCMCR.

If the hardware dead time function is enabled to set the hardware complementary PWM output, the following points should be noted:

1. During initialization, if GCMAR is set to ÿ the period value (PERAR), the subsequent CHB level will be error.

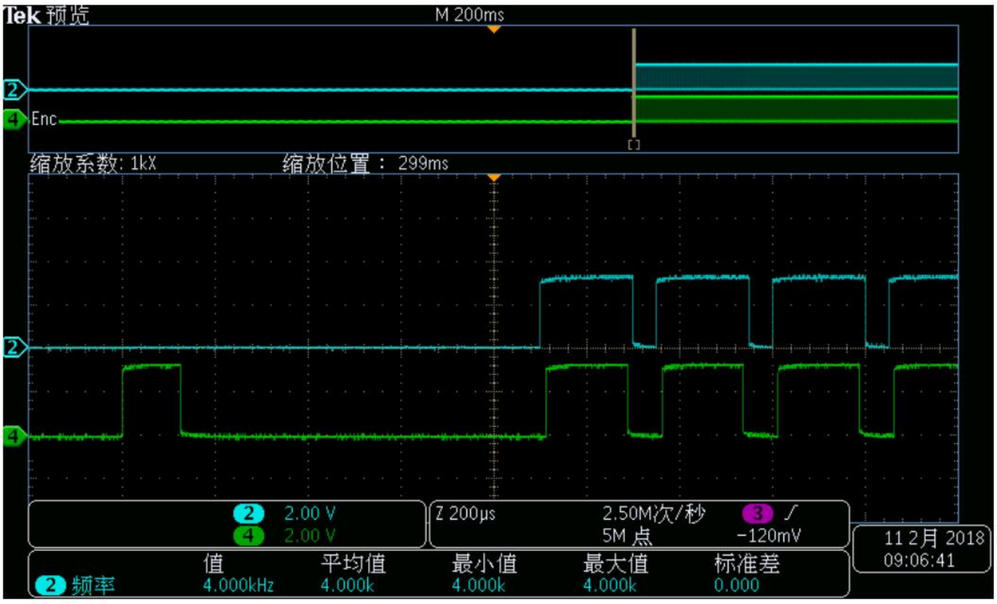


Figure 7. GCMBR initialized to 0xFFFF, CHB (green) subsequent output error

2. During initialization, the buffer transfer function is enabled, and GCMAR should be set to a value between 0 and the period value (PERAR). GCMCR is set to 0xFFFF. After enabling ADT in this way, CHB will not output an error.

3. When set as above, if PCONR.STACA = 0, PCONR.STACB = 1, after ADT is enabled to run, CHA It should output low level, CHB should output high level, but the initial IO port is input high impedance state, so at this moment CHA and CHB will not output the level. You can set the corresponding PIN pin port function to ADT when needed. CHA and CHB ports. In this way, CHA will output a low level, and CHB will output a high level. when 0 < GCMCR < PERAR, CHA and CHB will resume output hardware dead time complementary PWM waveform.

3.4 Level inversion of CHA and CHB

When the value of GCMAR and GCMBR is between 0 and the period value (PERAR), the level of CHA and CHB is flipped

Determined by PCONR.CMPCA, PCONR.CMPCB, PCONR.PERCA, and PCONR.PERCB. the above

chapter has been described.

This section briefly introduces the CHA and GCMBR values when GCMAR and GCMBR are 0 or ÿ the period value (PERAR).

The case of CHB level action.

3.4.1 Sawtooth Wave Incremental Counting Mode

When PCONR.PERCA = 0, PCONR.CMPCA = 1 :

When GCMAR ÿ period value (PERAR), CHA outputs low level.

When GCMAR = 0, CHA outputs high level, but when CNTER is overflowing, there will be a low level pulse

output.

When PCONR.PERCA = 1, PCONR.CMPCA = 0 :

When GCMAR ÿ period value (PERAR), CHA outputs high level.

When GCMAR = 0, CHA outputs low level, but when CNTER is overflowing, there will be a high level pulse

output.

3.4.2 Sawtooth wave countdown mode

When PCONR.PERCA = 0, PCONR.CMPCA = 1 :

When GCMAR = 0, the CHA output is low.

When GCMAR > period value (PERAR), CHA outputs low level.

When GCMAR = period value (PERAR), CHA outputs a high level, but when CNTER is in underflow, there will be

A low-level pulse output.

When PCONR.PERCA = 1, PCONR.CMPCA = 0 :

When GCMAR = 0, the CHA output is high.

When GCMAR > period value (PERAR), CHA outputs high level.

When GCMAR = period value (PERAR), CHA outputs a low level, but when CNTER is in underflow, there will be

A high-level pulse output.

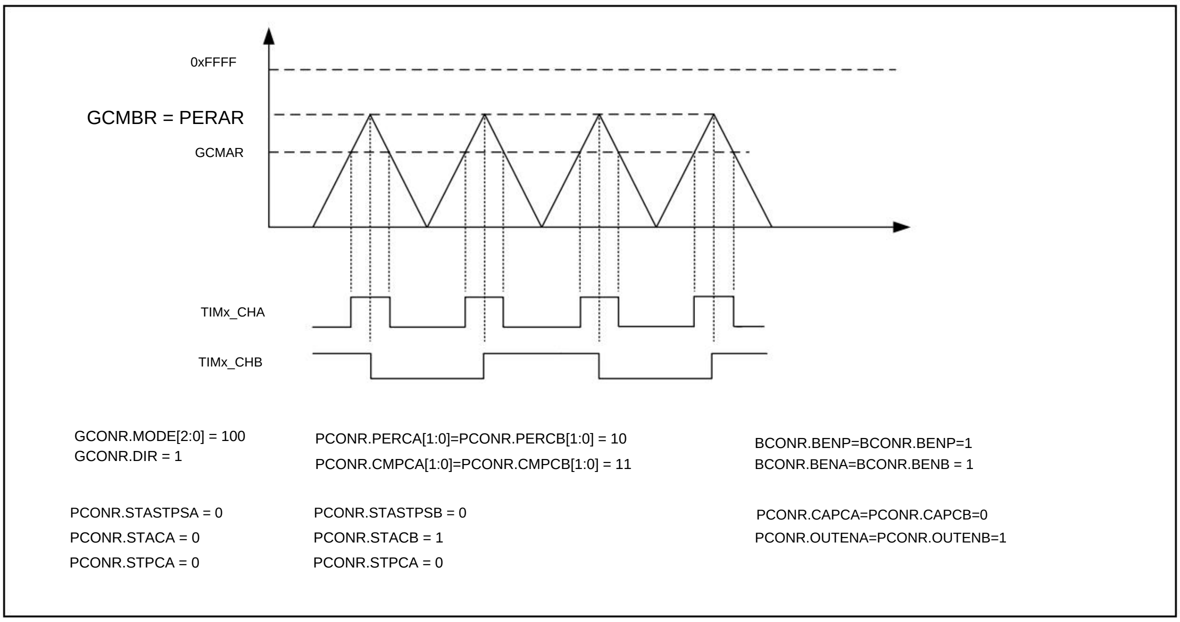
3.4.3 Triangle wave mode

When the hardware deadband function is disabled:

When the relevant registers are set as follows, the value of GCMAR is between 0 and the period value (PERAR), and the normal output of CHA is

For reference:

When GCMBR = the value of PERAR, the CHB level flips at the peak of the triangle wave, as shown in Figure 8.



GCONR.MODE[2:0] = 100
GCONR.DIR = 1

PCONR.PERCA[1:0]=PCONR.PERCB[1:0] = 10
PCONR.CMPCA[1:0]=PCONR.CMPCB[1:0] = 11

BCONR.BENP=BCONR.BENP=1
BCONR.BENA=BCONR.BENB = 1

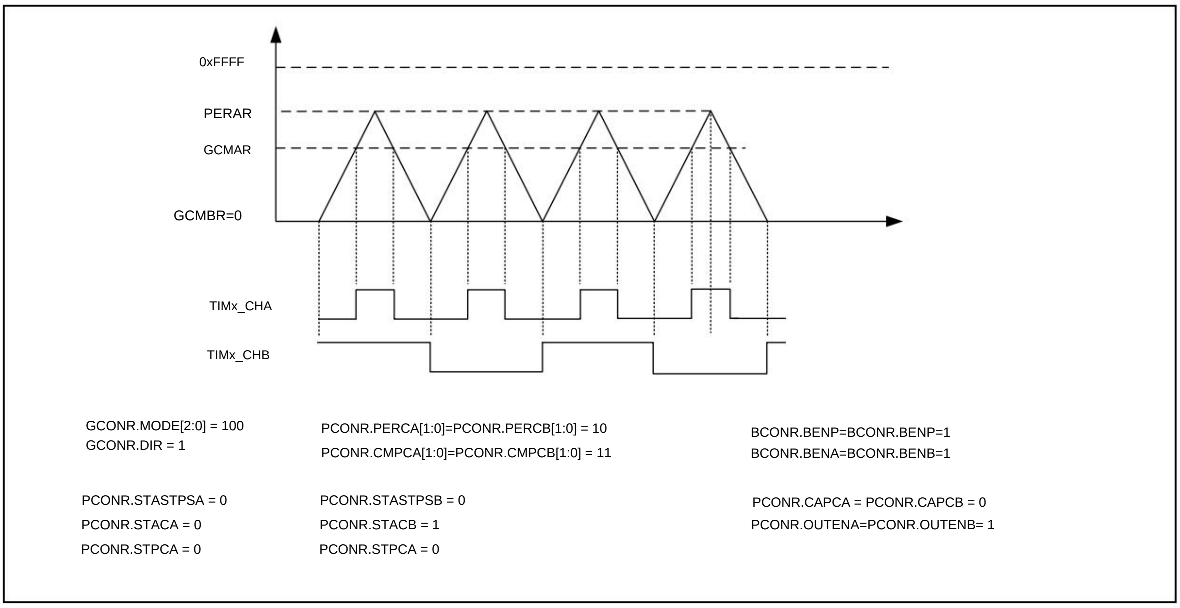
PCONR.STASTPSA = 0
PCONR.STACA = 0
PCONR.STPCA = 0

PCONR.STASTPSB = 0
PCONR.STACB = 1
PCONR.STPCA = 0

PCONR.CAPCA=PCONR.CAPCB=0
PCONR.OUTENA=PCONR.OUTENB=1

Figure 8. When GCMBR is the period value, the CHB level inversion diagram

When GCMBR = 0, the CHB level flips at the trough of the triangle wave, as shown in Figure 9.



GCONR.MODE[2:0] = 100
GCONR.DIR = 1

PCONR.PERCA[1:0]=PCONR.PERCB[1:0] = 10
PCONR.CMPCA[1:0]=PCONR.CMPCB[1:0] = 11

BCONR.BENP=BCONR.BENP=1
BCONR.BENA=BCONR.BENB=1

PCONR.STASTPSA = 0
PCONR.STACA = 0
PCONR.STPCA = 0

PCONR.STASTPSB = 0
PCONR.STACB = 1
PCONR.STPCA = 0

PCONR.CAPCA = PCONR.CAPCB = 0
PCONR.OUTENA=PCONR.OUTENB= 1

Figure 9. When GCMBR is 0, CHB level inversion diagram

When the hardware dead time function is enabled:

Triangle wave count mode with valid hardware dead zone function and valid buffer function

And: PCONR.PERCA = PCONR.PERCB = 10

PCONR.CMPCA = PCONR.CMPCB = 11

When GCMAR = 0 or GCMAR ÿ PERAR:

The output hold of the over-cycle protection setting occurs.

And when 0<GCMAR<PERAR, CHA and CHB return to normal output level at the counting valley point.

An example of a triangle wave A mode is given below:

1. GCMARÿPERAR

Can't go directly from GCMAR ÿ PERAR ÿ GCMAR = 0

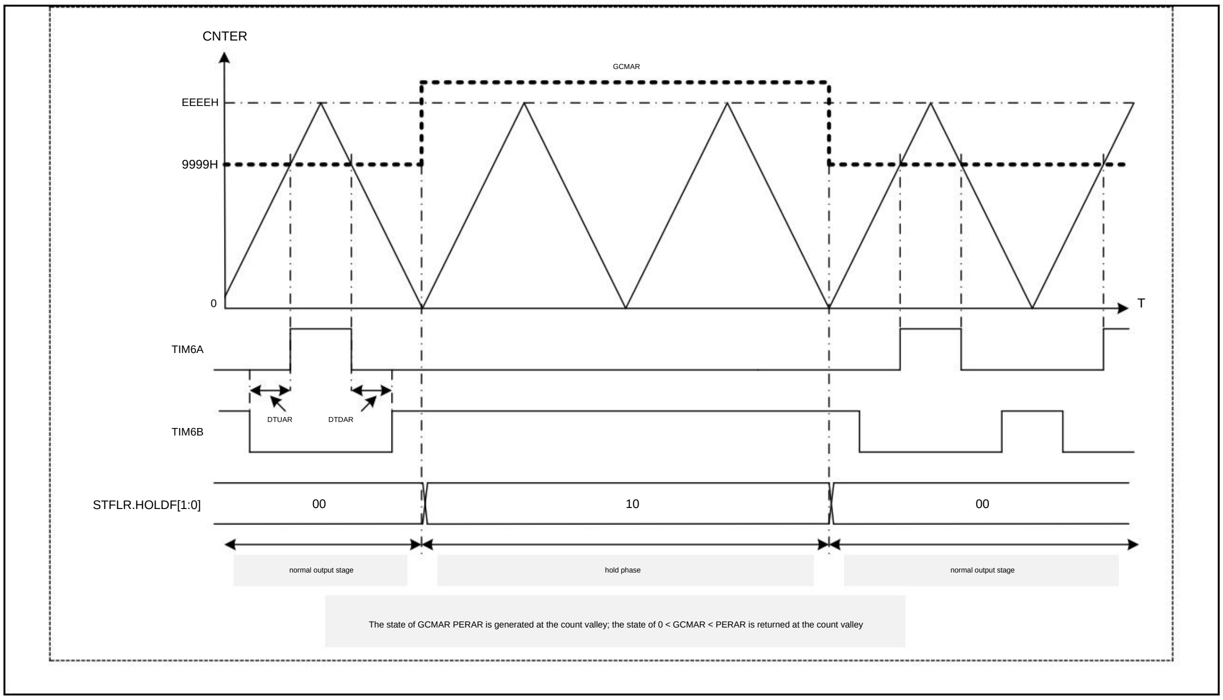
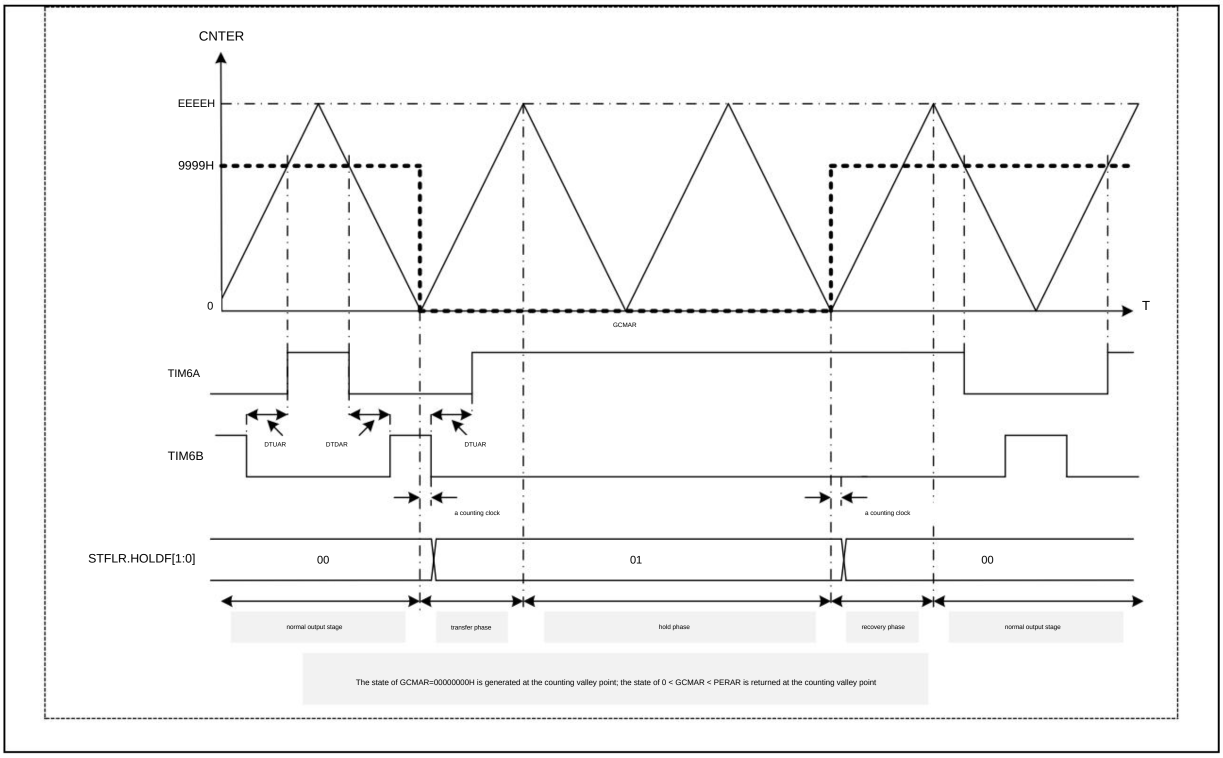

CNTER
GCMAR
EEEEH
9999H
0
T
TIM6A
TIM6B
DTUAR
DTDAR
STFLR.HOLDF[1:0]
00
10
00
normal output stage
hold phase
normal output stage
The state of GCMAR PERAR is generated at the count valley; the state of 0 < GCMAR < PERAR is returned at the count valley

Figure 10. Schematic of CHA and CHB output when GCMARÿPERAR

2. GCMAR = 0

not directly from GCMAR = 0 ÿ GCMAR ÿ PERAR



The state of GCMAR=00000000H is generated at the counting valley point; the state of 0 < GCMAR < PERAR is returned at the counting valley point

Figure 11. Schematic of CHA and CHB output when GCMAR=0

3.5 Protection Mechanisms

ADT has 4 protection mechanisms, as follows:

Forced output invalid condition 0: VC brake

Forced output invalid condition 1: The port output is the same as the high and the low level is braked

Forced Output Invalid Condition 2: Low Power Mode Brake

Forced Output Invalid Condition 3: Port Brake and Software Brake

When configuring the ADT general purpose port control register PCONR:

PCONR.DISSELA ÿ set which protection mechanism

PCONR.DISSELB ÿ set which protection mechanism

PCONR. DISVALA ÿ Set what level the CHA outputs when the forced output condition is met

PCONR. DISVALB ÿ Set what level CHB outputs when the forced output condition is met

When using the forced output invalid condition 3, it is necessary to configure the brake port, the effective level of the port brake signal and filter parameters.

AOSSR.BFILTEN ÿ enable port brake filter

AOSSR.BFILTS ÿ Filter Clock Selection

PTBKS ÿ Select Brake Port

PTBKP ÿ Set the active level of the brake port (H/L)

When the port brake occurs, the port brake flag will be set to 1 (AOSSR.FBRAKE)

If you want to resume the output PWM after the port brake occurs, you need to clear the port brake flag (AOSCL.FBRAKE)

3.6 Internal Interconnection

Through the internal interconnection function, the TIM4/5/6 can control the AOS interrupt signal or control the trigger ADC through the interrupt.

For example, an underflow match triggers the ADC:

When CR.UDFE is set to 1, when CNTER underflows match, ADC sampling is started at the same time.

In the ADT module of the HC32L136/L130 family, there are also two dedicated compare reference registers (SCMAR and SCMBR), in the interrupt control register (ICONR), SCMAR or SCMBR can be enabled to trigger ADC. The relevant bit (CR.CMSAE or CR.CMSBE) is also enabled in the control register CR, when the value of CNTER matches the ADC sampling can also be started when SCMAR or SCMBR match. To enable DMA transfer, it is also required in CR Enable related control bits.

4 Reference samples and drivers

Through the above introduction, with the user manual of Huada Semiconductor MCU* series, we can understand ADVANCED TIMER

Methods and precautions as a multifunctional PWM generator.

Huada Semiconductor (HDC) officially provides the application sample and driver library of this module at the same time. Users can open the sample by opening the

The project is further familiar with the application of this module and the driver library, and can also directly refer to the sample and use the driver in the actual development.

Dynamic library to quickly implement the operation of the module.

ÿ Example reference: ~/HC32L110_DDL/example/adt

~/HC32F003_DDL/example/adt

~/HC32F005_DDL/example/adt

~/HC32L136_DDL/example/adt;

~/HC32L130_DDL/example/adt;

ÿ Driver library reference: ~/HC32L110_DDL/driver/…/adt

~/HC32F003_DDL/driver/…/adt

~/HC32F005_DDL/driver/…/adt

~/HC32L136_DDL/driver/…/adt;

~/HC32L130_DDL/driver/…/adt;

5 Summary

The above chapters briefly introduce the multifunctional PWM generator of the ADVANCED TIMER module of Huada Semiconductor MCU*

In the actual application development process, if the user needs to further understand the use method and operation of the module

items, the corresponding user manual shall prevail. The samples and driver libraries mentioned in this chapter can be used as further experiments for users

With learning, it can also be directly applied in actual development.

* See the cover for supported models.

6 Other information

Technical support information: www.hdsc.com.cn

7 Version Information & Contact Information

date	Version revision record
2018/6/4	The first version of Rev1.0 is released.
2018/6/19	Rev1.1 adds supported models.
2018/9/6	Rev1.2 update supported models.

If you have any comments or suggestions in the process of purchasing and using, please feel free to contact us.

Email: mcu@hdsc.com.cn

Website: www.hdsc.com.cn

Mailing address: No. 39, Lane 572, Bibo Road, Zhangjiang Hi-Tech Park, Shanghai

Postcode: 201203