Product Features

- 32MHz Cortex-M0+ bit32 CPU platform
- HC32L110 series with flexible power management system, ultra-low power performance
  - 0.5μA @ 3V deep sleep mode: power consumption when all clocks are off, power-on reset active, IO state hold, IO interrupt active, all registers, RAM and CPU data save state
  - 1.0μA @3V deep sleep mode + RTC operation
  - 6μA@32.768kHz Low-speed operating mode: CPU and peripheral module running, program running from flash
  - 203μA/MHz@V@16MHz Sleep mode: CPU stops working, peripheral modules run, master clock runs
  - 120μA/MHz@3V@16MHz Operating mode: CPU and peripheral module running, program running from Flash
  - 4μs ultra-low power wake-up time, making mode switching more flexible and efficient, and system response more agile
  - The above characteristics are typical values at room temperature, refer to the electrical characteristics chapter for specific electrical characteristics and power consumption characteristics
- 16K/32K bytes Flash memory with erase protection
- 2K/4K bytes of RAM memory with parity check for enhanced system stability
- General purpose I/O pins (16IO/20pin, 12IO/16pin)
- Clocks, crystals
  - External High Speed Crystal 4~32MHz
  - External low-speed crystal 32.768KHz

  -Internal high-speed clock 4/8/16/22.12/24MHz
  - Internal low-speed clock 32.8/38.4KHz
  - Hardware support for internal and external clock calibration and monitoring
- Timer /Counter
  - 3 One general-purpose bit 16timer/counter
  - 3 High performance bit 16timer/counter with PWM support

    Complementary, dead zone protection function

  - 1 low-power bit 16timer/counter
  - 1 Programmable bit 16timer/counter, capture comparison support, PWM output
  - 1 Single-bit 20programmable count watchdog circuit with built-in dedicated ultra-low power RC-OSC for WDT counting
- Communication Interface
  - UART0-UART1 Standard communication interface
  - LPUART supports ultra-low power communication interface using low-speed clock
  - SPI standard communication interface
  - ^{2}IC standard communication interface
- Buzzer frequency generator with complementary output support
- Hardware Perpetual Calendar RTC Module
- Hardware CRC-16 Module
- Unique Byte10 ID Number
- 12 High-speed, high-precision SARADC with 1Msps sampling and built-in op-amp for measuring weak external signals
- Integrated Bit 26DAC and Programmable Reference Inputs for the VC
- Integrated low voltage detector LVD with configurable 16order comparison level to monitor port voltage as well as supply voltage
- Embedded debugging solution providing a full-featured real-time debugger
- Operating temperature: -40～85℃
- Operating voltage: 1.8~5.5V
- Package Type: QFN20,TSSOP20,TSSOP16,CSP16

Support Model

HC32L110C6UA	HC32L110C6PA
HC32L110C4UA	HC32L110C4PA
HC32L110B6PA	HC32L110B4PA
HC32L110B6YA	

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Catalog

1. Introduction

The HC32L110 series is an ultra-low power, low pin count, wide voltage MCU designed to extend the battery life of portable measurement systems, integrating a 121Msps high precision SARADC and a rich communication peripheral such as comparator, multi UART, SPI, ^{2}IC, etc. with high integration, high interference immunity, high reliability and ultra-low power consumption. It is characterized by high integration, high interference immunity, high reliability and ultra-low power consumption. The core of the product adopts Cortex-M0+ kernel, with mature Keil & IAR debugging development software, supporting C and assembly language, assembly instructions.

Ultra Low Power MCU Typical Applications

- Sensor applications, IoT applications.
- Intelligent transportation, smart cities, smart homes.
- Intelligent sensor applications such as fire probes, smart door locks, wireless monitoring, etc..
- A variety of battery-powered and power-critical portable devices, etc.

32 Bit CORTEX M0+ Kernel

The ARM® Cortex®-M0+ processor is derived from the Cortex-M0 and includes a bit 32RISC processor with 0.95Dhrystone MIPS/MHz computing power, and incorporates several new designs to improve debugging and traceability, reduce the number of instruction cycles per instruction (IPC), and improve the two-stage pipeline for Flash access, as well as incorporating power saving technologies. The Cortex-M0+ processor fully supports the integrated Keil & IAR debuggers.

The Cortex-M0+ includes a hardware debug circuit that supports a 2-pin SWD debug interface.

ARM Cortex-M0+ Features.

Instruction set	Thumb / Thumb-2
Flow line	2Level assembly line
Performance Efficiency	2.46 CoreMark / MHz
Performance Efficiency	0.95 DMIPS / MHz in Dhrystone
Interruptions	32Fast break
Interrupt priority	Configurable4 level interrupt priority
Enhanced Instructions	Single-cycle 32bit multiplier
Debugging	Serial-wire debug port with4 a hard interrupt (break point) and2 a watch point

16K/32K Byte Flash

Built-in fully integrated Flash controller, no need for external high voltage input, high voltage is generated by fully built-in circuit to program. Supports ISP, IAP, ICP functions.

2K/4K Byte RAM

Depending on the customer's choice of ultra-low power mode, RAM data are retained. With its own hardware parity bit, in case the data is accidentally corrupted, the hardware circuitry will generate an interrupt immediately when the data is read to ensure the reliability of the system.

Clock System

A high-precision internal clock RCH with a configurable frequency of 4~24MHz, a wake-up

time of 4μs from low-power mode to operating mode at a configurable 16MHz, and a small frequency deviation over the full voltage and temperature range, allowing the elimination of expensive external high-frequency crystals.

An external crystal XTH with a frequency of 4 to 32 MHz.

An external crystal XTL at 32.768KHz, mainly providing the RTC real-time clock. An internal clock RCL at 32.8/38.4KHz.

Working mode

1) Active Mode: CPU is running and peripheral function modules are running.
2) Sleep Mode: CPU stops running and peripheral function modules are running.
3) Deep sleep mode: CPU stops running, high-speed clock stops running, and low-power function module runs.

Real Time Clock RTC

The RTC (Real Time Counter) is a register supporting BCD data, using 32,768Hz crystal as its clock, enabling perpetual calendar function with interrupt period configurable as year/month/day/hour/minute/second. 24/12 hour time mode with hardware automatic leap year correction. Accuracy compensation up to 0.96ppm with internal temperature sensor or external temperature sensor and software +1/-1 adjustment of year/month/day/hour/minute/second with minimum adjustable accuracy of 1 second.

The RTC calendar recorder for time and date indication does not erase the reserved value when the MCU is reset by external factors, making it the best choice for measurement equipment instruments that require a permanent, high-precision real-time clock.

Port Controller GPIO

Up to 16 GPIO ports are available, with some GPIOs multiplexed with analog ports. Each port is controlled by a separate control register bit. Edge-triggered interrupts and level-triggered interrupts are supported to wake up the MCU to operating mode from various ultra-low power modes. Supports Push-Pull CMOS push-pull output and Open-Drain open-drain output. Built-in pull-up resistor, pull-down resistor, and Schmitt trigger input filtering function. Output drive capability is configurable, supporting up to 12mA current drive capability. 16 External asynchronous interrupts can be supported for each general-purpose IO.

Interrupt Controller NVIC

The Cortex-M0+ processor has a built-in nested vector interrupt controller (NVIC) which supports up to one32 interrupt request (IRQ) input; it has four interrupt priority levels to handle complex logic and is capable of real-time control and interrupt processing.

32 The interrupt entry vector addresses, respectively, are

Interrupt vector number	Interruption source
[0]	GPIO_P0
[1]	GPIO_P1
[2]	GPIO_P2
[3]	GPIO_P3
[4]	-
[5]	-
[6]	UART0
[7]	UART1
[8]	LPUART
[9]	-
[10]	SPI
[11]	-
[12]	^{2}IC
[13]	-
[14]	Timer0
[15]	Timer1
[16]	Timer2
[17]	LPTimer
[18]	Timer4
[19]	Timer5
[20]	Timer6
[21]	PCA
[22]	WDT
[23]	RTC
[24]	ADC
[25]	-
[26]	VC0
[27]	VC1
[28]	LVD
[29]	-
[30]	RAM FLASH fault
[31]	Clock trim

Reset controller RESET

This product has 7 sources of reset signals, each of which allows the CPU to run again, most registers will be reset, and the program counter PC will be reset to point00000000 .

	Reset Source
[0]	Power-On Power-Off Reset POR BOR
[1]	External Reset Pin Reset
[2]	WDT reset
[3]	PCA reset
[4]	Cortex-M0+ LOCKUP Hardware Reset
[5]	Cortex-M0+ SYSRESETREQ Software Reset
[6]	LVD reset

Timer TIM

		Bit width	Pre-defrequency	Counting direction	PWM	Capture	Complementary output
Basic Timer	Timer0	16/32	1/2/4/8/16 32/64/256	Upper count	None	None	None
	Timer1	16/32	1/2/4/8/16/ 32/64/256	Upper count	None	None	None
	Timer2	16/32	1/2/4/8/16/ 32/64/256	Upper count	None	None	None
Low power timer	LPTimer	16	None	Upper count	None	None	None
Programmable Counting Array	PCA	16	2/4/8/16/32	Upper count	5	5	None
Advanced Timer	Timer4	16	1/2/4/8/16/ 64/256/1024	Upper count/ Lower count/ Up and down counting	2	2	1
	Timer5	16	1/2/4/8/16/ 64/256/1024	Upper count/ Lower count/ Up and down counting	2	2	1
	Timer6	16	1/2/4/8/16/ 64/256/1024	Upper count/ Lower count/ Up and down counting	2	2	1

The basic timer contains three timers Timer0/1/2. Timer0/1/2 are identical in function. timer0/1/2 are synchronous timers/counters that can be used as timers/counters with bit 16auto reload function or as timers/counters with bit 32no reload function. timer0/1/2 can count

external pulses or implement system timing.

Low-power timers are asynchronous bit16 timers/counters that can be timed/counted by internal low-speed RC or external low-speed crystal oscillation even after the system clock is turned off. The system wakes up in low-power mode via interrupts.

The PCA (Programmable Counter Array) supports capture/compare modules of up to one 5bit16. Each module of the PCA can be programmed independently to provide input capture, output comparison, or pulse width modulation. An additional watchdog timer mode is available for Module 4.

The Advanced Timer is a high performance counter containing three timers, Timer4/5/6, which are identical in function and can be used to generate different forms of clock waveforms by counting, and 1each timer can generate a complementary pair of PWM or independent 2PWM outputs that can capture external inputs for pulse width or period measurements.

The basic functions and features of the advanced timer are shown in the table.

Waveform mode	Sawtooth wave, triangle wave
Basic Functions	• Incremental and decremental counting direction
	• Software Synchronization
	• Hardware Synchronization
	• Cache function
	• Orthogonal coding count
	• Universal PWM output
	• Protection mechanism
	• AOS associated actions
Interrupt Type	Counting comparison match interrupts
	Counting cycle matching interrupts
	Dead time error interrupt
	Short circuit monitoring interruption

Watchdog WDT

The WDT (Watch Dog Timer) is a configurable 20-bit timer that provides a reset in the event of an MCU exception; the built-in 10K

Low-speed clock input as counter clock. Debug mode with the option to pause or resume operation; the WDT can be restarted only by writing a specific sequence.

Universal synchronous asynchronous transceiver UART0~UART1, LPUART

2 Universal Asynchronous Receiver/Transmitter (UART) Basic functions

of Universal UART.

- Half-duplex and full-duplex transmission
- 8/9-Bit Transfer Data Length
- Hardware Parity Check
- Bit 1stop bit support

- Four different transmission modes
- Multi-machine communication
- Hardware address recognition

1 Low Power Universal Asynchronous Receiver/Transmitter (LPUART) Basic functions.

- Transmission clock SCLK (SCLK is selectable from XTL, RCL, and PCLK)
- Sending and receiving data in system low-power mode
- Half-duplex and full-duplex transmission
- 8/9-Bit Transfer Data Length
- Hardware Parity Check
- Bit 1stop bit support
- Four different transmission modes
- Multi-machine communication
- Hardware address recognition

Serial Peripheral Interface SPI

1 Serial Peripheral Interface (SPI) supporting master-slave mode. SPI Basic Features.

- Can be programmed as a master or slave
- Four-wire transmission method, full duplex communication
- Host mode Configurable 7baud rate
- Host mode with a maximum crossover factor of PCLK/2 and a maximum communication rate of 16M bps
- Slave mode with a maximum crossover factor of PCLK/8 and a maximum communication rate of 4M bps
- Configurable serial clock polarity and phase
- Interruption support
- 8 Bit data transfer, high bit first then low bit

^{2}IC Bus

1 I2C basic features.

- Support host transmit/receive, slave transmit/receive four working modes
- Support Standard(100Kbps) / Fast(400Kbps) / High Speed(1Mbps) three operating rates
- Support Bit7 Addressing Function
- Support noise filtering function
- Broadcast address support
- Support interrupt status query function

Buzzer Buzzer

3 A basic timer and a 1low-power timer function are multiplexed to provide a programmable drive frequency for the Buzzer. The buzzer port provides 12mA of sink current with complementary outputs, eliminating the need for an additional triode.

Clock Calibration Circuit Module CLKTRIM

The built-in clock calibration circuit allows you to calibrate the internal RC clock with an accurate external crystal clock, or use the internal RC clock to verify that the external crystal clock is working properly.

Basic clock calibration characteristics.

- Calibration Mode
- Monitoring Mode
- 32-bit reference clock counter can be loaded with initial values
- 32 Bit to be calibrated clock counter configurable overflow value
- 6 Reference clock sources
- 4 Various clock sources to be calibrated
- Support interrupt method

Electronic signature of devices

Each chip is shipped with a unique byte10 device identification number, including wafer lot information, and chip coordinate information, etc. ID address

0x0010_0E74-0x0010_0E7F

Cyclic Redundancy Check CRC

Conforms to the polynomial $F(x)=X^{16}+X^{12}+X^5+1$ given in ISO/IEC13239.

Analog to Digital Converters ADC

The reference voltage can be selected from an on-chip precision voltage (1.5V or 2.5V) or from an external input or supply voltage. 12 The ADC has two input channels, including an 9external pin input, 1 an internal temperature sensor voltage, 1 a 1/3 supply voltage, and an 1internal BGR 1.2V voltage. A configurable input signal amplifier is built in to detect weak signals.

SAR ADC Basic Features.

- 12 Bit conversion accuracy.
- 1Msps conversion speed.
- 12 The following inputs are available: an 8external pin input, 1 an internal temperature sensor voltage, 1 a VCC/3 voltage, a 1built-in

  BGR 1.2V voltage.
- 4 (a) Two reference sources: VCC voltage, ExRef pin, built-in 1.5V reference voltage, built-in 2.5V reference voltage.
- Voltage input range of the ADC: 0 to Vref.
- 3 (a) Conversion modes: single conversion, sequential scan continuous conversion, continuous conversion accumulation.
- Input channel voltage threshold monitoring.
- Software configurable ADC conversion rate.
- Built-in signal amplifier for converting high-resistance signals.
- Supports on-chip peripherals to automatically trigger ADC conversion, effectively reducing chip power consumption and improving the real-time conversion.

Analog Voltage Comparator VC

Chip pin voltage monitoring/comparison circuitry. 8 Configurable positive/negative external input channels; 5 internal input channels, including 1internal temperature sensor voltage, 1 internal BGR 2.5V reference voltage, 1internal BGR 1.2V voltage, 1 and 64step resistor voltage divider. Asynchronous interrupts can be generated based on rising/falling edges to wake up the MCU from low-power mode. configurable software

antijitter function.

Low Voltage Detector LVD

The chip power supply voltage or the chip pin voltage is detected.16 The voltage monitoring value (1.8~3.3V) Can be generated based on rising/falling edges

Asynchronous interrupt or reset. Features hardware hysteresis circuitry and configurable software antijitter.

LVD Basic characteristics.

- 4 Road monitoring sources, VCC, PC13, PB08, PB07.
- 16 Order threshold voltage, 1.8 to 3.3V selectable.
- 8 A combination of trigger conditions, high, rising and falling edges.
- 2 kind of trigger result, reset, interrupt.
- 8 Order filtering configuration to prevent false triggering.
- With hysteresis function, strong anti-interference.

Embedded debugging system

Embedded debugging solution, providing a full-featured real-time debugger with standard and mature debugging development software such as Keil/IAR. Support 4

There are two hard breakpoints and several soft breakpoints.

Programming Mode

One programming mode is supported: offline programming.

Two programming protocols are

supported: ISP protocol, SWD protocol.

programming interface for ISP protocol:

P35, P36 or P27, P31. programming

interface for SWD protocol: P27, P31.

When the chip **receives** an **ISP** programming command within a few milliseconds time window after the reset is completed, the chip operates in ISP programming mode and the FLASH can be programmed using the programmer.

When the chip **does not receive** an **ISP** programming instruction within a window of several milliseconds after the reset is completed, the chip works in user mode and the chip executes

The program code

inside FLASH.

Caution.

- **It is recommended to reserve P35, P36 as ISP programming interface; if you want to use**

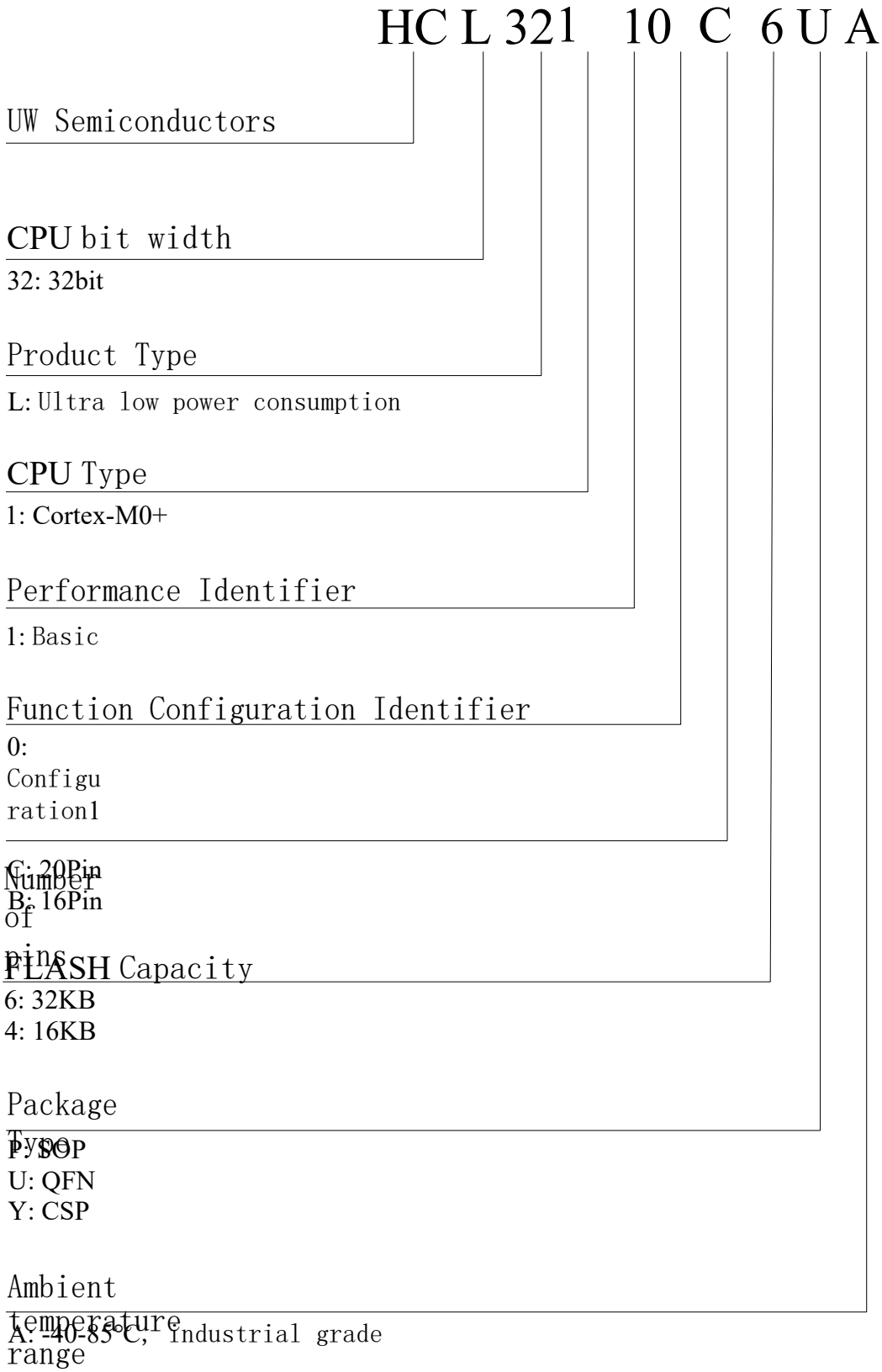
P27, P31 as ISP programming interface, please refer to PCN: PCN20200304-1_HC32L110HC32F003HC32F005 to improve the burn-in speed.

High security

Encrypted embedded debugging solution that provides a full-featured real-time debugger.

2. Product Lineup

Product Name



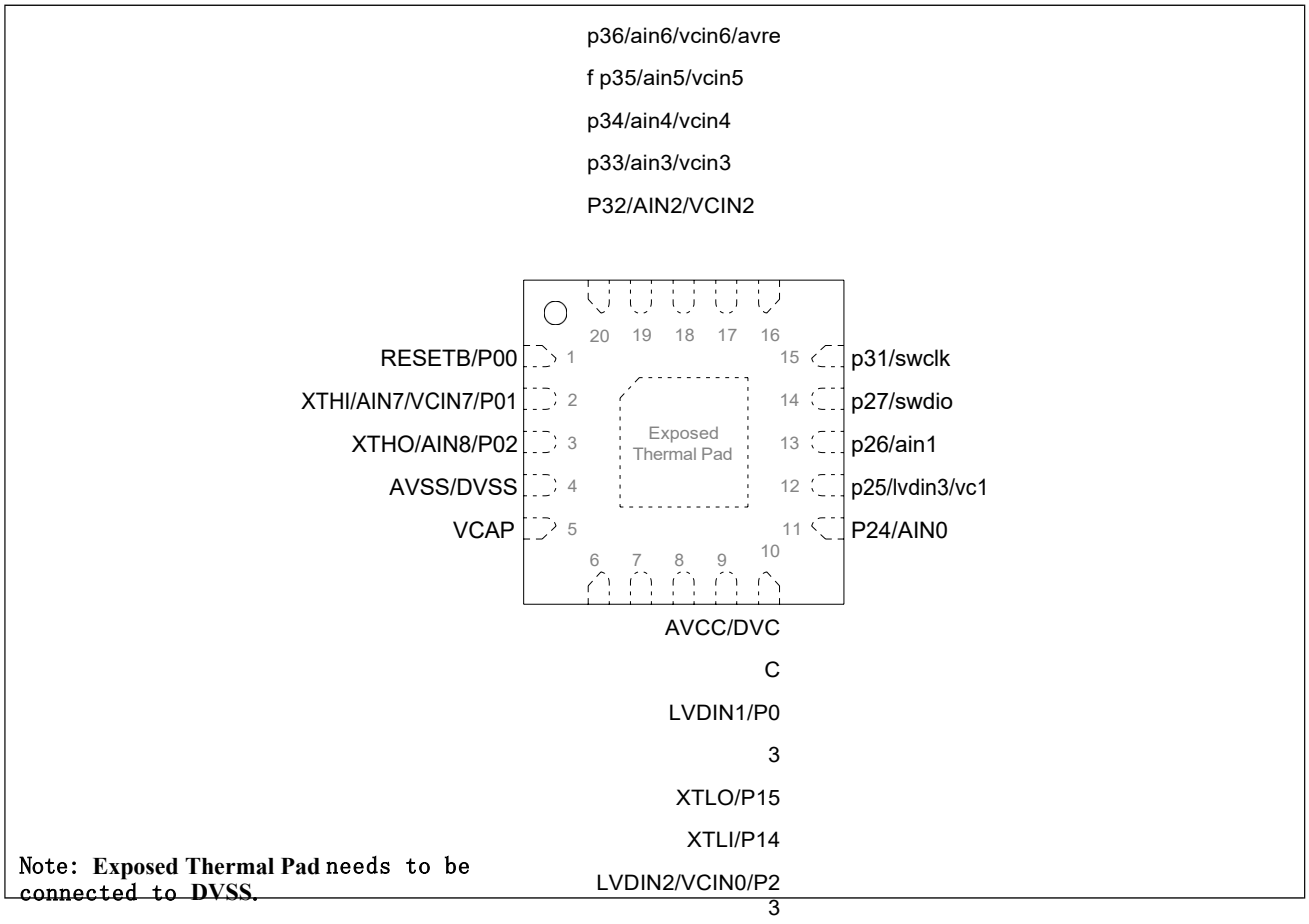
Function

Product Name		hc32l110c6ua / hc32l110c6pa hc32l110c4ua / hc32l110c4pa	HC32L110B4PA / HC32L110B6PA HC32L110B6YA
Number of pins		20	16
Number of GPIO pins		16	12
CPU	Kernel	Cortex M0+	
	Frequency	32MHz	
Power supply voltage range		1.8 ~5.5V	
Single/dual power supply		Single power supply	
Temperature range		-40 ~ 85°C	
Debugging functions		SWD Debugging Interface	
Unique Identification Code		Support	
Communication Interface		UART0/1 LPUART SPI ^{2}IC	
Timer		Universal Timer TIM0/1/2 Low Power Timer LPTIM Advanced Timer TIM4/5/6	
12 Bit A/D converters		9ch	6ch
Analog Voltage Comparator		VC0/1	
Real Time Clock		1	
Port Interruptions		16	12
Low voltage detection reset/interrupt		1	
Clock	Internal high-speed oscillator	RCH 4/8/16/22.12/24MHz	
	Internal low-speed oscillator	RCL 32.8/38.4KHz	
	External high-speed crystal oscillator	4~32MHz	
	External low-speed crystal oscillator	32.768kHz	
Buzzer		Max 4ch	
FLASH Security Protection		Support	

Product Name	hc32l110c6ua / hc32l110c6pa hc32l110c4ua / hc32l110c4pa	HC32L110B4PA / HC32L110B6PA HC32L110B6YA
RAM Parity Check	Support	

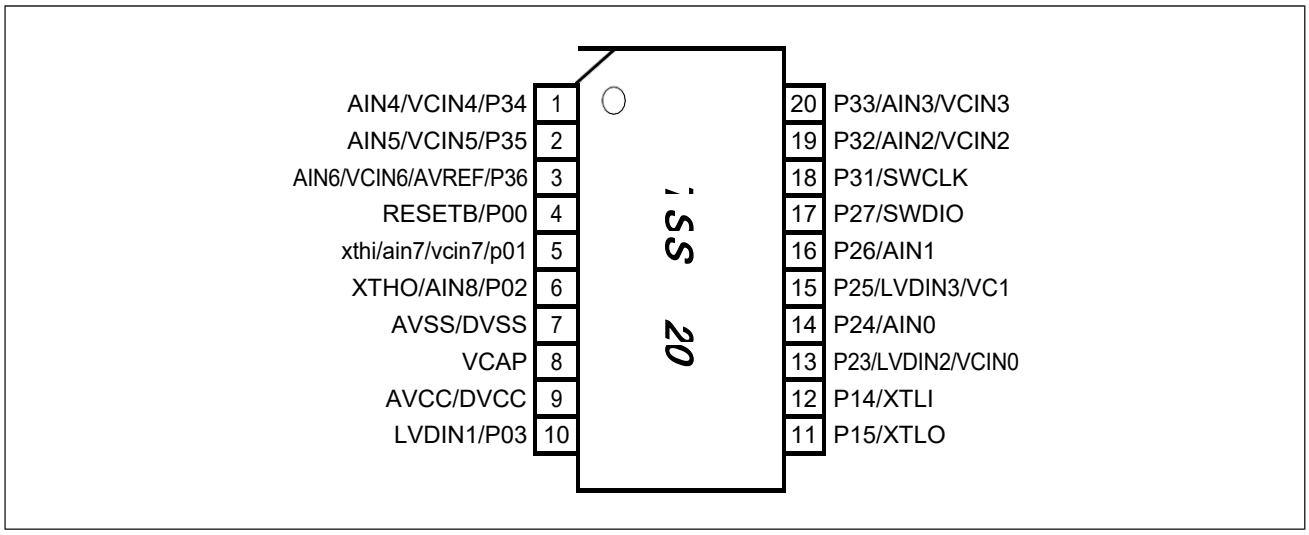
3. Pin Configuration

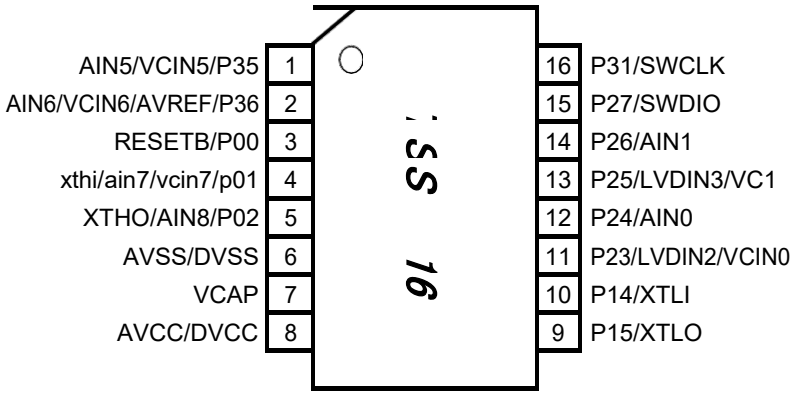
HC32L110C6UA / HC32L110C4UA



Note: **Exposed Thermal Pad** needs to be connected to DVSS.

HC32L110C6PA / HC32L110C4PA

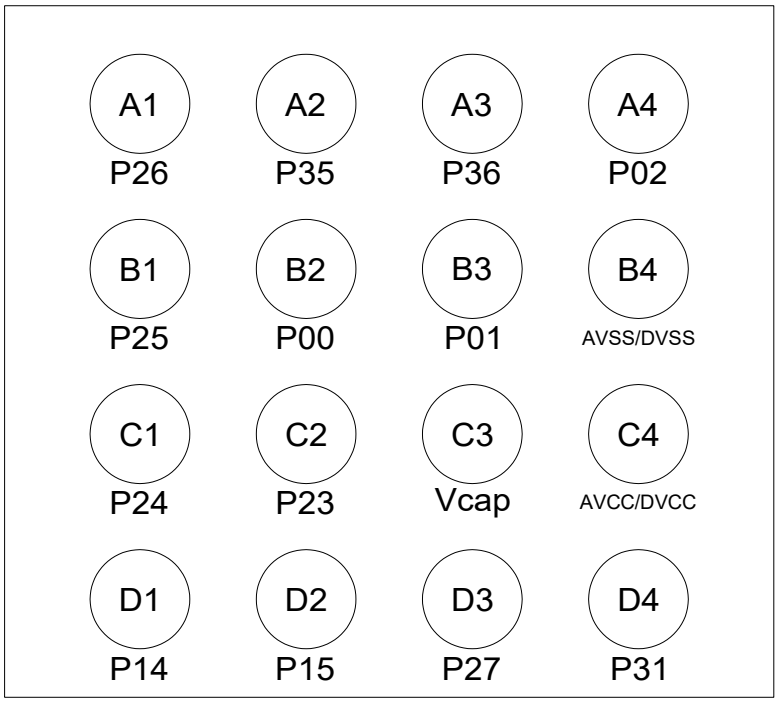




Note: In the application, it is necessary to set the unpinned **IO** pin of this package relative to the **TSSOP20** as an input and enable the pull-up.

HC32L110B6YA

CSP16 TOP VIEW



Notes.

- In the application, the unpinned **IO** pins of this package relative to the **TSSOP20** need to be set as inputs and enabled for pull-up.
- **A1 is Pin 1.**

4. Pin Function Description

Pin No. QFN20	Pin No. TSSOP20	Pin No. TSSOP16	Pin No. CSP16	Pin Name	Pin Type	Description
1	4	3	B2	RESETB P00	RESETB	Reset input port, active low, chip reset
					GPIO	P00 Digital input
2	5	4	B3	P01	GPIO	P01 General purpose digital input/output pins
					UART0_RXD	UART0 RXD
					^{2}IC_SDA	^{2}IC Data
					UART1_TXD	UART1 TXD
					TIM0_TOG	Timer0 Flip output
					TIM5_CHB	Timer5 Capture input/compare output B
					SPI_SCK	SPI Clock
					TIM2_EXT	Timer2 external clock
					AIN7/VC7	Analog Inputs
					XTHI	External XTH crystal clock input
3	6	5	A4	P02	GPIO	P02 General purpose digital input/output pins
					UART0_TXD	UART0 TXD
					^{2}IC_SCL	^{2}IC Clocks
					UART1_RXD	UART1 RXD
					TIM0_TOGN	Timer0 Flip Inverted Output
					TIM6_CHA	Timer6 Capture input/compare output A
					SPI_CS	SPI CS
					TIM2_GATE	Timer2 Gate Control
					AIN8	Analog Inputs
					XTHO	External XTH crystal clock output
4	7	6	B4	AVSS/DVSS	GND	Chip Land
5	8	7	C3	Vcap	Power	LDO core supply output (internal circuitry only) (Use, connect 4.7uF capacitor)
6	9	8	C4	AVCC/DVCC	Power	Chip power supply 1.8v~5.5v
7	10	Note	Note	P03	GPIO	P03 General purpose digital input/output pins
					PCA_CH3	PCA capture input/compare output 3
					SPI_CS	SPI CS
					TIM6_CHB	Timer6 Capture input/compare output B
					LPTIM_EXT	LPTimer external clock input
					RTC_1HZ	RTC 1Hz output
					PCA_ECI	PCA external clock input
					VC0_OUT	VC0 Output
					LVDIN1	Analog Inputs
8	11	9	D2	P15	GPIO	P15 General purpose digital input/output pins
					^{2}IC_SDA	^{2}IC Data

					TIM2_TOG	Timer2 Flip Output
					TIM4_CHB	Timer4 Capture input/compare output B
					LPTIM_GATE	LPTimer door control
					SPI_SCK	SPI Clock

Pin No. QFN20	Pin No. TSSOP20	Pin No. TSSOP16	Pin No. CSP16	Pin Name	Pin Type	Description
					UART0_RXD	UART0 RXD
					LVD_OUT	LVD Output
					XTLO	External XTL crystal clock output
9	12	10	D1	P14	GPIO	P14 General purpose digital input/output pins
					^{2}IC_SCL	^{2}IC Clocks
					TIM2_TOGN	Timer2 Flip Inverted Output
					ECI	PCA external clock input
					ADC_RDY	ADC ready
					SPI_CS	SPI CS
					UART0_TXD	UART0 TXD
					XTLI	External XTL crystal clock input
10	13	11	C2	P23	GPIO	P23 General purpose digital input/output pins
					TIM6_CHA	Timer6 Capture input/compare output A
					TIM4_CHB	Timer4 Capture input/compare output B
					TIM4_CHA	Timer4 Capture input/compare output A
					PCA_CH0	PCA capture input/compare output 0
					SPI_MISO	SPI module host input slave output data signal
					UART1_TXD	UART1 TXD
					IR_OUT	38K carrier output
					LVDIN2/VC0	Analog Inputs
11	14	12	C1	P24	GPIO	P24 General purpose digital input/output pins
					TIM4_CHB	Timer4 Capture input/compare output B
					TIM5_CHB	Timer5 Capture input/compare output B
					HCLK_OUT	HCLK Output
					PCA_CH1	PCA capture input/compare output 1
					SPI_MOSI	SPI module host output slave input data signal
					UART1_RXD	UART1 RXD
					VC1_OUT	VC1 Output
					AIN0	Analog Inputs
12	15	13	B1	P25	GPIO	P25 General purpose digital input/output pins
					SPI_SCK	SPI Clock
					PCA_CH0	PCA capture input/compare output 0
					TIM5_CHA	Timer5 Capture input/compare output A
					LVD_OUT	LVD Output
					LPUART_RXD	LPUART RXD
					^{2}IC_SDA	^{2}IC Data
					TIM1_GATE	Timer1 Gate Control
					LVDIN3/VC1	Analog Inputs
13	16	14	A1	P26	GPIO	P26 General purpose digital

						input/output pins
					SPI_MOSI	SPI module host output slave input data signal
					TIM4_CHA	Timer4 Capture input/compare output A
					TIM5_CHB	Timer5 Capture input/compare output B
					PCA_CH2	PCA capture input/compare output 2
					LPUART_TXD	LPUART TXD
					^{2}IC_SCL	^{2}IC Clocks

Pin No. QFN20	Pin No. TSSOP20	Pin No. TSSOP16	Pin No. CSP16	Pin Name	Pin Type	Description
					TIM1_EXT	Timer1 Part clock input
					AIN1	Analog Inputs
14	17	15	D3	P27	GPIO	P27 General purpose digital input/output pins
					SPI_MISO	SPI module host input slave output data signal
					TIM5_CHA	Timer5 Capture input/compare output A
					TIM6_CHA	Timer6 Capture input/compare output A
					PCA_CH3	PCA capture input/compare output 3
					UART0_RXD	UART0 RXD
					RCH_OUT	24M oscillation output
					XTH_OUT	32M oscillation output
					SWDIO	SWDIO
15	18	16	D4	P31	GPIO	P31 General purpose digital input/output pins
					TIM3_TOG	Timer3 Flip Output
					PCA_ECI	PCA external clock
					PCLK_OUT	PCLK Output
					VC0OUT	VC0 Output
					UART0_TXD	UART0 TXD
					RCL_OUT	RCL Oscillation Output
					HCLK_OUT	HCLK Output
					SWCLK	SWCLK
16	19	Note	Note	P32	GPIO	P32 General purpose digital input/output pins
					TIM3_TOGN	LPTimer Flip Reverse Output
					PCA_CH2	PCA capture input/compare output 2
					TIM6_CHB	Timer6 Capture input/compare output B
					VC1OUT	VC1 Output
					UART1_TXD	UART1 TXD
					PCA_CH4	PCA capture input/compare output 4
					RTC_1HX	RTC1HZ output
					AIN2/VC2	Analog Inputs
17	20	Note	Note	P33	GPIO	P33 General purpose digital input/output pins
					LPUART_RXD	LPUART RXD
					PCA_CH1	PCA capture input/compare output 1
					TIM5_CHB	Timer5 Capture input/compare output B
					PCA_ECI	PCA external clock
					UART1_RXD	UART1 RXD
					XTL_OUT	32K oscillation output
					TIM1_TOGN	Timer1 Flip reverse output
					AIN3/VC3	Analog Inputs
18	1	Note	Note	P34	GPIO	P34 General purpose digital input/output pins
					PCA_CH0	PCA capture input/compare output 0

					LPUART_TXD	LPUART TXD
					TIM5_CHA	Timer5 Capture input/compare output A
					TIM0_EXT	Timer0 Part clock input
					TIM4_CHA	Timer4 Capture input/compare output A
					RTC_1HZ	RTC1HZ output

Pin No. QFN20	Pin No. TSSOP20	Pin No. TSSOP16	Pin No. CSP16	Pin Name	Pin Type	Description
					TIM1_TOG	Timer1 Flip output
					AIN4/VC4	Analog Inputs
19	2	1	A2	P35	GPIO	P35 General purpose digital input/output pins
					UART1_TXD	UART1 TXD
					TIM6_CHB	Timer6 Capture input/compare output B
					UART0_TXD	UART0 TXD
					TIM0_GATE	Timer0 Gating
					TIM4_CHB	Timer4 Capture input/compare output B
					SPI_MISO	SPI module host input slave output data signal
					^{2}IC_SDA	^{2}IC Data
					AIN5/VC5	Analog Inputs
20	3	2	A3	P36	GPIO	P36 General purpose digital input/output pins
					UART1_RXD	UART1 RXD
					TIM6_CHA	Timer6 Capture input/compare output A
					UART0_RXD	UART0 RXD
					PCA_CH4	PCA capture input/compare output 4
					TIM5_CHA	Timer5 Capture input/compare output A
					SPI_MOSI	SPI module host output slave input data signal
					^{2}IC_SCL	^{2}IC Clocks
					AIN6/VC6/ AVREF	Analog Inputs

Note: The unpinned IO pins of this package relative to the TSSOP20 need to be set as inputs and enabled for pull-up.

5. Block Diagram

Function Modules

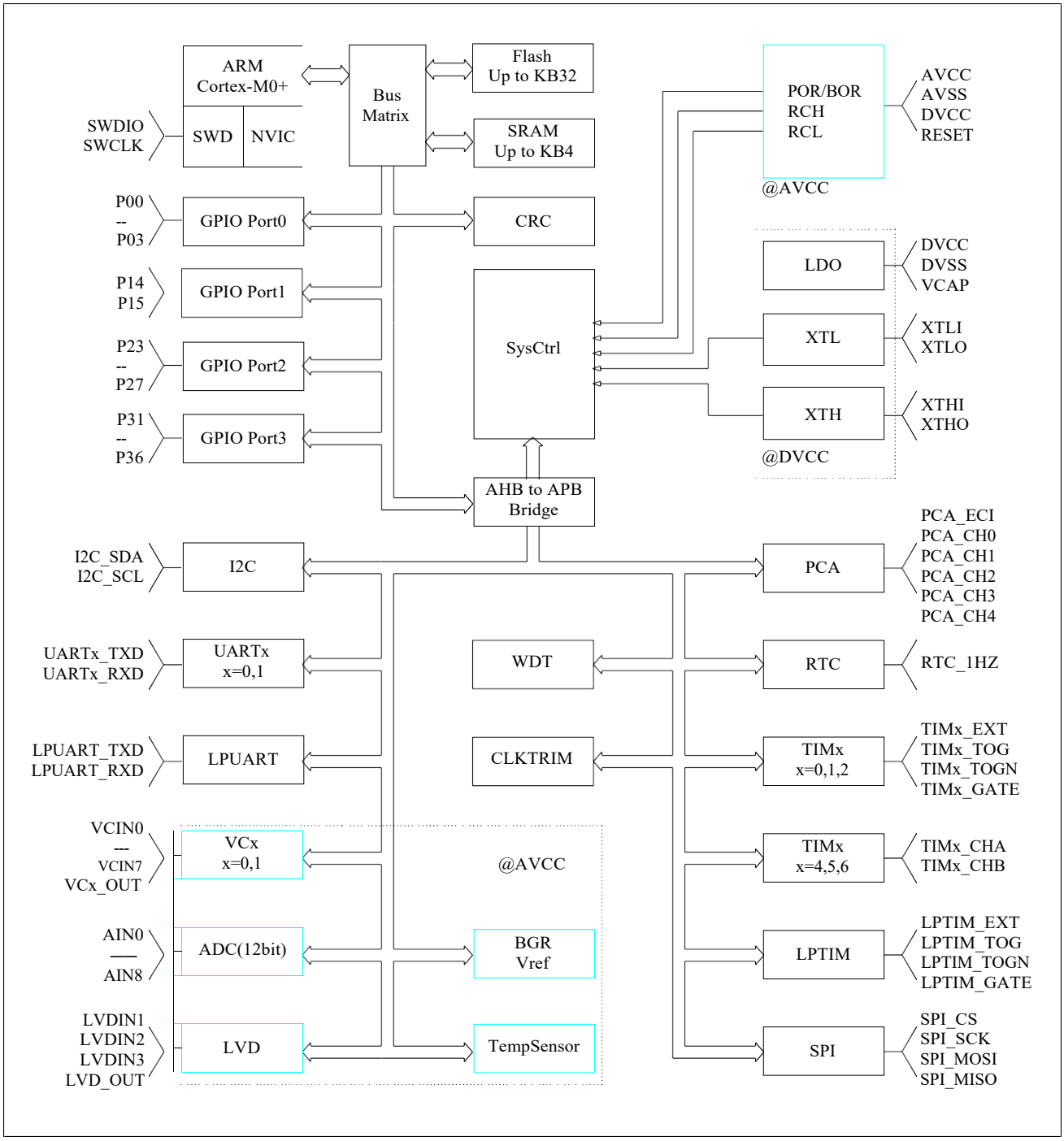
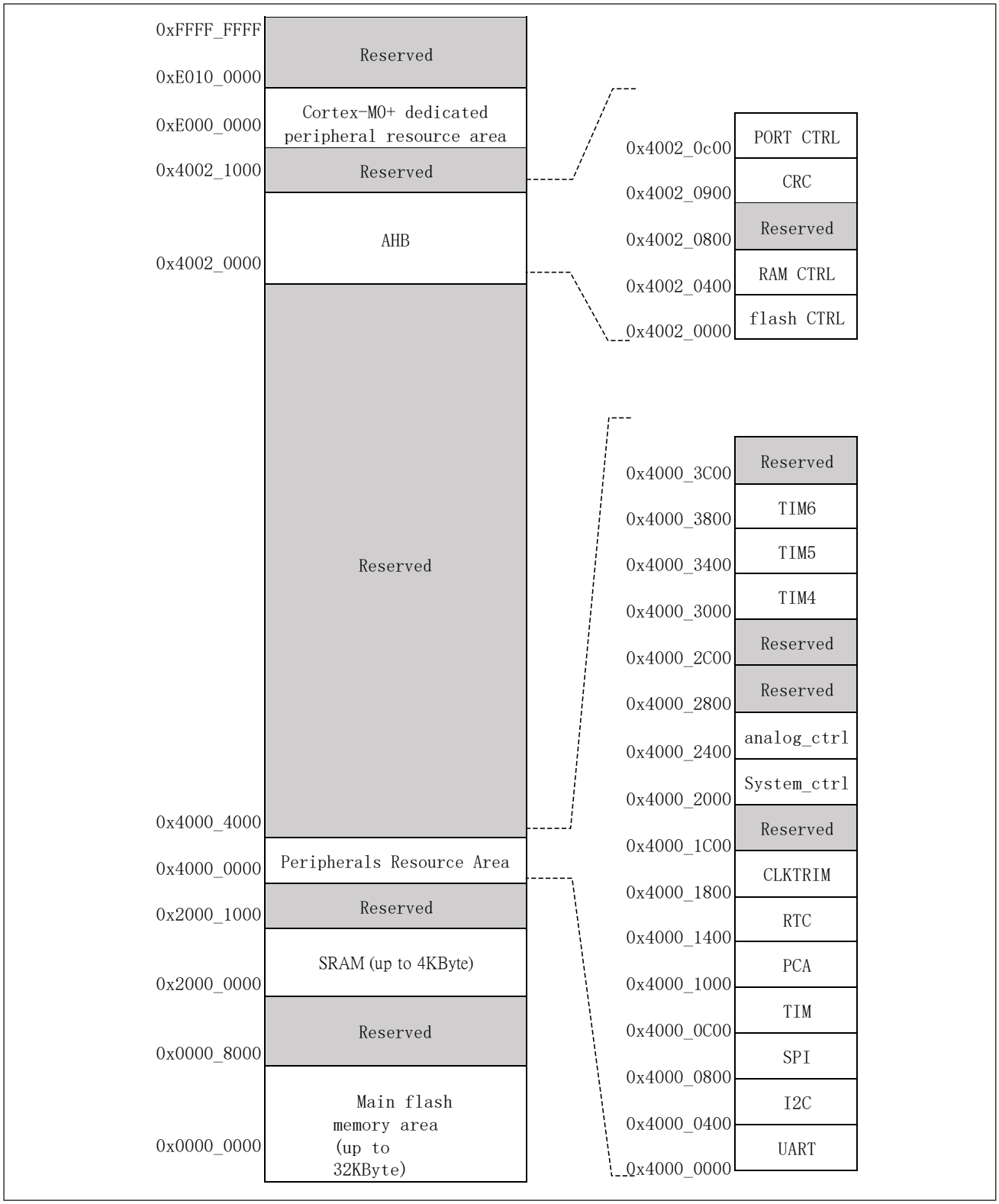
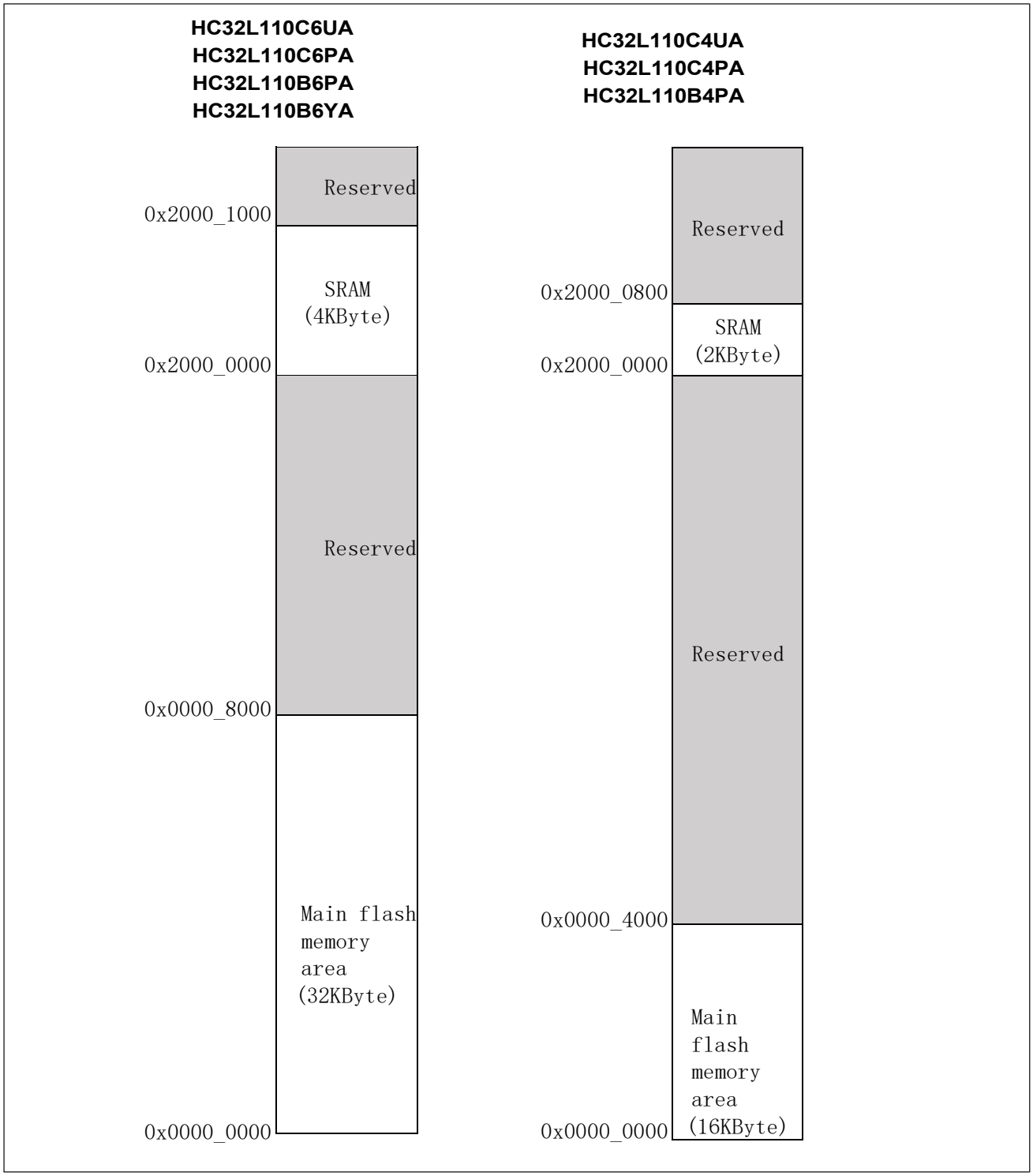


Figure 5-1 Function Module

6. Storage Area Mapping




HC32L110C6UA
HC32L110C6PA
HC32L110B6PA
HC32L110B6YA
Reserved
0x2000_1000
SRAM
(4KByte)
0x2000_0000
Reserved
0x0000_8000
Main flash
memory
area
(32KByte)
0x0000_0000
HC32L110C4UA
HC32L110C4PA
HC32L110B4PA
Reserved
0x2000_0800
SRAM
(2KByte)
0x2000_0000
Reserved
0x0000_4000
Main
flash
memory
area
(16KByte)
0x0000_0000

7. Electrical Characteristics

7.1 Test conditions

Unless otherwise noted, all voltages are referenced to VSS.

7.1.1. Minimum and maximum values

Unless otherwise specified, all minimum and maximum values will be guaranteed at the worst ambient temperature, supply voltage and clock frequency conditions by tests performed on 100% of the products in the production line at ambient temperature TA=25°C and TA=TAmax (TAmax matched to the selected temperature range).

The data obtained by comprehensive evaluation, design simulation and/or process characterization are described in the notes below each table and will not be tested on the production line; on the basis of the comprehensive evaluation, the minimum and maximum values are obtained by taking the average of the sample tests and then adding or subtracting three times the standard distribution (mean ± 3 sigma).

7.1.2. Typical values

Unless otherwise noted, typical data is based on TA=25°C and VCC=3.3V (1.8V ≤ VCC ≤ 5.5V voltage range). These data are for design guidance only and are not tested.

Typical ADC accuracy values are obtained by sampling a standard batch, tested at all temperature ranges, with 95% of the product having an error less than or equal to the value given (±2Σ on average).

7.2 Absolute maximum rating

Loads applied to the device that exceed the values given in the "Absolute Maximum Ratings" list may cause permanent damage to the device. This is only the maximum load that can be withstood and does not imply that the device will operate functionally under conditions will affect the reliability of the device.

Symbols	Description	Minimum value	Maximum value	Unit
VCC - VSS	External mains supply voltage (including AVCC and DVCC) (1)	-0.3	5.5	V
VIN	Input voltage on other pins(2)	VSS-0.3	VCC + 0.3	V
| ΔVCCx |	Voltage difference between different supply pins		50	mV
| VSSx - VSS |	Voltage difference between different ground pins		50	mV
VESD(HBM)	ESD electrostatic discharge voltage (human model)	Reference absolute maximum electrical parameters		V

Table 7-1 Voltage Characteristics

1. All power (DVCC, AVCC) and ground (DVSS, AVSS) pins must always be connected to an external supply system within the allowed range.
2. IINJ(PIN) must never exceed its limit, i.e. make sure that VIN does not exceed its maximum value. If it is not possible to guarantee that VIN does not exceed its maximum value, it is also necessary to ensure that the external limit I INJ(PIN) does not exceed its maximum value. When VIN>VCC, there is a forward injection current; when VIN<VSS, there is a reverse injection current.

Symbols	Description	Maximum value(1)	Unit
IVCC	Total current (supply current) through the DVCC/AVCC power line (1)	300	mA
IVSS	Total current (outflow current) through the VSS ground (1)	300	mA
IIO	Output supply current on arbitrary I/O and control pins	25	mA
	Output current on arbitrary I/O and control pins	-25	mA
IINJ(PIN) (2) (3)	Injection current of RESETB pin	+/-5	mA
	Injection current of XTHI pin of XTH and XTLI pin of XTL	+/-5	mA
	Injection current of other pins(4)	+/-5	mA
∑IINJ(PIN) (2)	Total injected current on all I/O and control pins(4)	+/-25	mA

Table 7-2 Current Characteristics

1. All power (DVCC,AVCC) and ground (DVSS,AVSS) pins must always be connected to a power supply system within the external allowable range.
2. IINJ(PIN) must never exceed its limit, i.e. make sure that VIN does not exceed its maximum value. If it is not possible to guarantee that VIN does not exceed its maximum value, it

is also necessary to ensure that the external limit $I_{INJ(PIN)}$ does not exceed its maximum value. When $V_{IN}>V_{CC}$, there is a forward injection current; when $V_{IN}<V_{SS}$, there is a reverse injection current.

3. Reverse injection current can interfere with the analog performance of the device.
4. The maximum value of $\sum I_{INJ(PIN)}$ is the sum of the immediate absolute values of the forward and reverse injection currents when several I/O ports have simultaneous injection currents. This result is based on the characteristics of the maximum value of $\sum IINJ(PIN)$ at each4 I/O port of the device.

Symbols	Description	Numerical value	Unit
T_{STG}	Storage temperature range	-60～+150	℃
T_J	Maximum junction temperature	105	℃

Table 7-3 Temperature Characteristics

7.3 Working conditions

7.3.1. General working conditions

Symbols	Parameters	Conditions	Minimum value	Maximum value	Unit
fHCLK	Internal AHB clock frequency		0	32	MHz
fPCLK	Internal APB clock frequency		0	32	MHz
DVCC	Digital section operating voltage		1.8	5.5	V
AVCC(1)	Analog section operating voltage	Must be the same as DVCC(2)	1.8	5.5	V
PD	Power dissipation TA=85℃	TSSOP20		283	mW
TA	Ambient temperature	Maximum power consumption	-40	85	℃
		Low power consumption(3)	-40	105	℃
TJ	Knot temperature range		-40	105	℃

Table 7-4 General working conditions

1. When using an ADC, see ADC Electrical Parameters.
2. It is recommended that the same power supply be used to power both DVCC and AVCC, allowing a maximum difference of 300mV between DVCC and AVCC during power-up and normal operation.
3. At lower power dissipation states, the $_{TA}$ can be extended to this range as long as $_{TJ}$ does not exceed $_{TJmax}$.

7.3.2. Operating conditions at power-up and power-down

Symbols	Parameters	Conditions	Minimum value	Maximum value	Unit
tVcc	VCC rise rate		0	∞	μs/V
tVcc	VCC drop rate		10	∞	μs/V

Table 7-5 Power-up and power-down operating conditions

7.3.3. Embedded reset and LVD module features

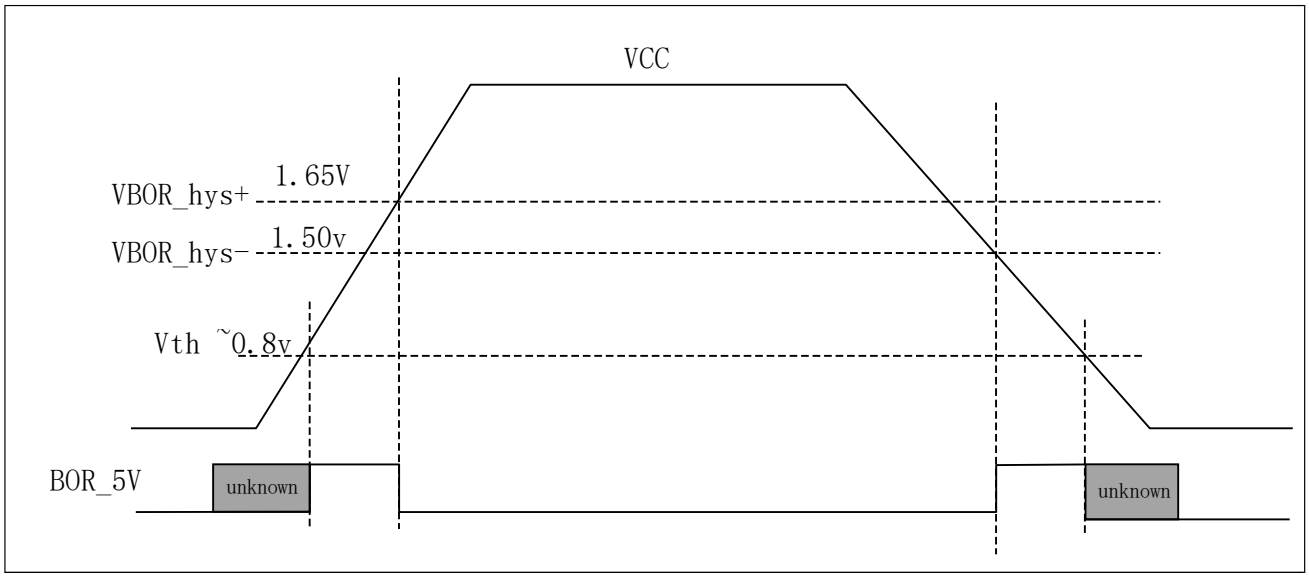


Figure 7-1POR/BrownOut Schematic

1. Design warranty, not tested in production.

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
Vpor	POR Release Voltage (Power-Up Process) BOR detection voltage (power-down process)		1.45	1.50	1.65	V

Table 7-6POR/BrownOut

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
Vex	External input voltage range		0		VCC	V
Vlevel	Detection Threshold	LVD_CR.VTDS=0000		1.8		V
		LVD_CR.VTDS =0001		1.9		
		LVD_CR.VTDS =0010		2.0		
		LVD_CR.VTDS =0011		2.1		
		LVD_CR.VTDS =0100		2.2		
		LVD_CR.VTDS=0101		2.3		
		LVD_CR.VTDS=0110		2.4		
		LVD_CR.VTDS=0111		2.5		
		LVD_CR.VTDS=1000		2.6		
		LVD_CR.VTDS=1001		2.7		
		LVD_CR.VTDS=1010		2.8		
		LVD_CR.VTDS=1011		2.9		
		LVD_CR.VTDS=1100		3.0		
		LVD_CR.VTDS=1101		3.1		
		LVD_CR.VTDS=1110		3.2		
		LVD_CR.VTDS=1111		3.3		
Icomp	Power consumption			0.12		μA
Tresponse	Response time			80		μs
Tsetup	Establishment time			400		μs
Vhyste	Hysteresis voltage			40		mV
Tfilter	Filtering time	LVD_debounce = 000		7		μs
		LVD_debounce = 001		14		
		LVD_debounce = 010		28		
		LVD_debounce = 011		112		
		LVD_debounce = 100		450		
		LVD_debounce = 101		1800		
		LVD_debounce = 110		7200		
		LVD_debounce = 111		28800		

Table 7-6LVDModule Characteristics

7.3.4. Built-in reference voltage

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
VREF25	Internal 2.5V Reference Voltage	Room temperature 25°C 3.3V	2.475	2.5	2.525	V
VREF25	Internal 2.5V Reference Voltage	-40~85°C2.8~5.5V	2.463	2.5	2.525	V[1]
VREF15	Internal 1.5V Reference Voltage	Room temperature 25°C 3.3V	1.485	1.5	1.515	V
VREF15	Internal 1.5V Reference Voltage	-40~85°C1.8~5.5V	1.477	1.5	1.519	V[1]
Tcoeff	Internal 2.5V 1.5V temperature coefficient	-40~85°C			120	ppm/°C

1. The data is based on assessment results and is not tested in production.

7.3.5. Operating current characteristics

Current consumption is a composite indicator of multiple parameters and factors, including operating voltage, ambient temperature, load on I/O pins, software configuration of the product, operating frequency, flip rate of I/O pins, location of the program in memory, and code executed.

The microcontroller is in the following conditions.

- All I/O pins are in input mode and are connected to a static level – VCC or VSS (no load).
- All peripherals are off, unless otherwise noted.
- The FLASH memory access time is adjusted to the f_{HCLK} frequency (0~24MHz for one wait cycle, 24~48MHz for one 0wait cycle). 1

  The waiting period for the first time is three months.)
- When peripheral is turned on: $f_{PCLK} = f_{HCLK}$.

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
IDD (Run in RAM)	All peripherals clock OFF, Run While(1) in RAM.	VCAP=1.55 V VCC=3.3V	RCH clock source	4M	220		µA
				8M	400		
				16M	740		
				24M	1080		
				32M	1400		
IDD	All peripherals		RCH	4M	670		
				8M	1300		
				16M	2380		

(Run CoreMark)	clock OFF, Run CoreMark in Flash.	V_{CAP}=1.55V VCC=3.3V	clock source	24M	3410		µA
				32M (Flash Wait= 1)	3530		
IDD (Run mode)	All peripherals clock ON,	V_{CAP} = 1.55V V_{CC} = 1.8-5.5V	RCH clock source	4M	700	880	µA
				8M	1350	1600	
				16M	2500	3000	

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
	Run while(1) in Flash			24M	3600	4300	
	All peripheral clock OFF, Run while(1) in Flash	V_{CAP} = 1.55V V_{CC} = 1.8-5.5V	RCH clock source	4M	550	750	
				8M	1050	1300	
				16M	1900	2400	
				24M	2700	3300	
				32M (Flash Wait= 1)	2850	3000	
IDD (Sleep mode)	All peripheral clock ON	V_{CAP} = 1.55V V_{CC} = 1.8-5.5V	RCH clock source	4M	260	280	µA
				8M	500	520	
				16M	950	970	
				24M	1400	1420	
	All peripheral clock OFF	V_{CAP} = 1.55V V_{CC} = 1.8-5.5V	RCH clock source	4M	110	125	
				8M	190	210	
				16M	330	360	
				24M	470	500	
				32M	580	610	
IDD (LP Run)	All peripherals clock ON, Run while(1) in Flash	V_{CAP} = 1.55V V_{CC} = 1.8-5.5V	XTL 32.768kHz (Driver = 1)	T_A = -40 to 25°C	7	9	µA
				T_A = 50°C	7.3	9.2	
				T_A = 85°C	8.9	11.3	
	All peripherals clock OFF, Run while(1) in Flash	V_{CAP} = 1.55V V_{CC} = 1.8-5.5V	XTL 32.768kHz (Driver = 1)	T_A = -40 to 25°C	6	8	
				T_A = 50°C	6.1	8.2	
				T_A = 85°C	7.7	10.1	
IDD (LP Sleep)	All peripherals clock ON	V_{CAP} = 1.55V V_{CC} = 1.8-5.5V	XTL 32.768kHz (Driver = 1)	T_A = -40 to 25°C	3.3	3.5	µA
				T_A = 50°C	3.6	3.8	
				T_A = 85°C	5.4	5.8	
	All peripherals clock OFF except LPTimer and RTC	V_{CAP} = 1.55V V_{CC} = 1.8-5.5V	XTL 32.768kHz (Driver = 1)	T_A = -40 to 25°C	2.2	2.4	
				T_A = 50°C	2.5	2.6	
				T_A = 85°C	4.2	4.6	
IDD (DeepSleep)	All peripherals clock OFF except RTC.	V_{CAP} = 1.55V V_{CC} = 1.8-5.5V		T_A = -40 to 25°C	1.5	1.65	µA
				T_A = 50°C	1.85	2.2	
				T_A = 85°C	3.5	4.2	

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
	WDT, the LPTimer						
	All peripherals clock OFF except WDT	V_{CAP} = 1.55V V_{CC} = 1.8-5.5V		T_A = -40 to 25°C	1.2	1.3	
				T_A = 50°C	1.5	1.8	
				T_A = 85°C	3.1	3.7	
	All peripherals clock OFF except LPTimer	V_{CAP} = 1.55V V_{CC} = 1.8-5.5V		T_A = -40 to 25°C	0.9	1	
				T_A = 50°C	1.1	1.3	
				T_A = 85°C	2.6	3	
	All peripherals clock OFF except RTC	V_{CAP} = 1.55V V_{CC} = 1.8-5.5V		T_A = -40 to 25°C	1.0	1.1	
				T_A = 50°C	1.2	1.5	
				T_A = 85°C	2.6	3.4	
	All peripherals clock OFF	V_{CAP} = 1.55V V_{CC} = 1.8-5.5V		T_A = -40 to 25°C	0.42	0.6	
				T_A = 50°C	0.75	0.95	
				T_A = 85°C	2.2	2.7	

1. If no other conditions are specified, the value of this Typ is measured at 25°C & V_{CC} = 3.3V.
2. If no other conditions are specified, the value of this Max is the maximum value in the range of V_{CC} = 1.8-5.5 & Temperature = N40 -85 °C.
3. The data is based on assessment results and is not tested in production.

Table 7-9 Operating Current Characteristics

7.3.6. Wake-up time from low-power mode

The wake-up time is measured during the wake-up phase of the RCH oscillator. The clock source used for wake-up depends on the current operating mode.

- Sleep mode: The clock source is the RCH oscillator
- Deep sleep mode: The clock source is the RCH oscillator used when entering deep sleep

Symbol	Papameter	Conditions	Min	Typ	Max	Unit
Twu	Sleep mode wake-up time			1.8		μs
	Deep hibernation wake-up time	F_{MCLK} = 4MHz		9.0		μs
		F_{MCLK} = 8MHz		6.0		μs
		F_{MCLK} = 16MHz		5.0		μs
		F_{MCLK} = 24MHz		4.0		μs

1. The wake-up time is measured from the start of the wake-up event until the first instruction is read by the user program.

7.3.7. External clock source characteristics

External input high-speed clock

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
Fxth_ext	User external clock frequency(1)		0	8	32	MHz
VXTHH	Input pin high level voltage		0.7VCC		VCC	V
VXTHL	Input pin low level voltage		VSS		0.3VCC	V
Tr(XTH)	Up time(1)				20	ns
Tf(XTH)	Time of descent(1)				20	ns
Tw(XTH)	Input high or low time(1)		16			ns
Cin(XTH)	Input resistance(1)			5		pF
Duty	Duty Cycle		40		60	%
IL	Input leakage current				±1	μA

1. Guaranteed by design, not tested in production.

External input low-speed clock

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
Fxtl_ext	User external clock frequency(1)		0	32.768	1000	kHz
VXTLH	Input pin high level voltage		0.7VCC		VCC	V
VXTLL	Input pin low level voltage		VSS		0.3VCC	V
Tr(XTL)	Up time(1)				50	ns
Tf(XTL)	Time of descent(1)				50	ns
Tw(XTL)	Input high or low time(1)		450			ns
Cin(XTL)	Input resistance(1)			5		pF
Duty	Duty Cycle		30		70	%
IL	Input leakage current				±1	μA

1. Guaranteed by design, not tested in production.

High-speed external clock XTH

A high speed external clock (XTH) can be generated using an oscillator consisting of a 4 to 32 MHz crystal/ceramic resonator. The information given in this section is based on a comprehensive characterization using the typical external components listed in the table below. In applications, the resonator and load capacitor must be placed as close to the oscillator pins as possible to minimize output distortion and stabilization time at start-up. For detailed parameters of crystal resonators (frequency, package, accuracy, etc.), please consult the appropriate manufacturer.

External XTH Crystal(1)(2)

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
FCLK	Oscillation frequency		4		32	MHz
ESRCLK	Supported crystal ESR range	32M		30	60	Ohm
		4M		400	1500	Ohm
CLX(3)	Load capacitance	Configured to the crystal manufacturer's requirements.				
Duty	Duty Cycle		40	50	60	%
Idd(4)	Current	32M Xtal, CL=12Pf, ESR=30ohm		600		μA
gm	cross-guide	Vibration	700			μA/V
Tstart(5)	Start-up time	32MHz @ XTH_CR.Driver=1111		400		μs
		4MHz @ XTH_CR.Driver=0011		2		ms

1. The resonator characteristics are given by the crystal/ceramic resonator manufacturer.
2. Derived from a comprehensive assessment and not tested in production.
3. CLX refers to the load capacitance of the two pins of the XTAL, and the user **must** select the capacitance of this capacitor according to the crystal manufacturer's requirements.

   If the capacitance of the load ***capacitor is given by the crystal*** manufacturer, the matching capacitor should be twice the capacitance o f the load capacitor given by the crystal manufacturer.

   If the crystal manufacturer gives the capacitance of the ***matching capacitor,*** then the capacitance of the matching capacitor given by the crystal manufacturer can be used directly. Example: If the crystal manufacturer gives a ***load capacitance*** of 8pF for the crystal, the capacitance of the matching capacitor should be 16pF.

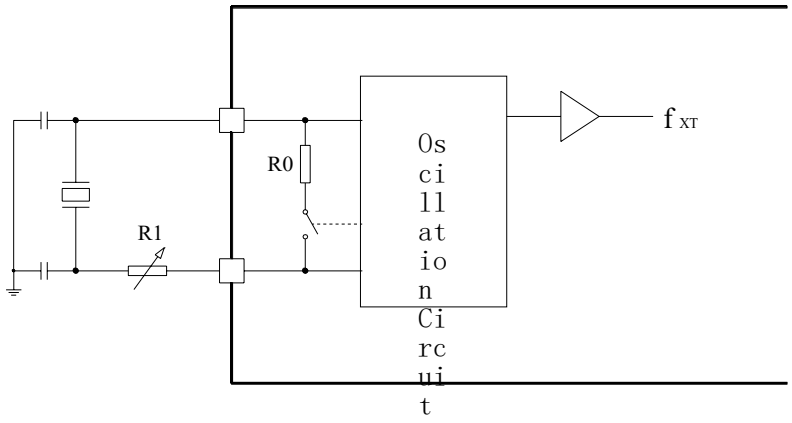
For the distribution capacitance between the pins, it is recommended to choose a matching capacitor with a capacitance of 15pF or 12pF.

The capacitance of the matching capacitor should be 12pF when the crystal manufacturer gives a *matching capacitance* of 12pF for the crystal, considering the PCB and MCU

For the distribution capacitance between the pins, it is recommended to choose a matching capacitor with a capacity of 10pF or 8pF.

4. Current follows the frequency change, test condition: XTH_CR.Driver=1110

5. T_{start} is the start-up time, measured from the time the software enables XTH until a stable 32MHz/4MHz oscillation is obtained. This value is measured on a standard crystal resonator and can vary greatly depending on the crystal manufacturer and model.



Caution.

- The matching capacitance of the crystal **must be** configured according to the requirements of the crystal manufacturer's technical manual.

  If the capacitance of the load ***capacitor is given by the crystal*** manufacturer, the matching capacitor should be twice the capacitance o f the load capacitor given by the crystal manufacturer.

  If the crystal manufacturer gives the capac***itance value of the*** matching capacitor, it is sufficient to use the capacitance value of the matching capacitor given by the crystal manufacturer.

- The feedback resistor **R0** has been integrated into the chip.

- See the relevant application notes for the debugging method of the damping resistor **R1** resistance value.

Low-speed external clock XTL

A low-speed external clock (XTL) can be generated using an oscillator consisting of a 32.768 kHz crystal/ceramic resonator. The information given in this section is based on typical external components and is obtained by a comprehensive characterization. In the application, the resonator and load capacitor must be placed as close as possible to the oscillator pins to minimize output distortion and stabilization time at start-up. For detailed parameters of crystal resonators (frequency, package, accuracy, etc.), please consult the appropriate manufacturer.

External XTL crystal(1)

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
FCLK	Oscillation frequency			32.768		kHz
ESRCLK	Supported crystal ESR range			65	85	kΩ
C_{LX}(2)	Load capacitance	Configured to the crystal manufacturer's requirements.				
DCACLK	Duty Cycle		30	50	70	%
Idd(3)	Current	ESR= 65 kΩ CL=12 Pf		850	1000	nA
gm	cross-guide	Vibration	2.5			μA/V
Tstart	Start-up time	ESR=65 kΩ CL=12 Pf 40% - 60% duty cycle has been reached		500		ms

1. Derived from a comprehensive assessment and not tested in production.
2. C_{LX} refers to the load capacitance of the two pins of the XTAL, and the user **must** select the capacitance of this capacitor according to the crystal manufacturer's requirements.

   If the capacitance of the load ***capacitor is given by the crystal*** manufacturer, the matching capacitor should be twice the capacitance o f the load capacitor given by the crystal manufacturer.

   If the crystal manufacturer gives the capacitance of the ***matching capacitor,*** then the capacitance of the matching capacitor given by the crystal manufacturer can be used directly. Example: If the crystal manufacturer gives a ***load capacitance*** of 8pF for the crystal, the capacitance of the matching capacitor should be 16pF.

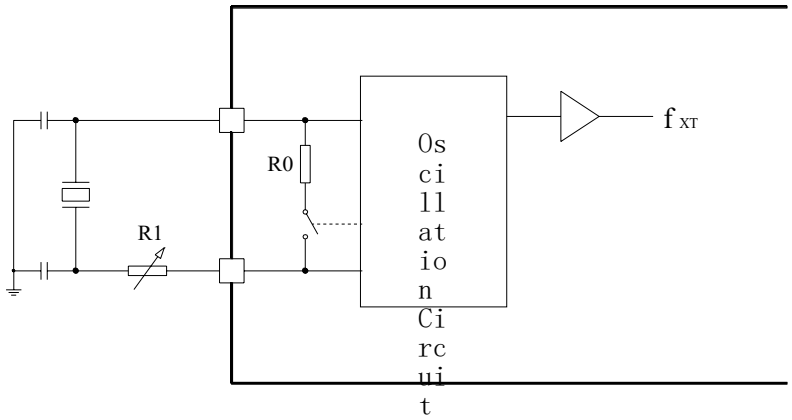
   For the distribution capacitance between the pins, it is recommended to choose a matching capacitor with a capacitance of 15pF or 12pF.

The capacitance of the matching capacitor should be 12pF when the crystal manufacturer gives a *matching capacitance* of 12pF for the crystal, considering the PCB and MCU

For the distribution capacitance between the pins, it is recommended to choose a matching capacitor with a capacity of 10pF or 8pF.

3. Typical value is the power consumption at XTL_CR.Driver=1001. Selecting a high quality oscillator with a small ESR value (e.g. MSIV- TIN32.768kHz), the current consumption can be optimized by reducing the XTL_CR.

4. T_{start} is the start-up time, measured from the time the software enables the XTL until a stable 32768oscillation is obtained. This value is measured on a standard crystal resonator and can vary greatly depending on the crystal manufacturer and model.



Caution.

- The matching capacitance of the crystal **must be** configured according to the requirements of the crystal manufacturer's technical manual.

  If the capacitance of the load ***capacitor is given by the crystal*** manufacturer, the matching capacitor should be twice the capacitance o f the load capacitor given by the crystal manufacturer.

  If the crystal manufacturer gives the capac***itance value of the*** matching capacitor, it is sufficient to use the capacitance value of the matching capacitor given by the crystal manufacturer.

- The feedback resistor **R0** has been integrated into the chip.

- See the relevant application notes for the debugging method of the damping resistor **R1** resistance value.

7.3.8. Internal clock source characteristics

Internal RCH oscillator

Symbol	Papameter	Conditions	Min	Typ	Max	Unit
Dev	RCH oscillator accuracy	User trimming step for given VCC and TA conditions		0.25		%
		VCC = ~1.8 5.5V T_{AMB} = -40 ~ 85°C	-3.5		+3.5	%
		VCC = ~1.8 5.5V T_{AMB} = -20 ~ 50°C	-2.0		+2.0	%
FCLK	Oscillation frequency		4.0	4.0 8.0 16.0 22.12 24.0	24.0	MHz
ICLK	Power consumption	F_{MCLK} = 4MHz		80		μA
		F_{MCLK} = 8MHz		100		μA
		F_{MCLK} = 16MHz		120		μA
		F_{MCLK} = 24MHz		140		μA
DCCLK	Duty cycle(1)		45	50	55	%

1. Derived from a comprehensive assessment and not tested in production.

Internal RCL oscillator

Symbol	Papameter	Conditions	Min	Typ	Max	Unit
Dev	RCL oscillator accuracy	User trimming step for given VCC and TA conditions		0.5		%
		VCC = ~1.8 5.5V T_{AMB} = -40 ~ 85°C	-5		+5	%
		VCC = ~1.8 5.5V T_{AMB} = -20 ~ 50°C	-3		+3	%
FCLK	Oscillation frequency			38.4 32.768		kHz
TCLK	Start-up time			150		μs
DCCLK	Duty cycle(1)		25	50	75	%
ICLK	Power consumption			0.25		μA

1. Derived from a comprehensive assessment and not tested in production.

7.3.9. Memory Features

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
ECFLASH	Number of erasures	Regulator voltage=1.5V, T_{AMB} = 25°C	20			kcycles
RETFLASH	Data retention period	T_{AMB} = 85°C. after kcycles20	20			Years
Tw_prog	Programming time		6		7.5	μs
Tp_erase	Page erase time		4		5	ms
Tm_erase	Whole chip erase time		30		40	ms

7.3.10. EFT Features

A chip reset restores the system to normal operation.

Symbols	Level / Type
EFT to IO(IEC61000-4-4)	Class:4(B)
EFT to Power (IEC61000-4-4)	Class:4(B)

Software suggestions

The software process must include controls to deal with program runaways, such as

- Broken program counter
- Unexpected reset
- Critical data is corrupted (control registers, etc.)

During EFT testing, interference beyond the application requirements can be applied directly to the chip power supply or IO, and where unexpected actions are detected, the software section is enhanced to prevent unrecoverable errors from occurring.

7.3.11. ESD Characteristics

Using specific measurement methods, the chip is tested for strength to determine its performance in terms of electrical sensitivity.

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
VESDHBM	ESD @ Human Body Mode			4		KV
VESDCDM	ESD @ Charge Device Mode			1		KV
VESDMM	ESD @ machine Mode			200		V
Ilatchup	Latch up current			200		mA

7.3.12. Port Characteristics

Output Characteristics - Port

Symbol	Parameter	Conditions	Min	Max	Uuit
VOH	High level output voltage Source Current	Sourcing Ma4, VCC = V3.3 (see Note 1)	VCC-0.25		V
		Sourcing Ma6, VCC = V3.3 (see Note 2)	VCC-0.6		V
VOL	Low level output voltage Sink Current	Sinking Ma4, VCC = V3.3 (see Note 1)		VSS+0.25	V
		Sinking Ma6, VCC = V3.3 (see Note 2)		VSS+0.6	V
VOHD	High level output voltage Double source Current	Sourcing Ma8, VCC = V3.3 (see Note 1)	VCC-0.25		V
		Sourcing Ma12, VCC = 3.3V (see Note 2)	VCC-0.6		V
VOLD	Low level output voltage Double Sink Current	Sinking Ma8, VCC = V3.3 (see Note 1)		VSS+0.25	V
		Sinking Ma12, VCC = V3.3 (see Note 2)		VSS+0.6	V

Table 7-10 Port Output Characteristics

NOTES:

1. The maximum total current, IOH(max) and IOL(max), for all outputs combined, should not exceed Ma40 to satisfy the maximum specified voltage drop.
2. The maximum total current, IOH(max) and IOL(max), for all outputs combined, should not exceed Ma100 to satisfy the maximum specified voltage drop.

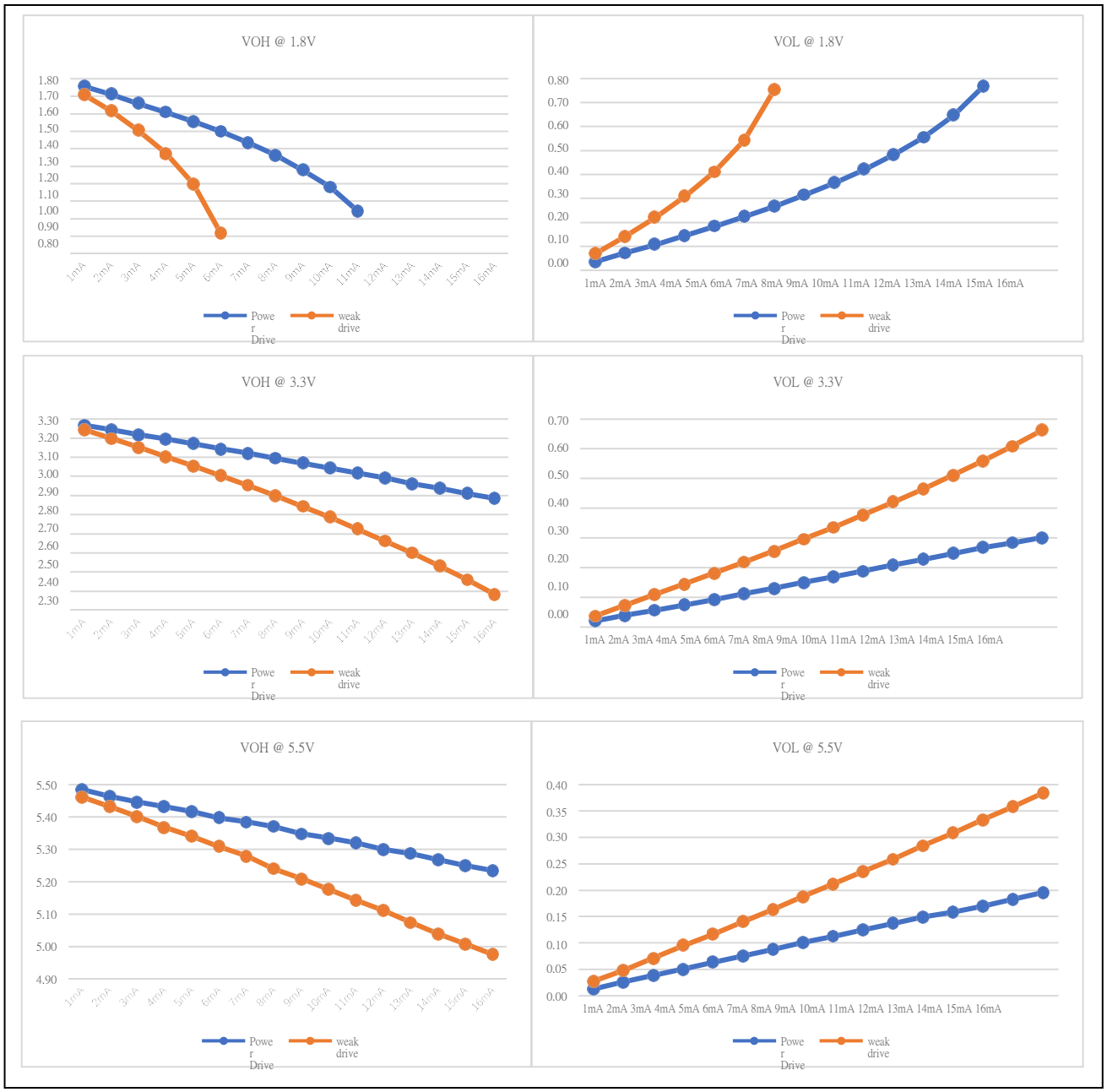


Figure 7-2 Output port VOH/VOL actual measurement curve

Input Characteristics - Ports P0,P1,P2,P3

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
VIH	Positive-going input threshold voltage	VCC=1.8V	0.7VCC			V
		VCC=3.3V	0.7VCC			V
		VCC=5.5V	0.7VCC			V
VIL	Negative-going input threshold voltage	VCC=1.8V			0.3VCC	V
		VCC=3.3V			0.3VCC	V
		VCC=5.5V			0.3VCC	V

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
Vhys(1)	Input voltage hysteresis (V_{IH} - V_{IL})	VCC=1.8V		0.3		V
		VCC=3.3V		0.4		V
		VCC=5.5V		0.6		V
Rpullhigh	Pullup resistor	Pullup enabled VCC=3.3V		80		kΩ
Rpulllow	Pulldown resistor	Pulldown enabled VCC=3.3V		40		kΩ
Cinput	Input capacitance			5		pF

1. Derived from a comprehensive assessment and not tested in production.

Port External Input Sampling Requirements - Timer Gate/Timer Clock

Symbol	Papameter	Conditions	VCC	Min	Max	Uuit
t(int)	External interrupt timing	External trigger signal for the interrupt flag (see Note 1)	1.8V	30		ns
			3.3V	30		ns
			5.5V	30		ns
t(cap)	Timer capture timing	Timer4/5/6 capture pulse width Fsystem = 4MHz	1.8V	0.5		μs
			3.3V	0.5		μs
			5.5V	0.5		μs
t(clk)	Timer clock frequency applied to pin	Timer0/1/2/4/5/6 external clock input Fsystem = 4MHz	1.8V		PCLK/2	MHz
			3.3V		PCLK/2	MHz
			5.5V		PCLK/2	MHz
t(pca)	PCA clock frequency applied to pin	PCA external clock input Fsystem = 4MHz	1.8V		PCLK/8	MHz
			3.3V		PCLK/8	MHz
			5.5V		PCLK/8	MHz

NOTE:

1. The external signal sets the interrupt flag every time the minimum $t_{(int)}$ parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$.

Port leakage characteristics - P0,P1,P2,P3

Symbol	Papameter	Conditions	VCC	Max	Unit
Ilkg(Px.y)	Leakage current	$V_{(Px.y)}$ (see Note 1,2)	1.8 V/3.6 V	±50	nA

NOTES:

1. The leakage current is measured with VSS or VCC applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as input.

7.3.13. RESETB pin characteristics

The RESETB pin input driver uses a CMOS process, which connects a pull-up resistor that cannot be disconnected.

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
VIL(RESETB) (1)	Input Low Level Voltage		-0.3		0.3VCC	V
VIH(RESETB)	Input high level voltage		0.7VCC		VCC+0.3	V
Vhys(RESETB)	Schmitt Trigger Voltage Hysteresis			200		mV
RPU	Weak pull-up equivalent resistance	VIN = VSS		80		kΩ
VF(RESETB) (1)	Input filter pulse				100	ns
VNF(RESETB) (1)	Input non-filtered pulses		300			ns

1. Guaranteed by design, not tested in production.

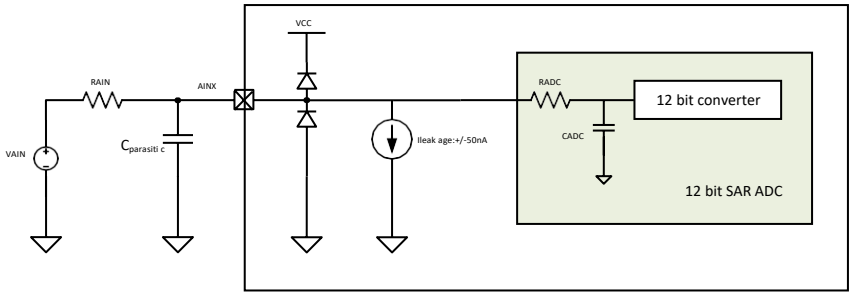
7.3.14. ADC Features

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
VADCIN	Input voltage range	Single ended	0		VADCREFIN	V
VADCREFIN	Input range of external reference voltage	Single ended	0		VCC	V
DEVVCC/3	VCC/3 accuracy			3		%
IADC1	Active current including reference generator and buffer	200Ksps		2		mA
IADC2	Active current without reference generator and buffer	1Msps		0.5		mA
CADCIN	ADC input capacitance			16	19.2	pF
RADC(1)	ADC sampling switch impedance			1.5		kΩ
RAI (1) N	ADC external input resistor(2)				100	kΩ
FADCCLK	ADC clock Frequency				24M	Hz
TADCSTART	Startup time of reference generator and ADC core			30		μs
TADCCONV	Conversion time		20	24	28	cycles

ENOB	Effective Bits	1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.8V REF=EXREF		10.3		Bit

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
		1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.8V REF=VCC		10.3		Bit
		200Ksps@VCC>=1.8V REF=internal 1.5V		9.4		Bit
		200Ksps@VCC>=2.8V REF=internal 2.5V		9.4		Bit
SNR	Signal to Noise Ratio	1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.8V REF=EXREF		68.2		dB
		1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.8V REF=VCC		68.2		dB
		200Ksps@VCC>=1.8V REF=internal 1.5V		60		dB
		200Ksps@VCC>=2.8V REF=internal 2.5V		60		dB
DNL(1)	Differential non-linearity	200KSps. VREF=EXREF/VCC	-1		1	LSB
INL(1)	Integral non-linearity	200KSps. VREF=EXREF/VCC	-3		3	LSB
Eo	Offset error			0		LSB
Eg	Gain error			0		LSB

1. Guaranteed by design, not tested in production.
2. Typical applications of ADCs are shown in the following diagram.



For the condition of 0.5LSB sampling error accuracy requirement, the external input impedance is calculated by the following equation

$$R_{AIN} = \frac{M}{F_{ADC} * C_{ADC} * (N+1) * \ln(2)} - R_{ADC}$$

Where f_{ADC} is the ADC clock frequency, register ADC_CR0<3:2> can set its relationship with PCLK as follows: The following table shows the relationship between the ADC clock frequency f_{ADC} and the PCLK division ratio.

ADC_CR0[3:2]	N
00	1
01	2
10	4
11	8

M is the number of sampling periods, set by register ADC_CR0<13:12>. The following table shows the relationship between ADC_CR0<13:12> the sampling time t_{sa} and the ADC clock frequency f_{ADC}.

ADC_CR0<13:12>	M
00	4
01	6
10	8
11	12

The following table shows the relationship between the ADC clock frequency f_{ADC} and the external resistor R_{AIN} (under the condition that M = 12,sampling error 0.5LSB)

R_{AIN} (kΩ)	f_{ADC} (kHz)
10	5600
30	2100
50	1300
80	820
100	660
120	550
150	450

For the above typical applications, it should be noted that

- Minimize the parasitic capacitance of the ADC input port $C_{AINXCPARACITIC}$; I_{TIC}

- In addition to considering the R_{AIN} value, it is also necessary to include consideration if the internal resistance of the signal source V_{AIN} is large.

7.3.15. VC Characteristics

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
Vin	Input voltage range		0		5.5	V
Vincom	Input common mode range		0		VCC-0.2	V
Voffset	Input offset	Room temperature 25°C3.3V	-10		+10	mV
Icomp	Comparator's current	VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11		0.3 1.2 10 20		μA
Tresponse	Comparator's response time when one input crosses another	VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11		20 5 1 0.2		μs
Tsetup	Comparator's setup time when ENABLE. Input signals unchanged.	VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11		20 5 1 0.2		μs
Twarmup	From main bandgap enable to 1.2V BGR reference, Temp sensor voltage, ADC internal 1.5V, 2.5V reference stable			20		μs
Tfilter	Digital filter time	VC_debounce = 000 VC_debounce = 001 VC_debounce = 010 VC_debounce = 011 VC_debounce = 100 VC_debounce = 101 VC_debounce = 110 VC_debounce = 111		7 14 28 112 450 1800 7200 28800		μs

7.3.16. TIM Timer Features

For details on the characteristics of the input-output multiplexing function pins (output compare, input capture, external clock, PWM output), see the following table.

Symbols	Parameters	Conditions	Minimum value	Maximum value	Unit
tres	Timer resolution time		1		tTIMCLK
		fTIMCLK=32MHz	31.3		ns
fext	External clock frequency		0	fTIMCLK/2	MHz
		fTIMCLK=32MHz	0	16	MHz
ResTim	Timer resolution			16	position
Tcounter	When the internal clock is selected, when the 16bit counter Clock cycle		1	65536	tTIMCLK
		fTIMCLK=32MHz	0.0313	2051	μs
TMAX_COUNT	Maximum possible count			67108864	tTIMCLK
		fTIMCLK=32MHz		2.1	s

1. Guaranteed by design, not tested in production.

Table 7-7 Advanced Timer (ADVTIM) Features

Symbols	Parameters	Conditions	Minimum value	Maximum value	Unit
tres	Timer resolution time		1		tTIMCLK
		fTIMCLK=32MHz	31.3		ns
fext	External clock frequency		0	fTIMCLK/2	MHz
		fTIMCLK=32MHz	0	16	MHz
ResTim	Timer resolution	Heavy load count		16	position
		Free counting		32	position
Tcounter	When the internal clock is selected, when the 16bit counter Clock cycle		1	65536	tTIMCLK
		fTIMCLK=32MHz	0.0313	2051	μs
TMAX_COUNT	Maximum possible count (reload mode)			16777216	tTIMCLK
		fTIMCLK=32MHz		524.3	ms

1. Guaranteed by design, not tested in production.

Table 7-8 Basic Timer Characteristics

Symbols	Parameters	Conditions	Minimum value	Maximum value	Unit
tres	Timer resolution time		1		tTIMCLK
		fTIMCLK=32MHz	31.3		ns
fext	External clock frequency		0	fTIMCLK/2	MHz
		fTIMCLK=32MHz	0	16	MHz
ResTim	Timer resolution			16	position
Tcounter	When the internal clock is selected, when the 16bit counter Clock cycle		1	65536	tTIMCLK
		fTIMCLK=32MHz	0.0313	2051	μs
TMAX_COUNT	Maximum possible count			2097152	tTIMCLK
		fTIMCLK=32MHz		65.54	ms

1. Guaranteed by design, not tested in production.

Table 7-9PCACharacteristics

Symbols	Parameters	Conditions	Minimum value	Maximum value	Unit
tres	Timer resolution time		1		tTIMCLK
		fTIMCLK=32MHz	31.3		ns
fext	External clock frequency		0	fTIMCLK/2	MHz
		fTIMCLK=32MHz	0	16	MHz
ResTim	Timer resolution			16	position
Tcounter	When the internal clock is selected, when the 16bit counter Clock cycle		1	65536	tTIMCLK
		fTIMCLK=32MHz	0.0313	2051	μs
TMAX_COUNT	Maximum possible count			65536	tTIMCLK
		fTIMCLK=32MHz		2.05	ms

1. Guaranteed by design, not tested in production.

Table 7-10 Low Power Timer Characteristics

Symbols	Parameters	Conditions	Minimum value	Maximum value	Unit
tres	WDT Overflow Time	fWDTCLK=10kHz	1.6	52000	ms

1. Guaranteed by design, not tested in production.

Table 7-11WDTCharacteristics

7.3.17. Communication Interface

I2C Features

The I2C interface characteristics are listed in the following table.

Symbols	Parameters	Standard mode (100K)		Fast mode (400K)		High-speed mode (1M)		Unit
		Minimum value	Maximum value	Minimum value	Maximum value	Minimum value	Maximum value	
tSCLL	SCL clock low time	4.7		1.25		0.5		μs
tSCLH	SCL Clock High Time	4.0		0.6		0.26		μs
tSU.SDA	SDA build time	250		100		50		ns
tHD.SDA	SDA Hold Time	0		0		0		μs
tHD.STA	Start condition hold time	2.5		0.625		0.25		μs
tSU.STA	Repeated start condition establishment time	2.5		0.6		0.25		μs
tSU.STO	Stop condition establishment time	0.25		0.25		0.25		μs
tBUF	Bus idle (stop condition to start condition)	4.7		1.3		0.5		μs

1. Guaranteed by design, not tested in production.

Table 7-12I2CInterface Characteristics

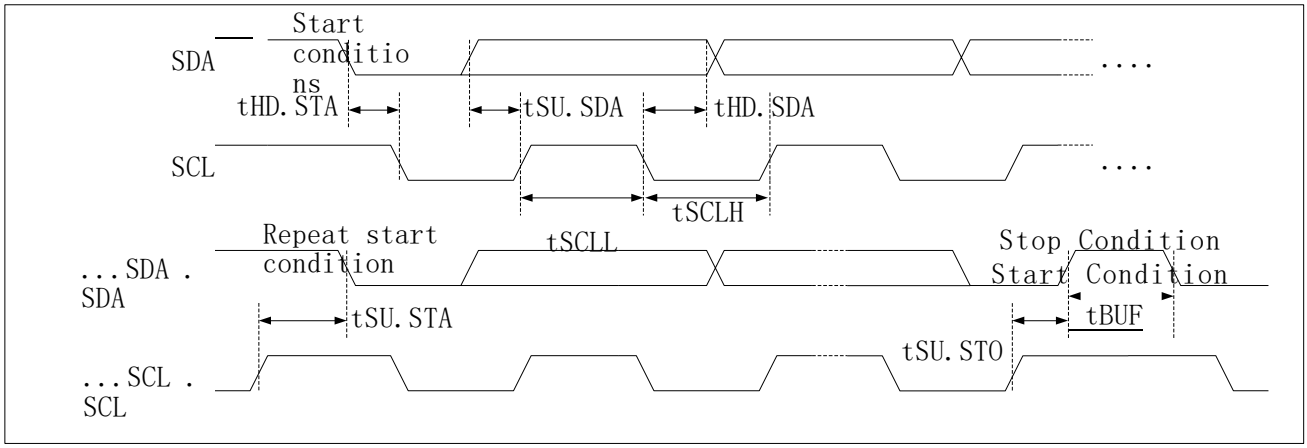


Figure 7-2I2CInterface Timing

SPI Features

Symbols	Parameters	Conditions	Minimum value	Maximum value	Unit
tc(SCK)	Period of serial clock	Host Mode	62.5	-	ns
		Slave Mode f_{PCLK} = 16MHz	250	-	ns
tw(SCKH)	High level time of serial clock	Host Mode	0.5 × $t_{c(SCK)}$	-	ns
		Slave Mode	0.5 × $t_{c(SCK)}$	-	ns
tw(SCKL)	Low level time of serial clock	Host Mode	0.5 × $t_{c(SCK)}$	-	ns
		Slave Mode	0.5 × $t_{c(SCK)}$	-	ns
tsu(SSN)	Slave selection build time	Slave Mode	0.5 × $t_{c(SCK)}$	-	ns
th(SSN)	Hold time for slave selection	Slave Mode	0.5 × $t_{c(SCK)}$	-	ns
tv(MO)	Effective time of host data output	f_{PCLK} = 32MHz	-	3	ns
th(MO)	Hold time of host data output	f_{PCLK} = 32MHz	2	-	ns
tv(SO)	Effective time of slave data output	f_{PCLK} = 16MHz	-	50	ns
th(SO)	Hold time of slave data output	f_{PCLK} = 16MHz	30	-	ns
tsu(MI)	Setup time for host data input		10	-	ns
th(MI)	Host data input hold time		2	-	ns
tsu(SI)	Establishment time of slave data input		10	-	ns
th(SI)	Hold time of slave data input		2	-	ns

1. Guaranteed by design, not tested in production.

Table 7-13SPIInterface Characteristics

The waveforms and timing parameters of the SPI interface signals are as follows.

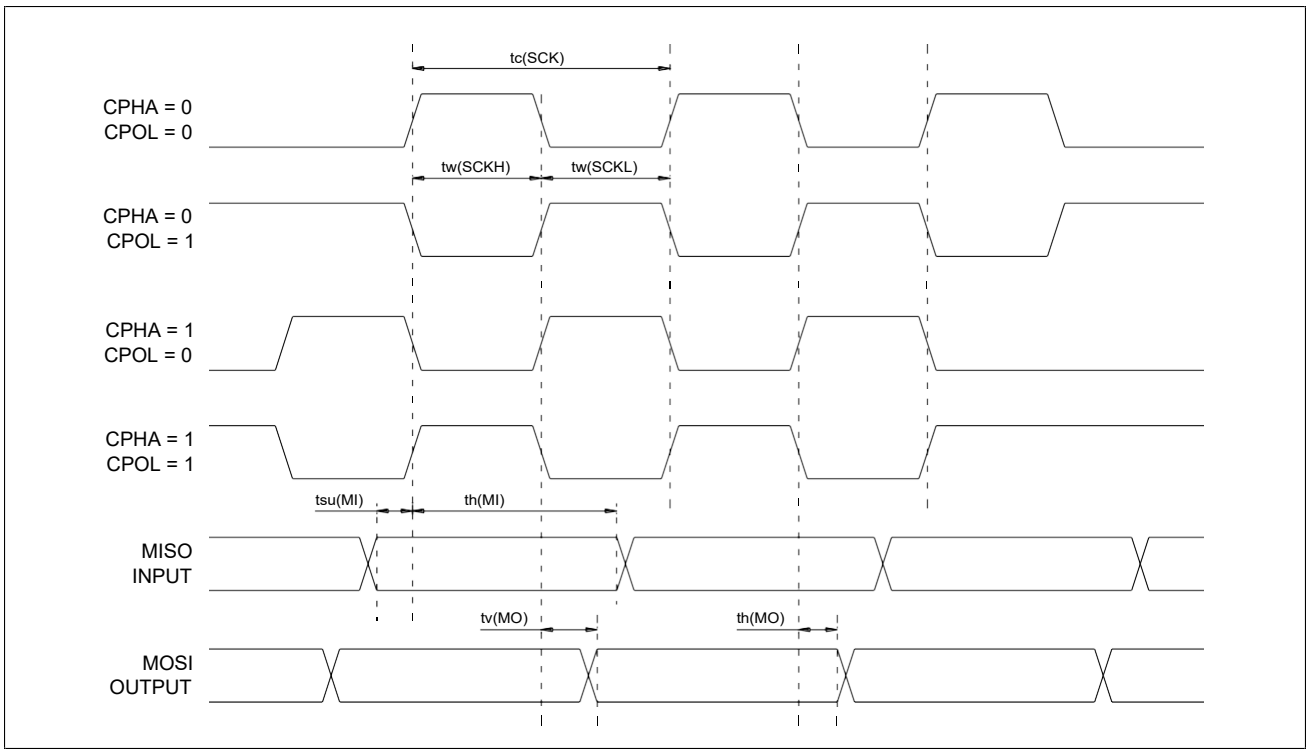


Figure 7-3SPITiming Diagram (Host Mode)

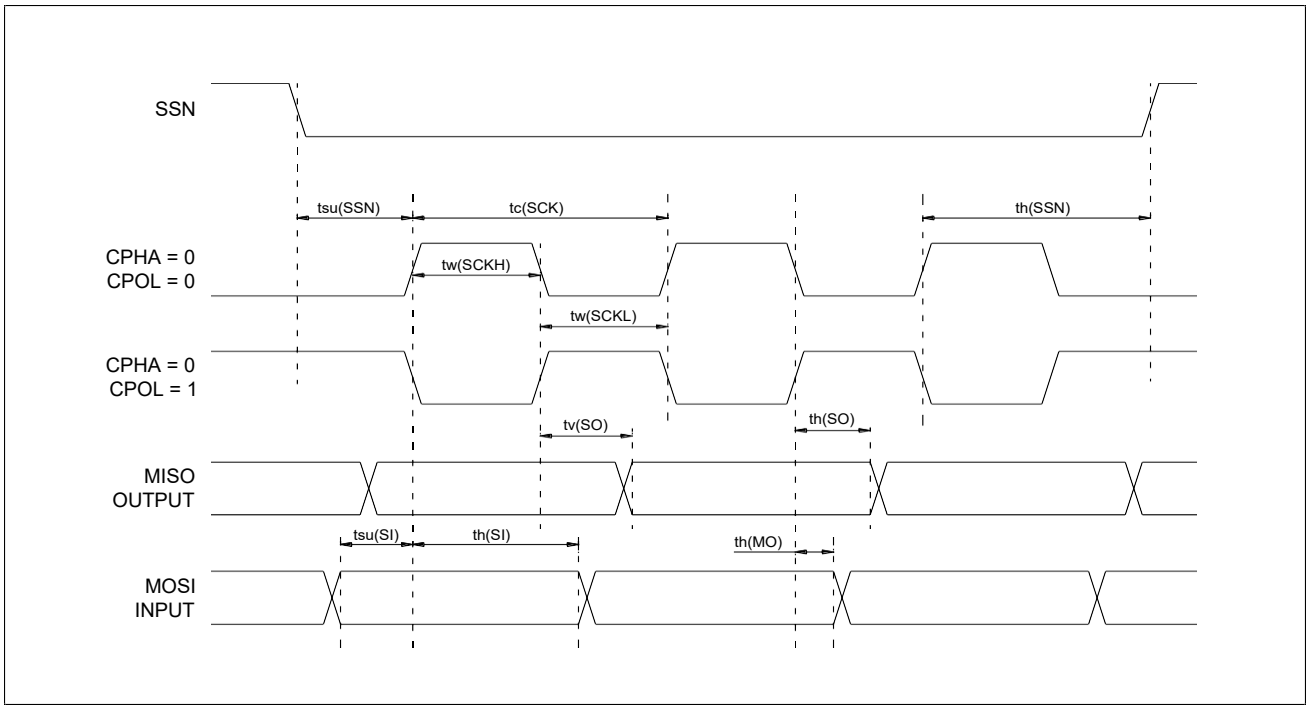


Figure 7-4SPITiming Diagram (Slave Mode cpha=0)

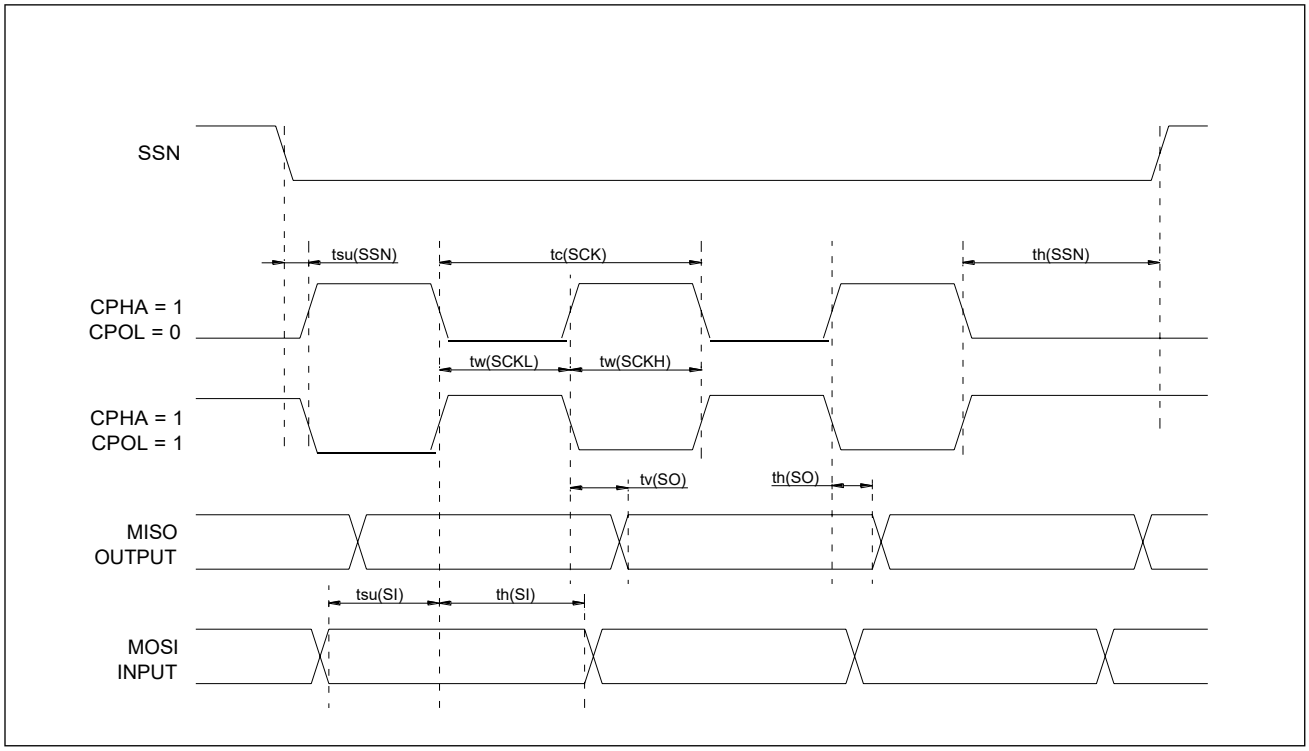
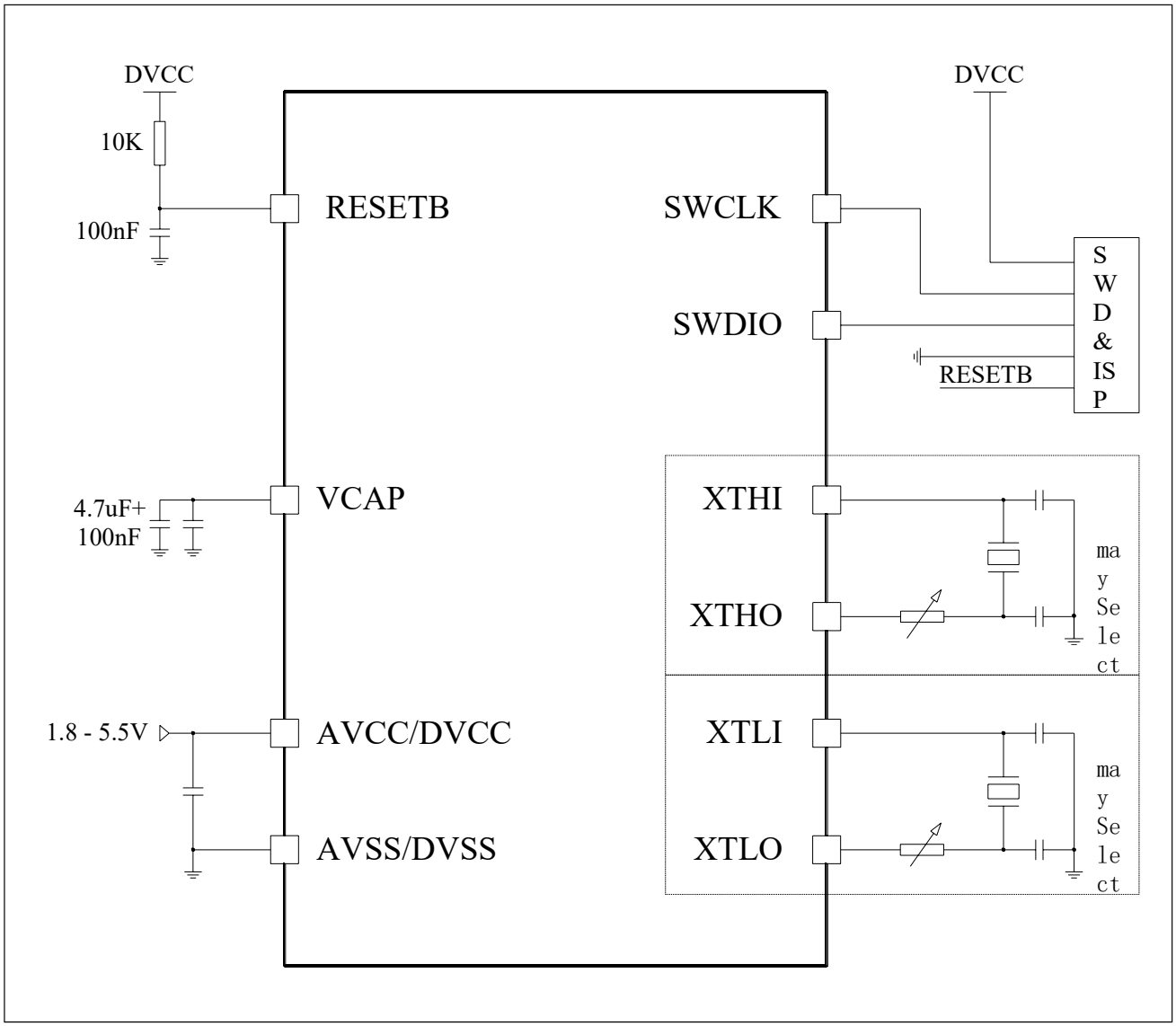


Figure 7-5SPITiming Diagram (Slave Mode cpha=1)

8. Typical Application Circuit Diagram



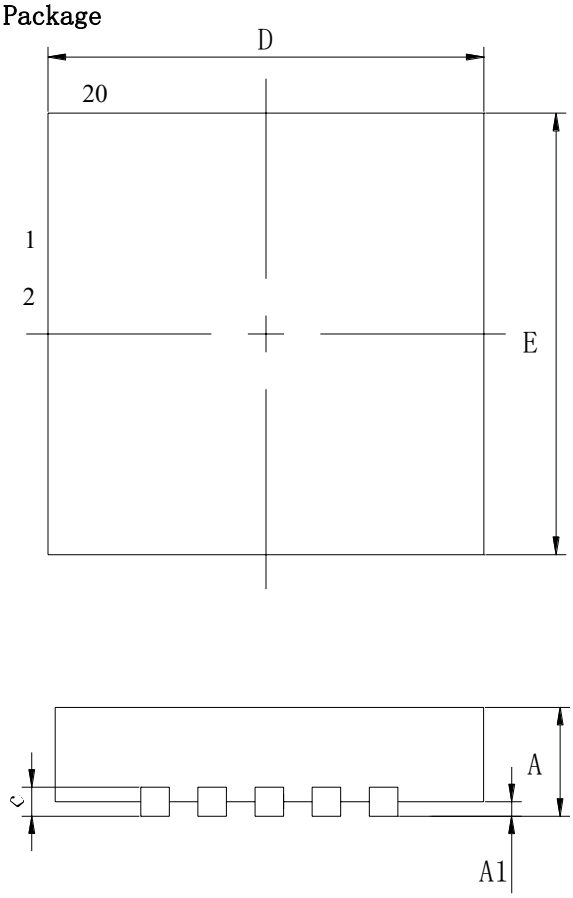
Caution.

- Each group of power supplies requires a decoupling capacitor, which is located as close as possible to the corresponding power supply pin.

9. Package Information

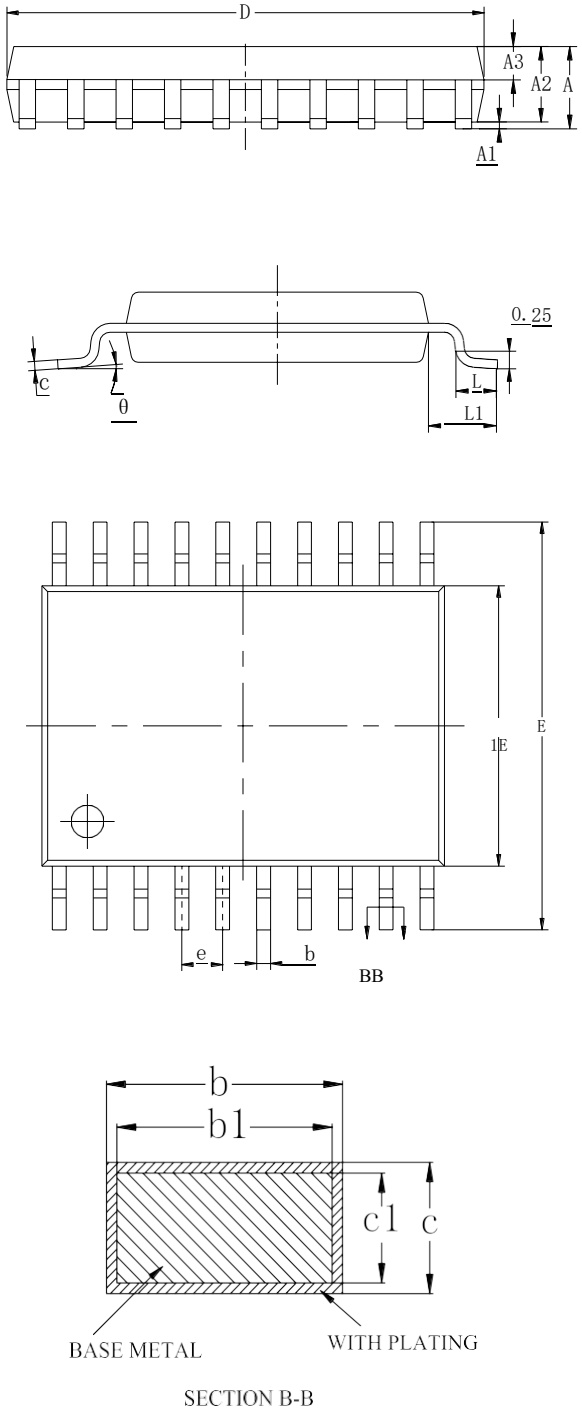
9.1 Package Size

QFN20
Package



Symbol	QFN20 (3x3) millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	--	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e	0.40BSC		
Ne	1.60BSC		
Nd	1.60BSC		
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.35	0.40	0.45
h	0.20	0.25	0.30
L/F Carrier size (Mil)	75 x 75		

TSSOP20 package

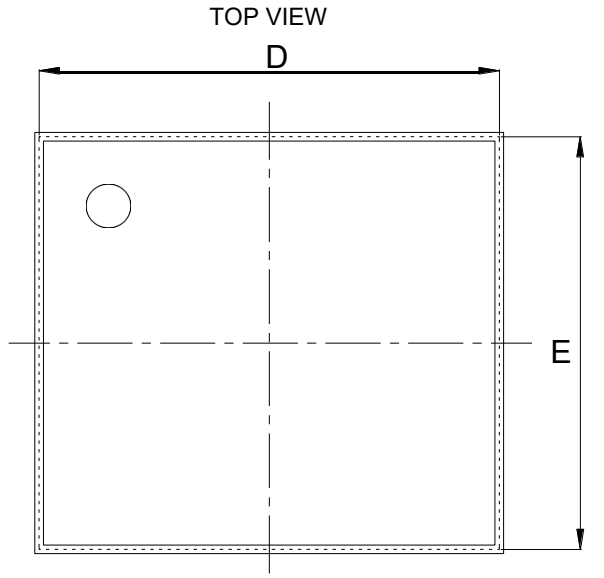


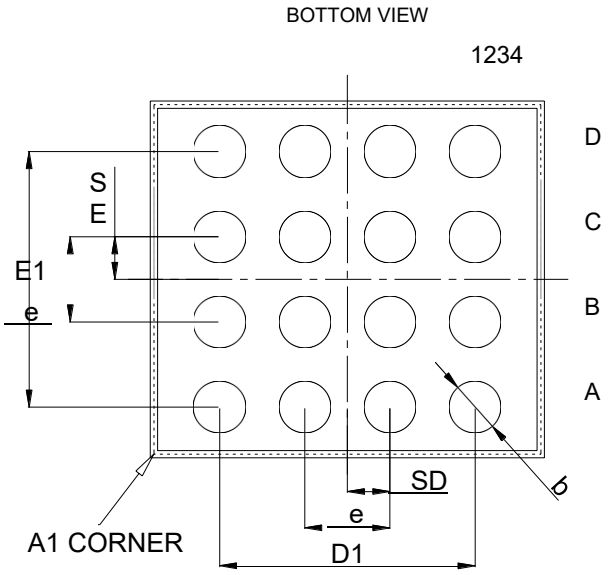
Symbol	TSSOP20 millimeter		
	Min	Nom	Max
A	--	--	1.20
A1	0.05	--	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	--	0.28
b1	0.19	0.22	0.25
c	0.13	--	0.18
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	--	8°

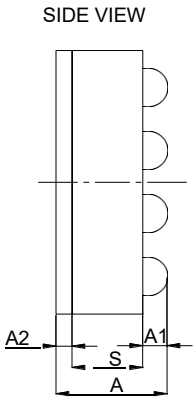
NOTE:

- Dimensions ″D″ and ″E1″ do not include mold flash.

CSP16 Package

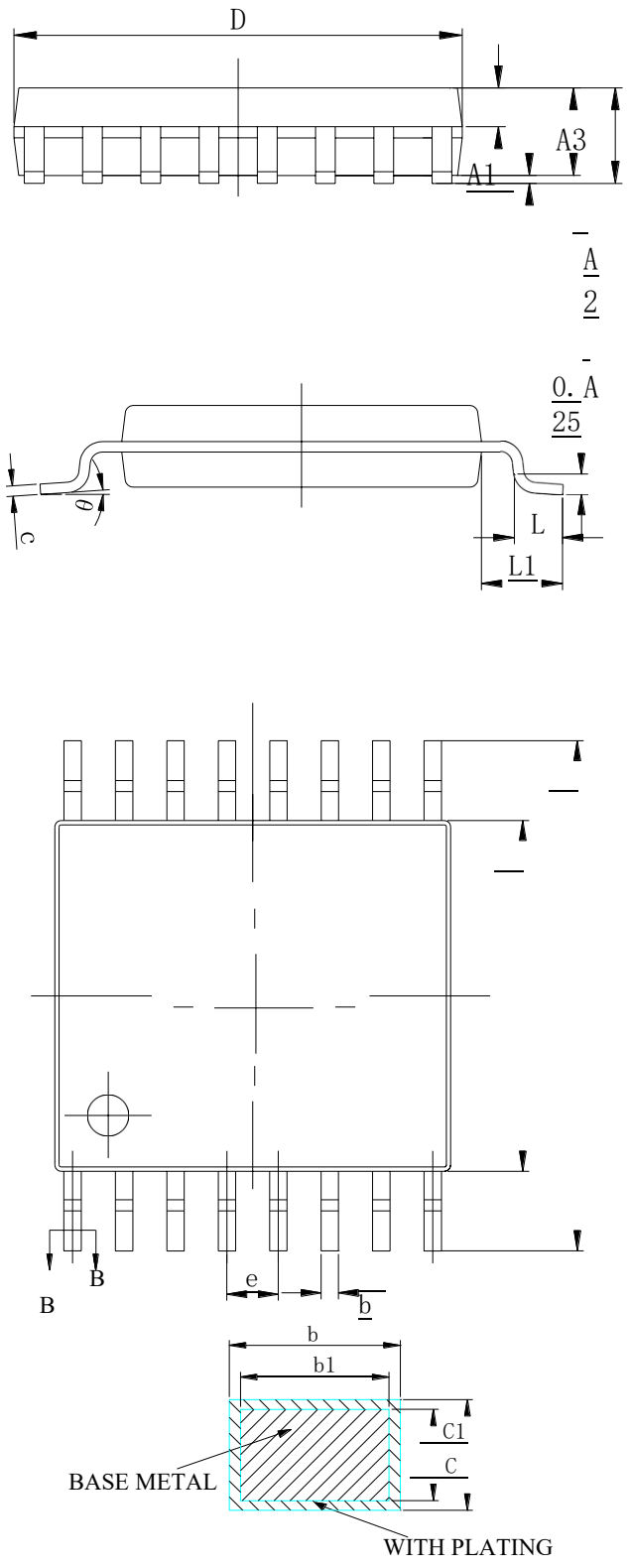






Symbol	CSP16 millimeter		
	Min	Nom	Max
A	0.496	0.533	0.57
A1	0.148	0.168	0.188
A2	0.037	0.04	0.043
b	0.18	0.21	0.24
S	0.3115	0.325	0.3385
D	1.565	1.59	1.615
E	1.411	1.436	1.461
e	0.35BSC		
D1	1.05BSC		
E1	1.05BSC		
SD	0.175		
SE	0.175		
n	16		

TSSOP16 package



SECTION B-B

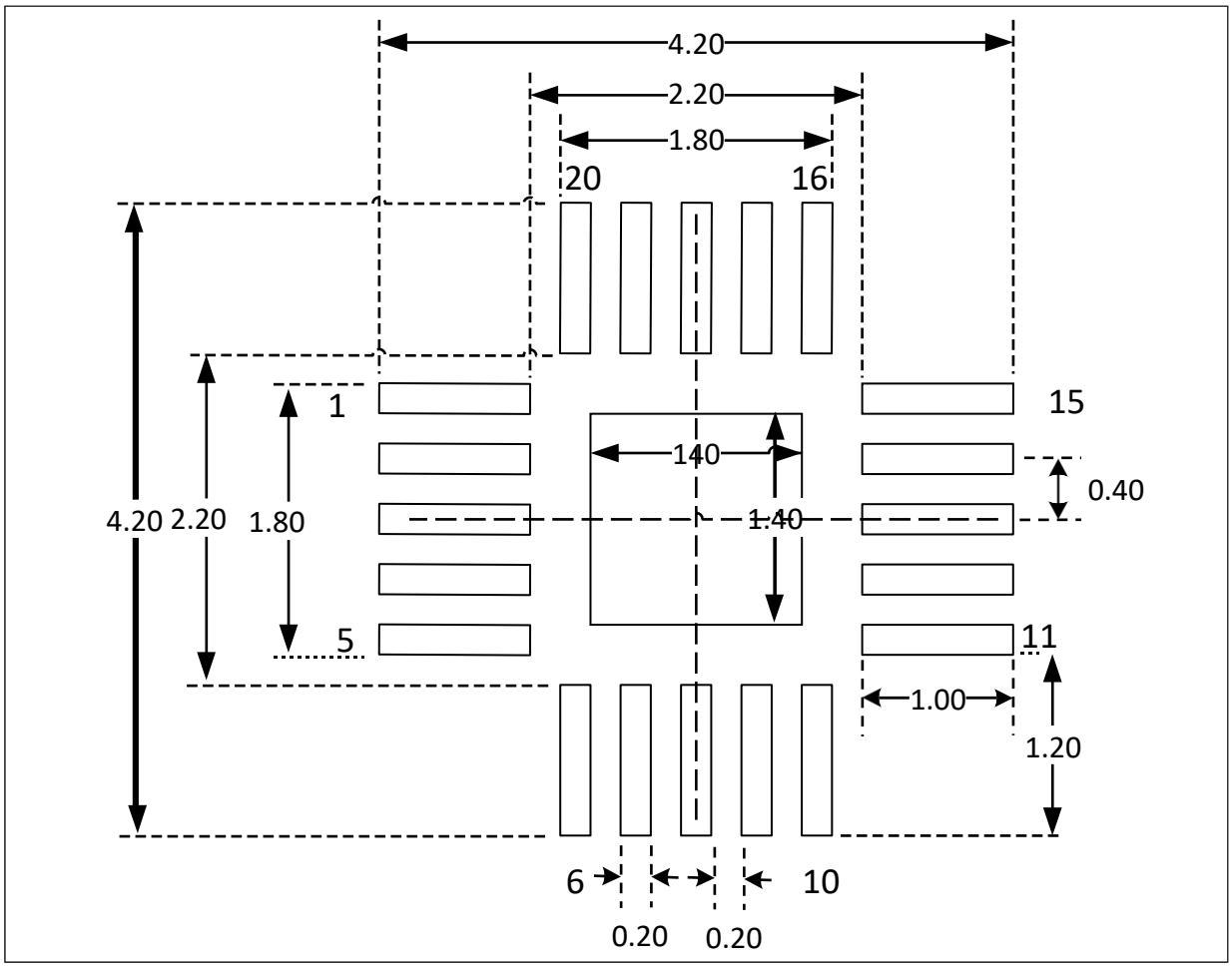
Symbol	TSSOP16 millimeter		
	Min	Nom	Max
A	--	--	1.20
A1	0.05	--	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	--	0.28
b1	0.19	0.22	0.25
c	0.13	--	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	--	8°

NOTE:

- Dimensions "D" and "E1" do not include mold flash.

9.2 Schematic diagram of solder pads

QFN20 package（3mm x 3mm）

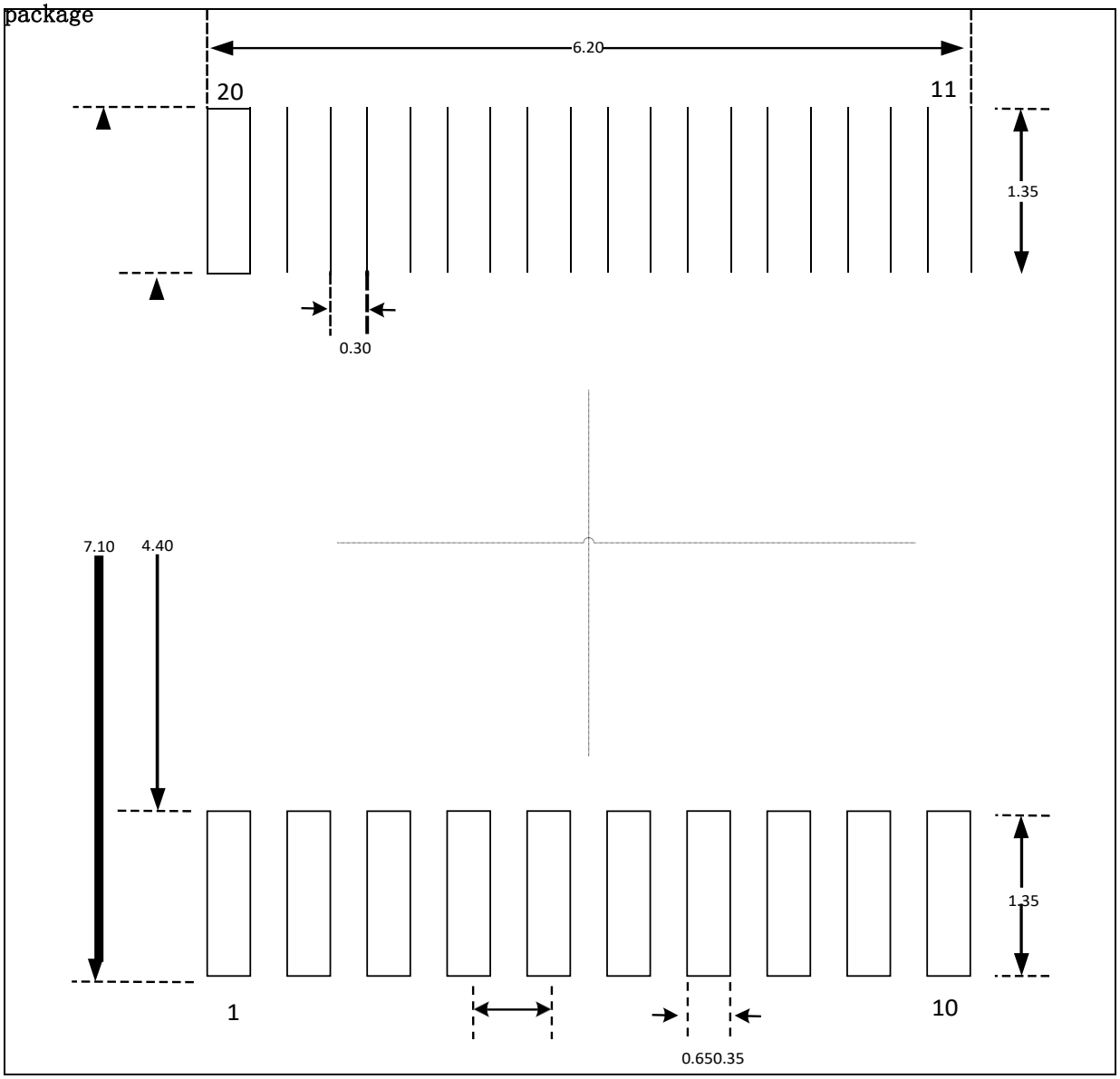


NOTE:

- **Dimensions are expressed in millimeters.**
- Dimensions are for reference only.

TSSOP20

package

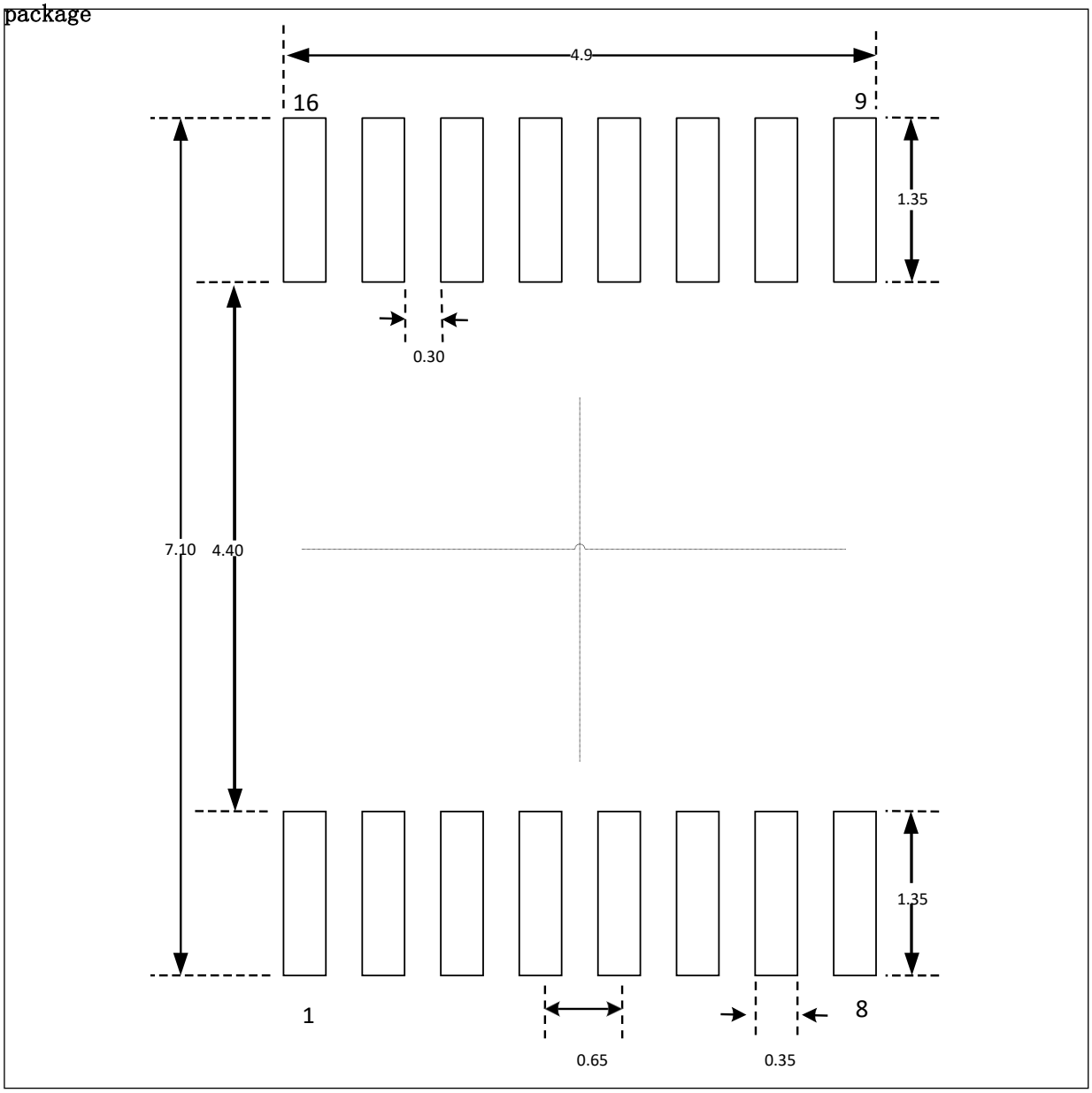


NOTE:

- **Dimensions are expressed in millimeters.**
- Dimensions are for reference only.

TSSOP16

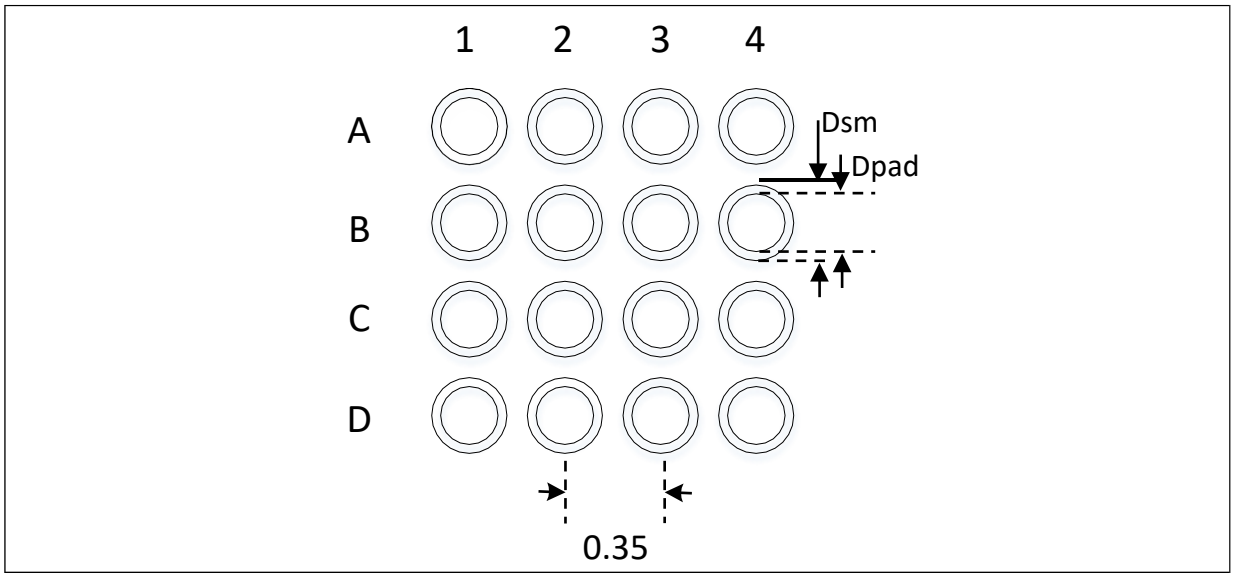
package



NOTE:

- **Dimensions are expressed in millimeters.**
- Dimensions are for reference only.

CSP16 Package



NOTE:

- **Dimensions are expressed in millimeters.**
- Dimensions are for reference only.

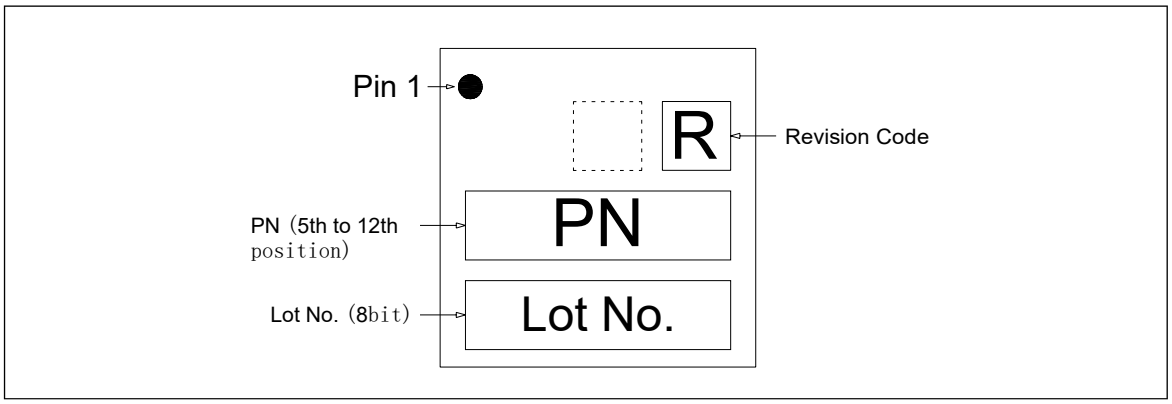
CSP16 recommended PCB design rules(0.35mm pitch)

Dimension	Recommended values
Pitch	0.35mm
Dpad	0.210mm
Dsm	0.275mm typ.（depends on the soldermask registration tolerance）
Stencil opening	0.235mm
Stencil thickness	0.100mm

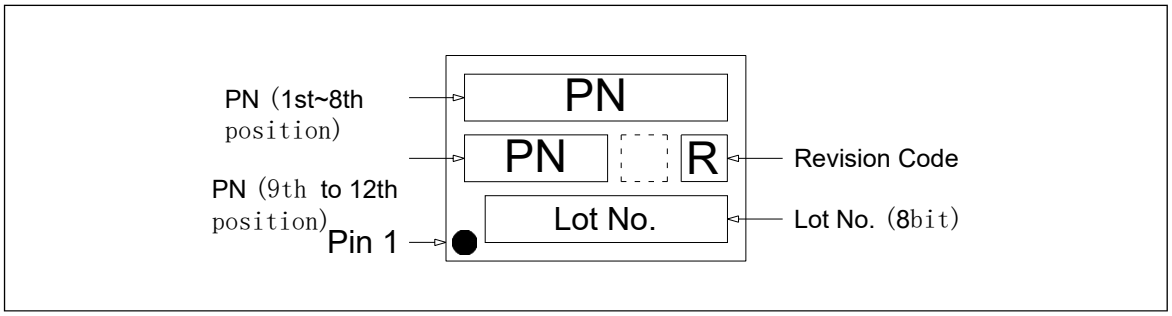
9.3 Silkscreen instructions

The pin locations land information on the front side of each package are described below.

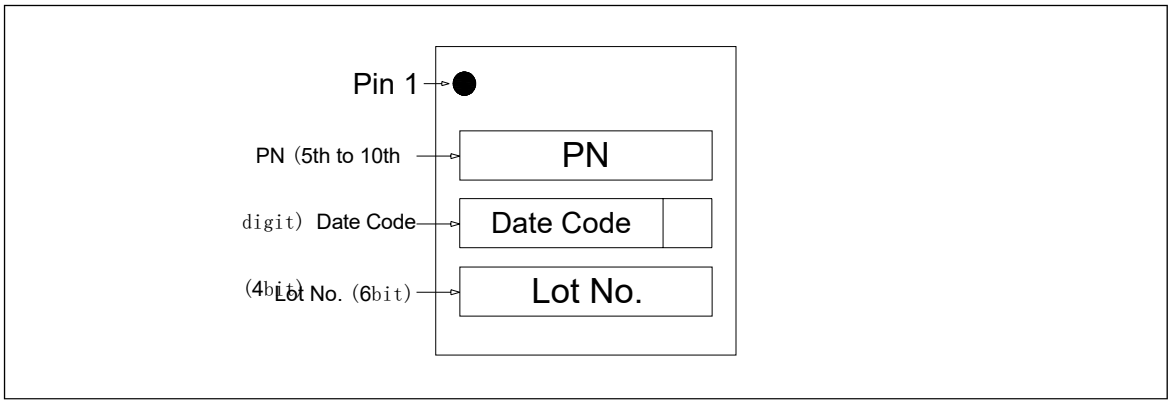
QFN20 package（3mm x 3mm）



TSSOP20 package / TSSOP16 package



CSP16 Package



Caution.

- The blank boxes above indicate optional production-related markers that are not described in this section.

9.4 Package thermal resistance coefficient

The junction temperature T_j(°C) on the chip surface when the packaged chip is operated at the specified operating ambient temperature can be calculated according to the following equation.

$$T_j = T_{amb} + (P_D \times \theta_{JA})$$

- T_{amb} is the operating ambient temperature in °C at which the package chip operates.
- θ_{JA} is the thermal resistance coefficient of the package to the operating environment in °C/W.
- P_D is the sum of the chip's internal power consumption and I/O power consumption in W. The chip's internal power consumption is the product's $I_{DD} \times V_{DD}$, and I/O power consumption refers to the power consumption generated by the I/O pins when the chip is operating, which is usually very small and can be ignored.

The junction temperature T_j on the chip surface when the chip is operating at the specified operating ambient temperature must not exceed the maximum junction temperature T_J that the chip can tolerate.

Package Type and Size	Thermal Resistance Junction-ambient Value (θ_{JA})	Unit
QFN20 3mm x 3mm / 0.4mm pitch	70 +/- 10%	℃/W
TSSOP16	105 +/- 10%	℃/W
TSSOP20	91 +/- 10%	℃/W

Table 9-1 Thermal resistance coefficient of each package

10. Ordering Information

Part Number	HC32L110C6UA-SFN20TR	HC32L110C6PA-TSSOP20	HC32L110B6PA-TSSOP16	HC32L110B6YA-CSP16TR	HC32L110C4UA-SFN20TR	HC32L110C4PA-TSSOP20	HC32L110B4PA-TSSOP16	HC32L110B4PA-TSSOP16TR
Flash	32KB	32KB	32KB	32KB	16KB	16KB	16KB	16KB
RAM	4KB	4KB	4KB	4KB	2KB	2KB	2KB	2KB
GPIO	16+1	16+1	12+1	12+1	16+1	16+1	12+1	12+1
Vdd	1.8~5.5V	1.8~5.5V	1.8~5.5V	1.8~5.5V	1.8~5.5V	1.8~5.5V	1.8~5.5V	1.8~5.5V
Timer	6	6	6	6	6	6	6	6
LPTimer	1	1	1	1	1	1	1	1
RTC	√	√	√	√	√	√	√	√
UART	2	2	2	2	2	2	2	2
LPUART	1	1	1	1	1	1	1	1
I2C	1	1	1	1	1	1	1	1
SPI	1	1	1	1	1	1	1	1
ADC(12bit)	9ch	9ch	6ch	6ch	9ch	9ch	6ch	6ch
Vcomp	2	2	2	2	2	2	2	2
LVD	√	√	√	√	√	√	√	√
LVR	√	√	√	√	√	√	√	√
Package	QFN20(3*3)	TSSOP20	TSSOP16	CSP16	QFN20(3*3)	TSSOP20	TSSOP16	TSSOP16
Foot spacing	0.4mm	0.65mm	0.65mm	0.35mm	0.4mm	0.65mm	0.65mm	0.65mm
Chip thickness	0.75mm	1.2mm	1.2mm	0.535mm	0.75mm	1.2mm	1.2mm	1.2mm
Shipment form	Tape and Reel	Tube fitting	Tube fitting	Tape and Reel	Tape and Reel	Tube fitting	Tube fitting	Tape and Reel

Before ordering, please contact the sales window for the latest mass production information.

11. Imprint & Contact

Versions	Revision Date	Summary of Revisions
Rev1.0	2018/1/23	First edition of HC32L110 series data sheet is released.
Rev1.1	2018/4/4	Version update.
Rev1.2	2018/4/17	Fix the Flash parameter.
Rev1.3	2018/5/3	Update VC electrical parameters.
Rev1.4	2018/9/25	Adjusted layout, updated chapter 7electrical characteristics, added chapter 9ordering information.
Rev1.5	2018/11/15	Add "Silkscreen Instructions" in Chapter8 1 to correct QFN20 / Tssop20 / Tssop16 package size.
Rev1.6	2018/11/27	Modify the name: UART2→LPUART, add "Note" in Chapter 3, etc. 4
Rev1.7	2019/2/22	Correction of the following data: ① ADC characteristics ② ESD characteristics ③ ECFLASH minimum value in memory characteristics ④ QFN20/TSSOP16 Package silkscreen description ⑤ Add NOTE to package size ⑥ Update ordering information ⑦ Add AVCC/AVSS to pin configuration
Rev1.8	2019/6/21	Corrected the following data: ①Corrected UID address to 0x0010_0E74-0x0010_0E7F ② Corrected programming mode ③Updated QFN lead Foot configuration diagram style ④ Add shipping form in the ordering information.
Rev1.9	2019/12/6	Correction of the following data: ① Typical application circuit diagram ② ADC characteristics unit ③ External clock source characteristics in XTH and XTL mapping and Caution.
Rev2.0	2020/1/17	Correct the following data: ①Add CSP16 package ②Silkscreen instructions.
Rev2.1	2020/3/6	Added a note to "Programming mode" in the introduction.
Rev2.2	2020/4/30	Correct the following data: ①Add VCC/3 accuracy in ADC characteristics ②Correct7.3.7 the pen error in ③RCL oscillator accuracy 7.3.8in
Rev2.3	2020/7/31	Fix the following data: ① Add 7.3.16 、7.3.17 ， ， and9.29.4section; ② 7.3.10level; ③ 7.3.1internal AHB/APB clock Frequency; ④ 7.3.12Input characteristics - the values of V_{IH} and V_{IL} in ports P0, P1, P2, P3, and RESET.
Rev2.4	2020/9/30	Correct the following data: (1) the description of clock system in the introduction; (2) the accuracy of RCH oscillator 7.3.8in the introduction; (3) the V_{IL} and V_{IH} 7.3.13of the RCH; and (4) the V_{IL} and V_{IH} of the RCH. Add SPI feature.
Rev2.5	2021/5/31	Fix the following data: (i) modify the declaration; (ii) $t_{HD.STA}$ and $t_{SU.STO}$ parameters in the I2C feature; (iii) serial peripheral interface SPI in the profile. ④ Data retention period in memory feature; ⑤ Add g_m parameter in external clock source feature.

If you have any comments or suggestions in the process of purchase and use, please feel free to contact us.

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