

32 -bit microcontroller

Clock Control Module for **HC32L110 / HC32F003 / HC32F005** Series

Applicable object

	X.
series	Product number
HC32L110	HC32L110C6UA
	HC32L110C6PA
	HC32L110C4UA
	HC32L110C4PA
	HC32L110B6PA
	HC32L110B4PA
HC32F003	HC32F003C4UA
	HC32F003C4PA
HC32F005	HC32F005C6UA
	HC32F005C6PA
	HC32F005D6UA



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1 Summary

Inis application note mainly introduces the clock control module of HC32L110 / HC32F003 / HC32F005 series.
This application note mainly includes:
ÿ Introduction of system clock module
ÿ Turn on the clock source
ÿ Switching of clock sources
ÿ RCH frequency switching
ÿ Frequency division control of clock
ÿ Control of peripheral clock
Notice:
- This application note is an application supplement for the HC32L110 / HC32F003 / HC32F005 series and is not intended to replace the user manual.
Please refer to the user manual for specific functions and register operations.

2 Function introduction

The clock control module can configure different clock sources as the system clock, configure different system clock frequency divisions, and enable

The peripheral clocks can be activated or disabled, and the internal clocks are calibrated to ensure high accuracy.



3 Clock Control Module

3.1 Schematic diagram of the clock tree

The schematic diagram describes the connection, frequency division relationship and related configuration registers from the clock source to System CLK, HCLK, PCLK device. Referring to the schematic diagram, you can quickly become familiar with the clock control module.

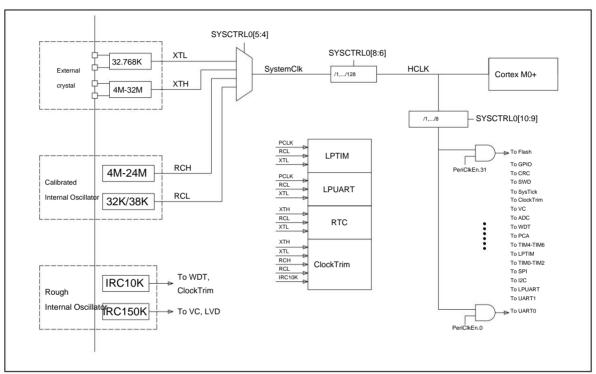


Figure 1. System Clock Tree

3.2 Introduction to Clock Sources

Clock source is a general term for MCU internal clock and external clock. This series of chip clock sources include the following types:

ÿ System clock

- External low-speed clock (XTL): external 32.768K crystal oscillator, used for working modules in ultra-low power consumption mode
- External high-speed clock (XTH): 4M~32M crystal oscillator can be externally connected according to actual needs
- Internal high-speed RC clock (RCH): the default system clock, which can be used for fast system startup and fast wake-up
- Internal low-speed RC clock (RCL): can be used for low-speed, low-precision application scenarios

Note: RCH, XTL and XTH can also be configured to be input by an external clock source through the P31, P14 and P01 ports respectively.

Note: XTL only supports HC32L110 series.

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ÿ Other clocks

- Internal low-speed clock (IRC10K): Provided for WDT and Clock Trim modules
- Internal low-speed clock (IRC150K): used for internal debounce, provided for VC and LVD modules

3.3 Turn on the system clock source

The steps to turn on the system clock source are as follows:

- 1. Set the stabilization time according to the selected clock:
- RCL: configure RCL_CR.STARTUP
- XTH: configure XTH_CR.STARTUP
- XTL: configure XTL_CR.STARTUP
- 2. If an external clock is selected, set the IO corresponding to the clock as an analog input according to the selected clock:
 - XTH: Set P0ADS.P0ADS1 and P0ADS.P0ADS2
 - XTL: Set P1ADS.P1ADS4 and P1ADS.P1ADS5
- 3. If external clock is selected, set the drive capability according to the selected clock:
 - XTH: configure XTH_CR.DRIVER
 - XTL: configure XTL_CR.DRIVER
- 4. Load the TRIM values:
 - RCH: configure RCH_CR.TRIM
 - RCL: configure RCL_CR.TRIM
- 5. Enable the selected clock:
 - RCH: set SYSCTRL0.RCH_EN
 - RCL: set SYSCTRL0.RCL_EN
 - XTH: set SYSCTRL0.XTH_EN
 - XTL: set SYSCTRL0.XTL_EN
- 6. Wait for the selected clock source to stabilize:

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-	RCH:	wait	tor	RCH_	_CR.S	IABLE	to sta	abilize

- RCL: wait for RCL_CR.STABLE to stabilize
- XTH: wait for XTH_CR.STABLE to stabilize
- XTL: wait for XTL_CR.STABLE to stabilize

Note: XTL only supports HC32L110 series.

3.4 Switching of clock sources

The switching steps of the clock source are as follows:

- 1. If the target clock or current clock frequency is higher than 24MHz, set the FLASH read wait period:
 - set FLASH_CR.WAIT
- 2. Turn on the target clock source (Reference: 3.3 Turning On the System Clock Source)
- 3. Switch the clock:
 - Configure SYSCTRL0.CLK_SW4_SEL;
- 4. Select whether to turn off other clock sources as required:
 - RCH: clear SYSCTRL0.RCH_EN
 - RCL: clear SYSCTRL0.RCL_EN
 - XTH: clear SYSCTRL0.XTH_EN
 - XTL: Clear SYSCTRL0.XTL_EN

Notice:

 \ddot{y} Attention must be paid to the switching of the clock source: before the clock switching, it is necessary to determine the maximum frequency of the current clock and the target clock.

Whether to increase the FLASH read waiting period; after the clock is switched successfully, it can be set according to the switched clock frequency value

Or clear the FLASH read wait cycle.

- XTL only supports HC32L110 series.

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If you need to switch in each frequency band of the RCH, it is recommended to follow the following procedures:

3.5 RCH frequency switching

	1. Switch the system clock source to RCL;
	2. According to the frequency of the target RCH, load and update the RCH_CR.TRIM value;
	3. Switch the system clock source to RCH.
3.6 Clock fr	requency division control
	In practical applications, any clock source can be selected as the system clock as required. After the system clock is divided, it can be used as the CPU
	As the clock (HCLK), the peripheral clock (PCLK) can be obtained by dividing the frequency of HCLK.
	When a clock source is selected as the system clock, an appropriate clock can be obtained according to actual needs. For the configuration reference of clock frequency division
	Proceed as follows:
	Configure the HCLK division factor:
	- Configure SYSCTRL0.HCLK_PRS
	2. Configure the PCLK division factor:
	- Configure SYSCTRL0.PCLK_PRS
3.7 Control	of peripheral clock
	The peripheral clock source has gating settings, and the corresponding peripherals can be configured and working only when the gating settings are turned on. except for some basic
	The peripherals are turned on by default, and most of the peripherals are turned off by default when they are powered on. Before enabling a peripheral, it is necessary to enable the corresponding peripheral
	clock switch.
	To turn on the clock of the peripheral module, you need to enable the control bit of the module corresponding to PERI_CLKEN;
	To turn off the clock of the peripheral module, the control bit of the module corresponding to PERI_CLKEN needs to be cleared.
	Note: In (ultra) low-power mode, the clocks of modules that are not in use can be turned off as needed to reduce power consumption.



4 Reference samples and drivers

Through the above introduction, together with the user manual of HC32L110 / HC32F003 / HC32F005 series, we

The function and operation method of the clock control module of the MCU have been further mastered.

Huada Semiconductor (HDC) officially provides the application sample and driver library of this module at the same time. Users can open the sample by opening the

The project is further intuitively familiar with the application of the module and the driver library, and can also directly refer to the sample and use in the actual development

Driver library to quickly implement the operation of this module.

ÿ Example reference: ~/HC32L110_DDL/example/clk

~/HC32F003_DDL/example/clk

~/HC32F005_DDL/example/clk

ÿ Driver library reference: ~/HC32L110_DDL/driver/.../clk

~/HC32F003_DDL/driver/.../clk

~/HC32F005_DDL/driver/.../clk

5 Summary

The above chapters briefly introduce the basic functions of the clock control module of the HC32L110 / HC32F003 / HC32F005 series.

Describes the functions and operation steps of the clock module. In the actual application development process, if the user needs to go further

To understand the usage and operation of this module, please refer to the corresponding user manual. Examples and drivers mentioned in this chapter

The library can be used as a user for further experimentation and learning, or can be directly applied in actual development.

6 Other information

Technical support information: www.hdsc.com.cn

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7 Version Information & Contact Information

date	Version revi	sion record
2018/6/4	Rev1.0 initia	al release



If you have any comments or suggestions in the process of purchasing and using, please feel free to contact us.

Email: mcu@hdsc.com.cn

Website: www.hdsc.com.cn

Mailing address: No. 39, Lane 572, Bibo Road, Zhangjiang Hi-Tech Park, Shanghai

Postcode: 201203



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