HDSC 华大半导体 HUADA SEMICONDUCTOR

32 Bit Microcontrollers

HC32L110 / HC32F003 / HC32F005 Series

Hardware Development Guide

Applicable objects

Series	Product Model
HC32L110	HC32L110C6UA HC32L110C6PA HC32L110C4UA HC32L110C4PA HC32L110B6PA HC32L110B4PA
HC32F003	HC32F003C4UA HC32F003C4PA
HC32F005	HC32F005C6UA HC32F005C6PA HC32F005D6UA

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1 Abstract

This application note mainly introduces the peripheral hardware design based on HC32L110 / HC32F003 / HC32F005 series chips, including power supply, GPIO, crystal, UART, SWD, I2C, device package, minimum system reference hardware design, etc.

Caution.

- This application note is an application supplement for HC32L110 / HC32F003 / HC32F005 series, and cannot replace the user's manual. Please refer to the user's manual for specific functions and register operations and other related matters.

2 Power supply

Each group of power supply (DVCC/AVCC) needs a decoupling capacitor 4.7uF + bypass capacitor 0.1uF, PCB layout, the capacitor as close as possible to the corresponding power supply pins.

VCAP pin of the chip: LDO core power output pin (internal circuit use only, external 4.7uF + 10nF decoupling capacitor is required); no external load can be connected.

All power (DVCC/AVCC) and ground (DVSS/AVSS) pins must always be connected to a power supply system within the MCU operating voltage range.

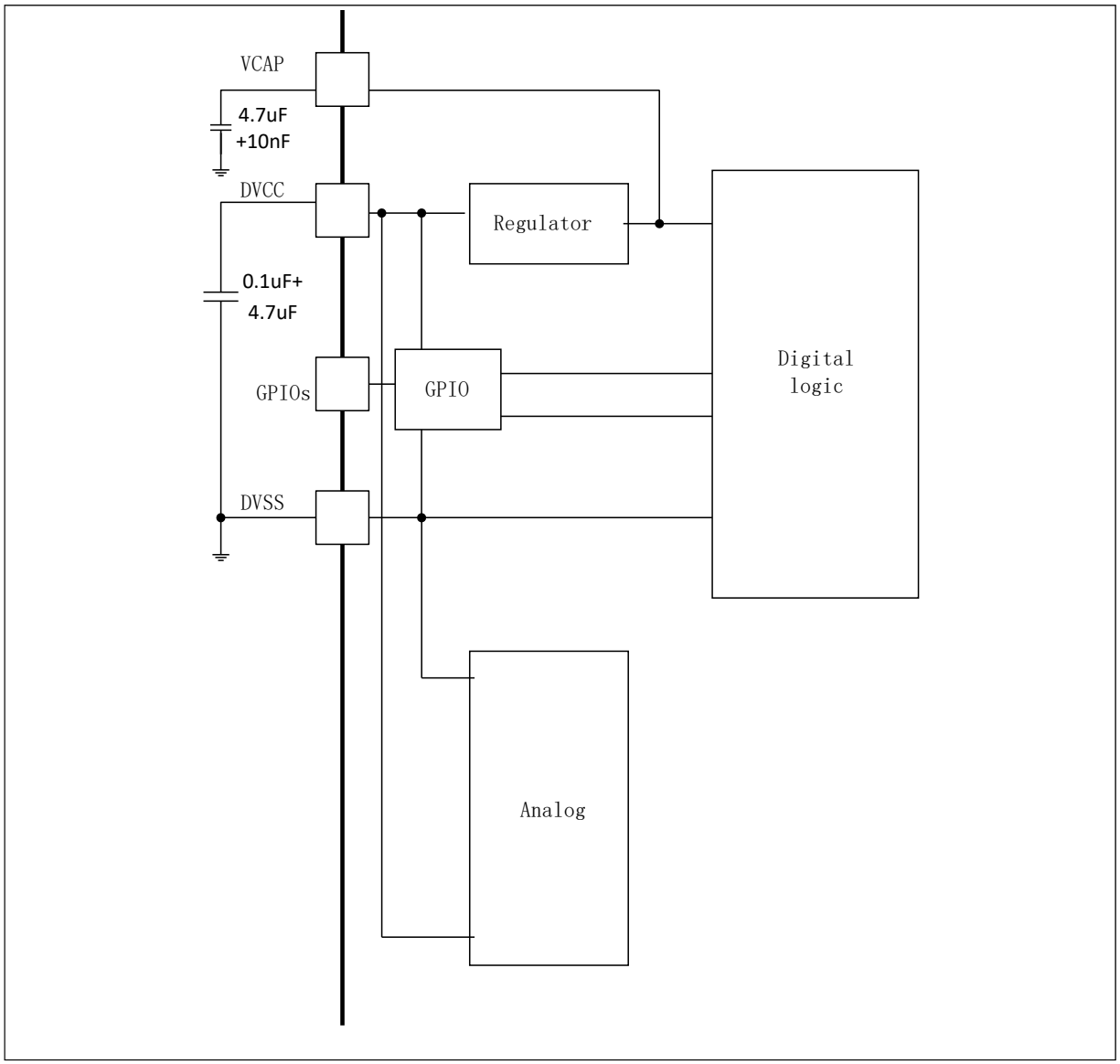


Figure 1Decoupling Capacitor

MCU operating voltage range: 1.8V ≤ DVCC/AVCC ≤ 5.5V.

3 Reset circuit

When designing, connect a capacitor between the RESETB pin and ground (DVSS) to form an RC delay circuit with a pull-up resistor; if RESETB is not used in the application, RESETB must be pulled up to DVCC through a resistor (4.7K recommended).

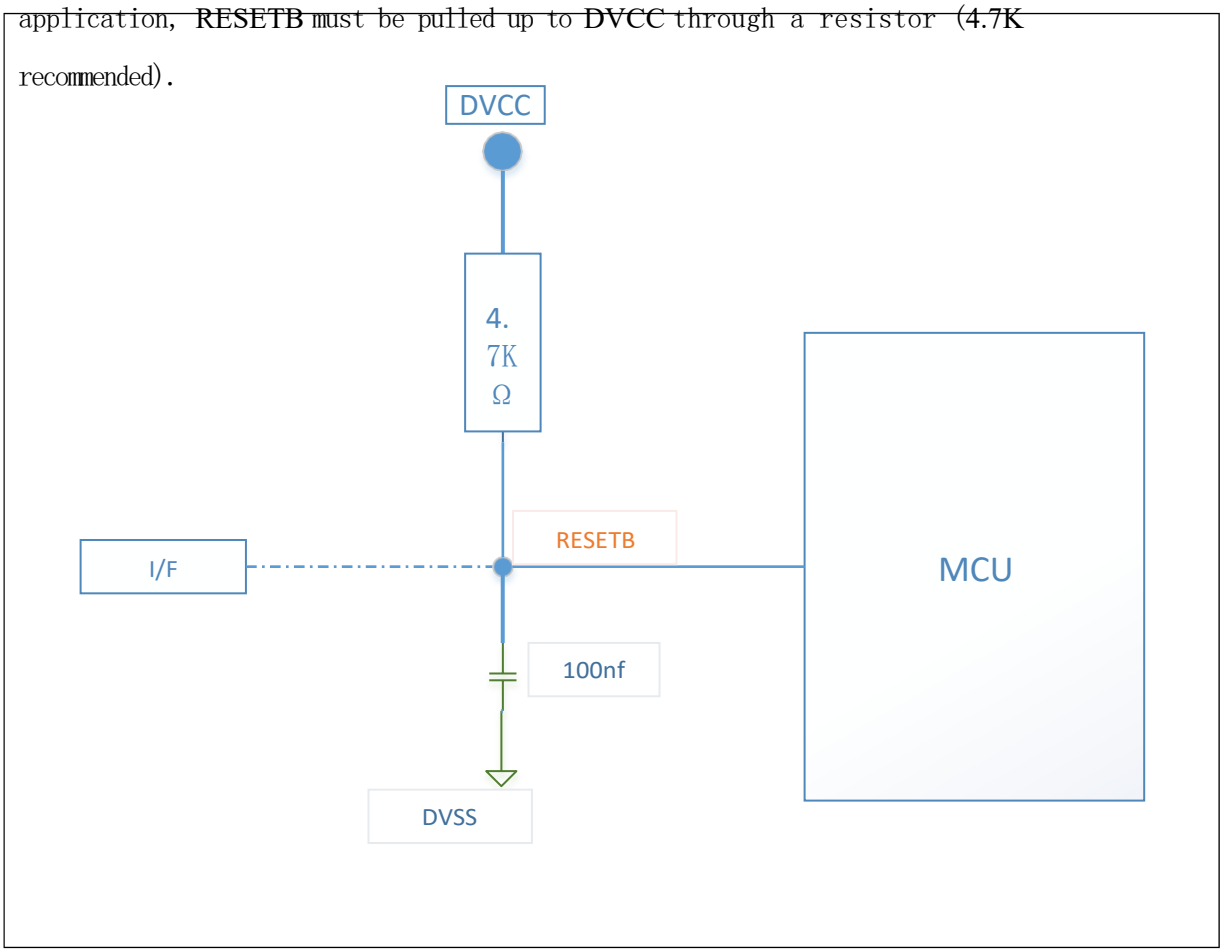


Figure NRST2 Circuit

4 GPIO

A maximum of one16 GPIO port is available, with some GPIOs multiplexed with analog ports. Each port is controlled by a separate control register bit. Edge-triggered interrupts and level-triggered interrupts are supported to wake up the MCU to operating mode from various ultra-low power modes. Supports Push-Pull CMOS push-pull output and Open-Drain open-drain output. Built-in pull-up resistor, pull-down resistor, and Schmitt trigger input filtering function. Configurable output drive capability, supports up to 12mA current drive capability. 16 External asynchronous interrupts can be supported for each general purpose IO.

Caution.

- The RESETB port can also be configured as GPIO input port P00 when the NRST function is not used.

5 Crystal oscillator circuit design

5.1 Circuit Design

The high speed external clock (XTH) can be generated using an oscillator consisting of a4 to 32 MHz crystal/ceramic resonator. Both pins have load capacitors. In applications, the resonator and load capacitors must be placed as close as possible to the oscillator pins to minimize output distortion and stabilization time at startup. For detailed parameters of crystal resonators (frequency, package, accuracy, etc.), please consult the appropriate manufacturer.

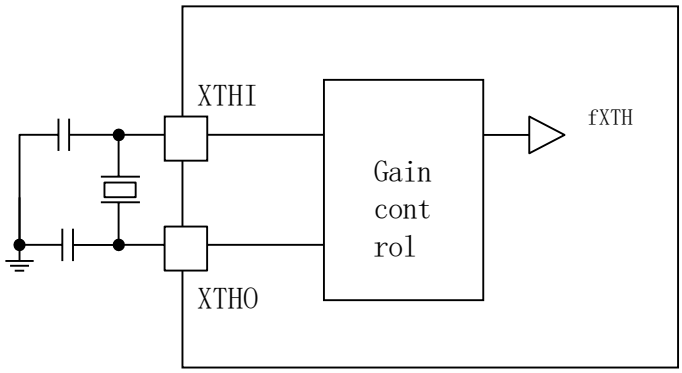


Figure Diagram of external 3high-speed crystal

The low-speed external clock (XTL) can be generated using an oscillator consisting of a32.768KHz crystal/ceramic resonator. Both pins have load capacitance. In applications, the resonator and load capacitor must be as close to the oscillator pins as possible to minimize output distortion and stabilization time at startup. For detailed parameters of crystal resonators (frequency, package, accuracy, etc.), please consult the appropriate manufacturer.

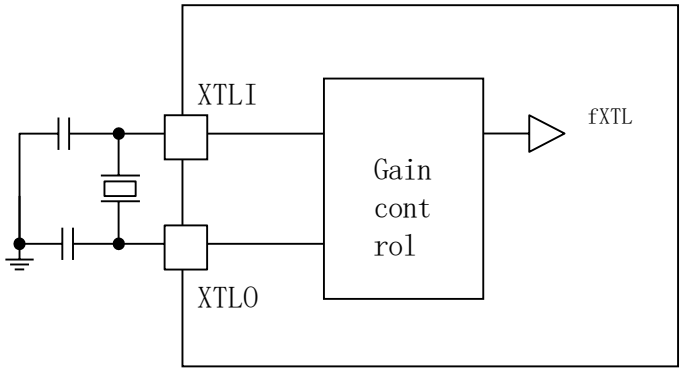


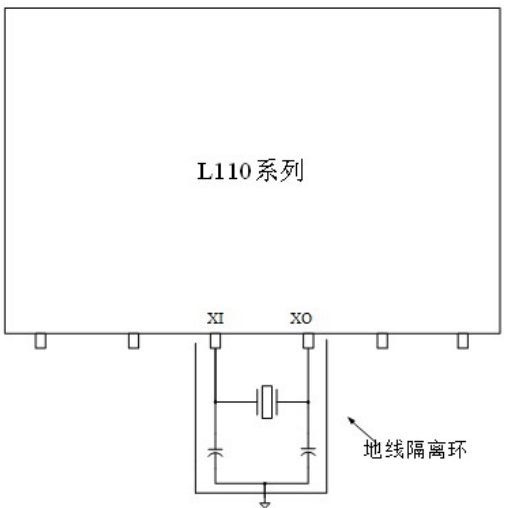
Figure Diagram of external4 low-speed crystal

Caution.

- When reading the datasheet provided by the crystal manufacturer, the parameter load capacitance CL (Load capacitance) refers to the total effective capacitance across the crystal terminals in the circuit, not the external matching capacitance of the crystal; in addition, when calculating the matching capacitance value of the crystal circuit, you need to take into account the parasitic capacitance of the layout line to ground of the crystal circuit PCB.

5.2 Circuit layout

- The external crystal unit and load capacitor should be as close to the chip side as possible.
- External crystal signal line alignment should be as short as possible. The width of the line should not be too thin, the thinnest should not be lower than the width of the chip pin.
- In the crystal local circuit adjacent to the layerlayer, there should be a complete overlay.
- The external crystal should be surrounded by the ground line to make a protective isolation ring (guard ring), the ground ring line needs to be fully grounded (more over the ground hole), to reduce the external crystal signal and other signals between the mutual interference. (Reference Figure 5)
- Crystal circuit should pay attention to the local signal clean, to avoid external interference. In the vicinity of the crystal circuit or adjacent layer layer as far as possible not to take the line, especially not allowed to take high-speed lines, power lines, clock lines, etc..



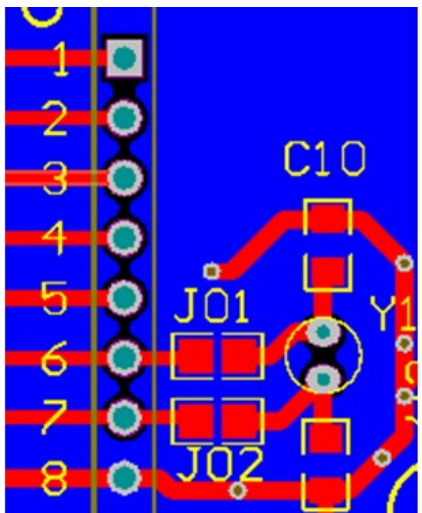


Figure Crystal5 circuit ground isolation ring

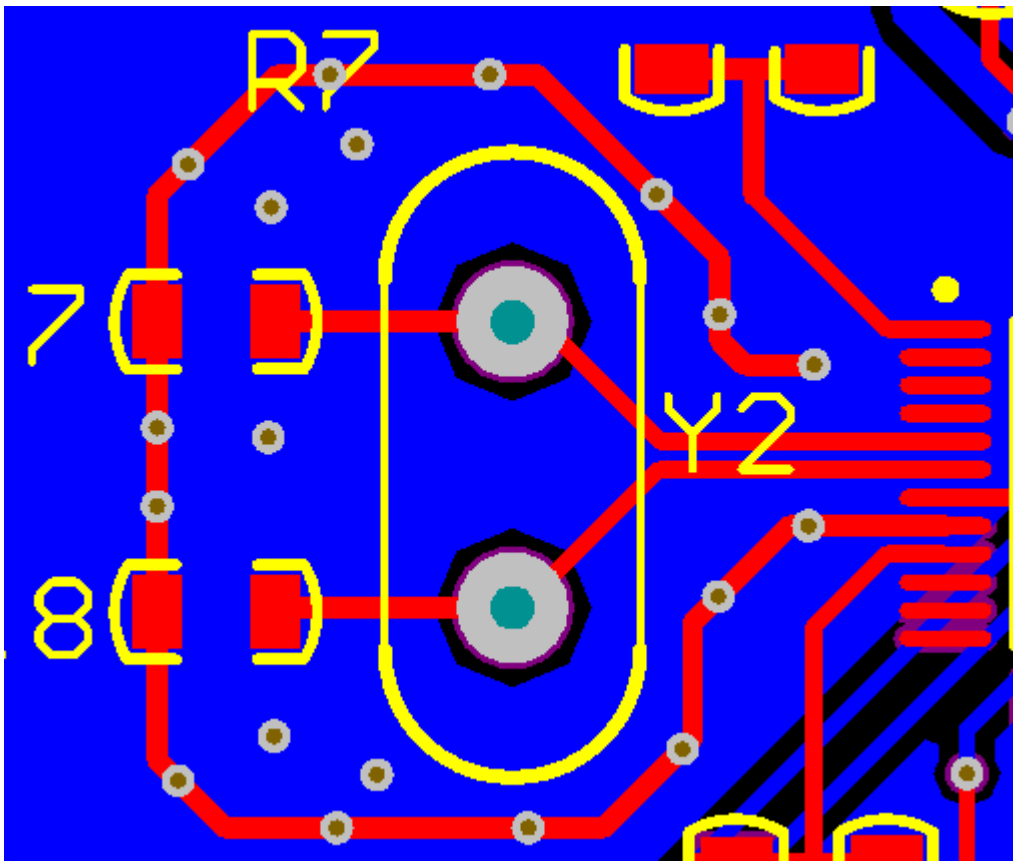


Figure Crystal6 circuit overall layout, filtering, package ground isolation design schematic

6 Common interface design

6.1 UART Interface Design

For UART interface design, it is recommended that the TX/RX signal line be connected to a 4.7KΩ pull-up resistor for power supply.

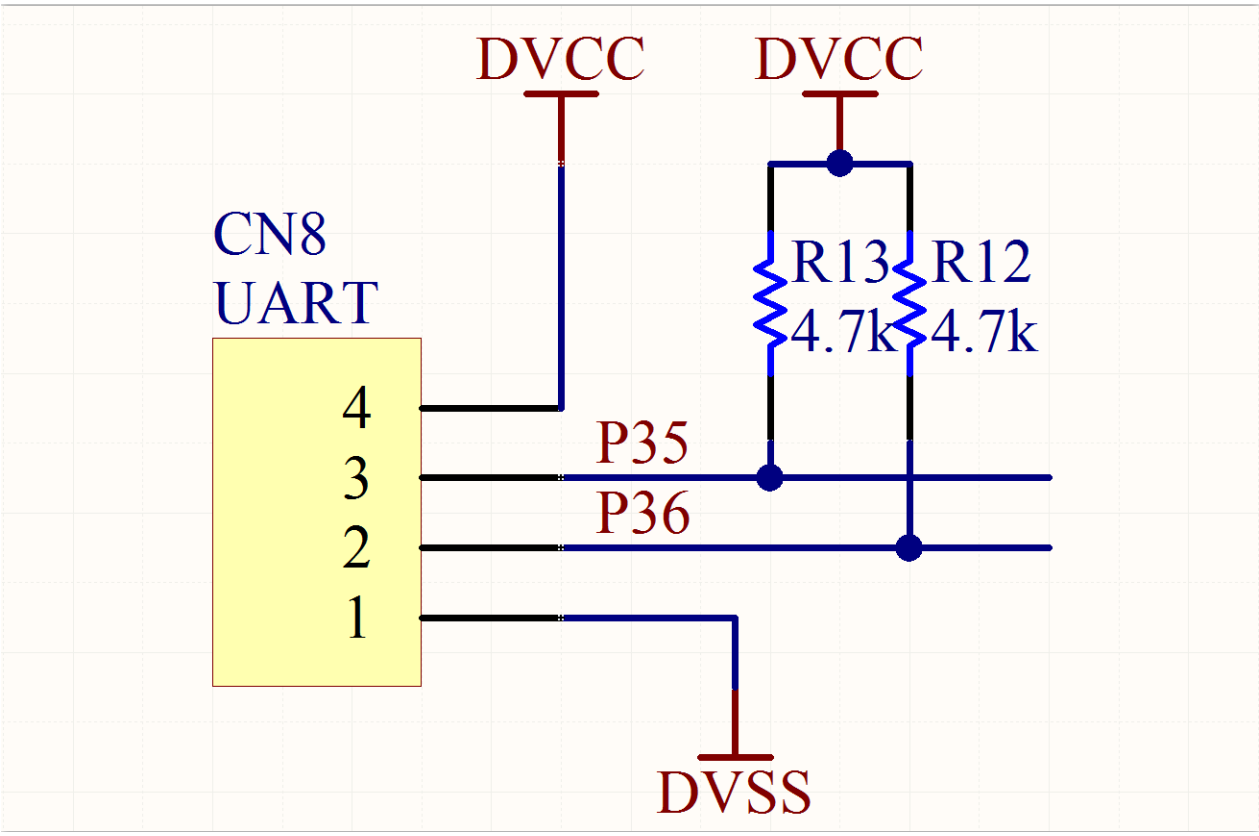


Figure UART7 interface design schematic

6.2 SWD Interface Design

For SWD interface design, it is recommended that the SWCLK/SWDIO signal line be connected to a 4.7KΩ pull-up resistor to the power supply.

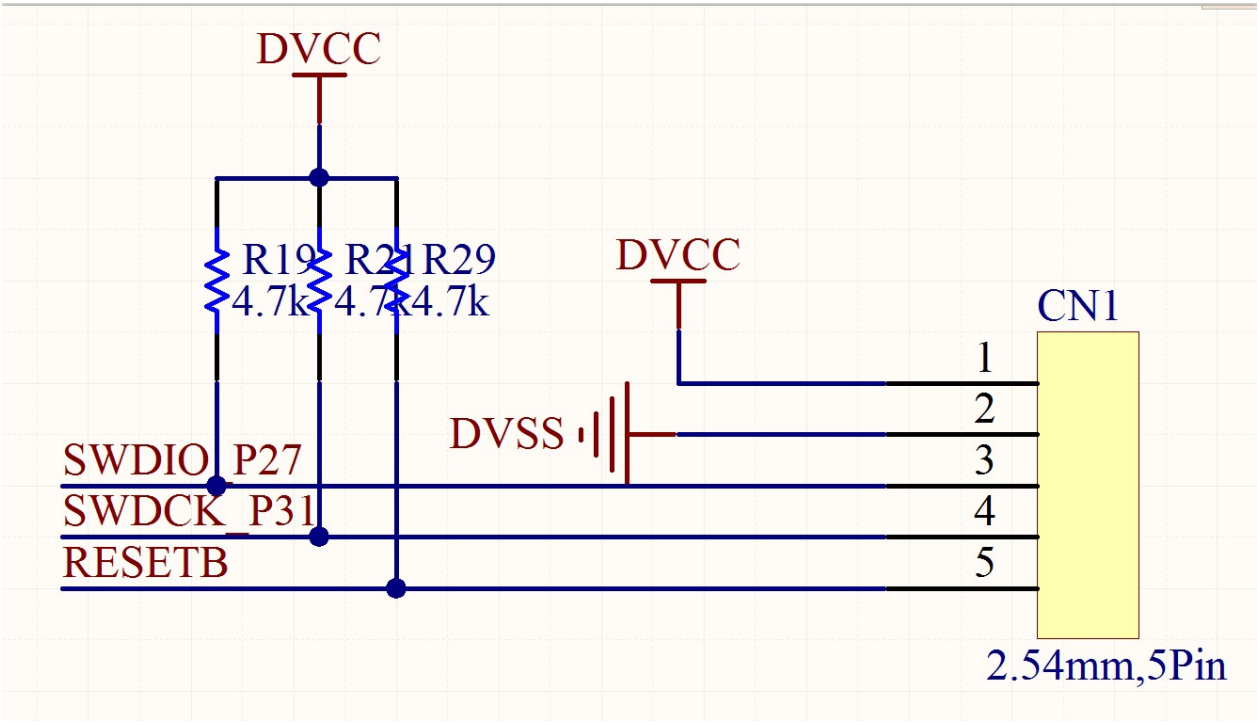


Figure SWD8 interface design schematic

6.3 I2C Interface Design

For I2C interface design, it is recommended that the I2C_SCL/I2C_SDA signal line be connected to a 1KΩ pull-up resistor to the power supply.

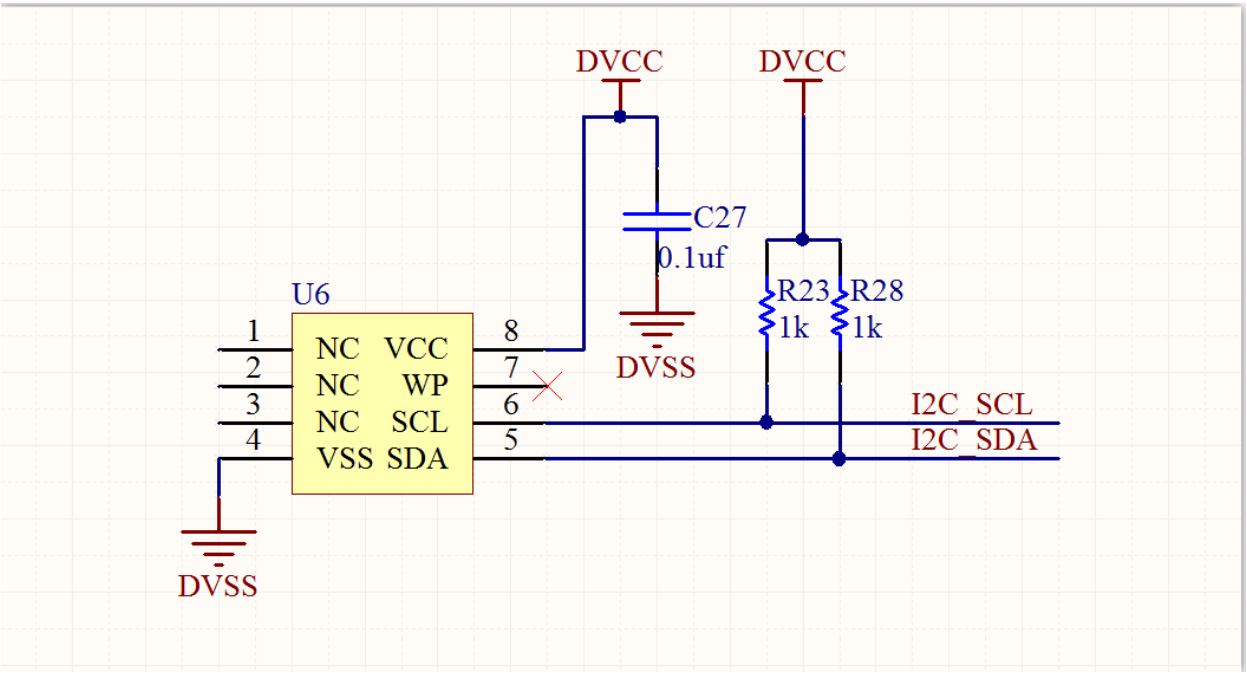


Figure I2C9 interface design schematic

7 Chip Packaging PCB Layout

Please refer to the "Package Information" section of the chip datasheet published by our company. Please design the chip package Layout strictly according to the data sheet specifications. In addition, we provide all PCB package libraries for this series of chips, please refer to http://www.hdsc.com.cn/mcu.htm.

8 Application circuit (minimum system, for reference only)

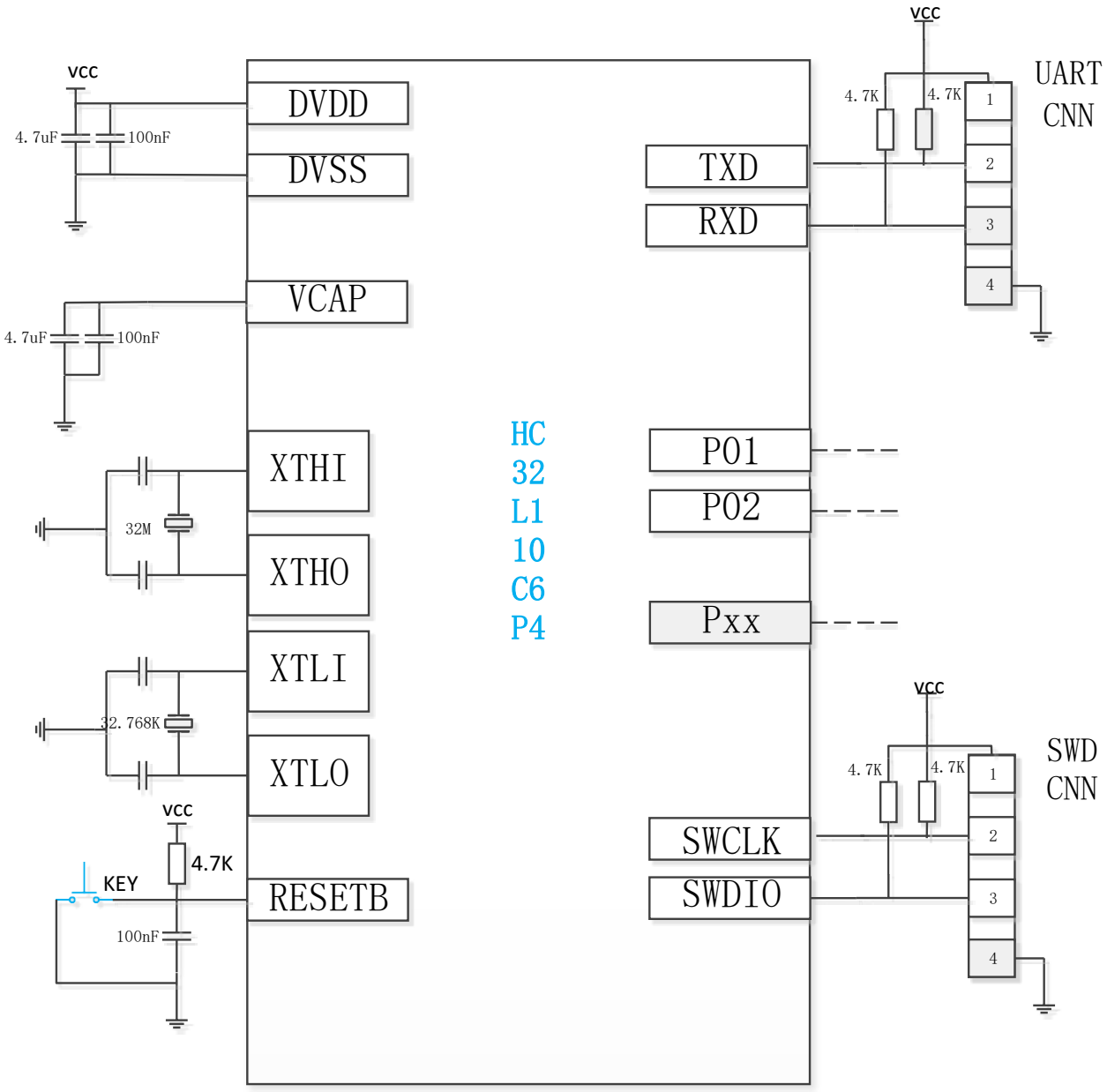


Fig. Reference diagram of the minimum system design of the 10chip

9 Comparison of the pin configuration of the HC32F003/HC32F005 and the X003 series of friendly products

9.1 TSSOP20 Pin Configuration Differences

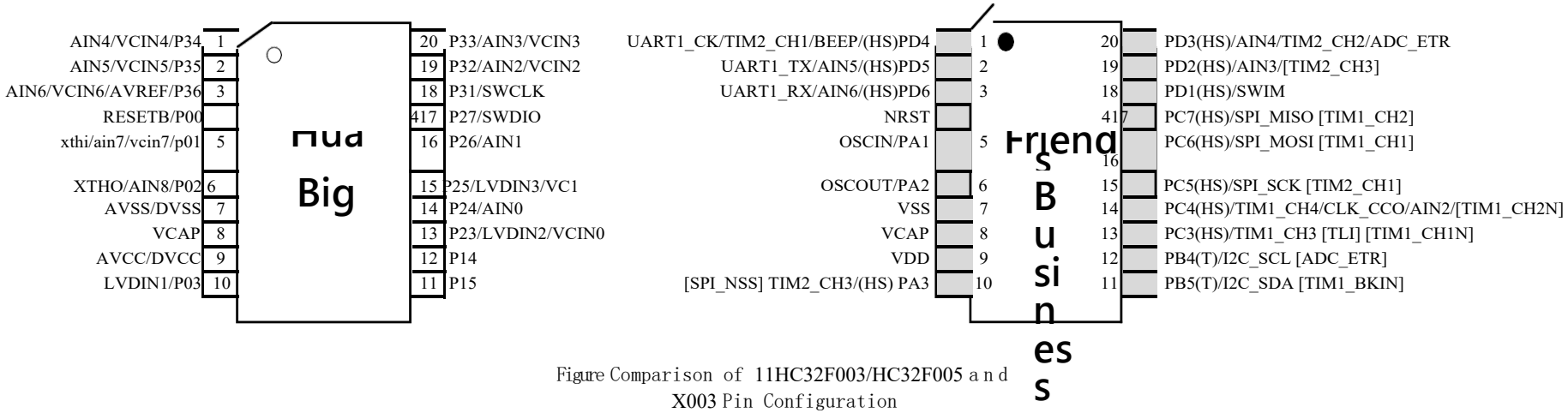


Figure Comparison of 11HC32F003/HC32F005 and X003 Pin Configuration

Table List of pin configuration differences between the UW1 chip and the friendly chip TSSOP20

Chip Model	**HC32L110C6PA/ HC32L110C4PA /hc32f005c6pa/ hc32f005c4pa**	**x003**
Pin17	P27/SWDIO	PC7
Pin18	P31/SWCLK	PD1/SWIM

Description.

- UW's chip Pin17/Pin18 constitutes the SWD burning port, while the friendly chip Pin18 is the single-line program burning port.

SWIM.

10 Other Information

Technical support information: www.hdsc.com.cn

11 Version Information & Contact

Date	Versions	Modify records
2019/6/14	Rev1.0	Initial release.

If you have any comments or suggestions in the process of purchase and use, please feel free to contact us.

Email: mcu@hdsc.com.cn

Website: http://www.hdsc.com.cn/mcu.htm

Address: No. Lane39, Bebo Road, Zhangjiang Hi-Tech Park, Shanghai,572 China

Zip code.201203