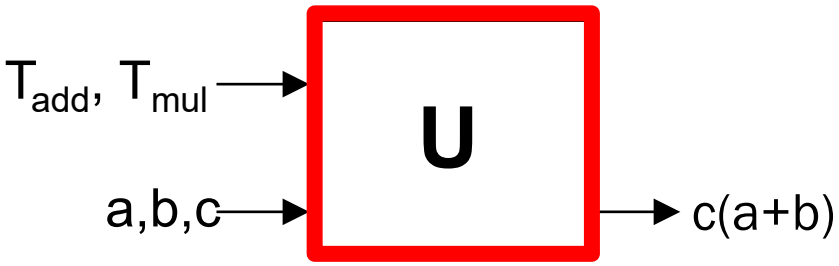
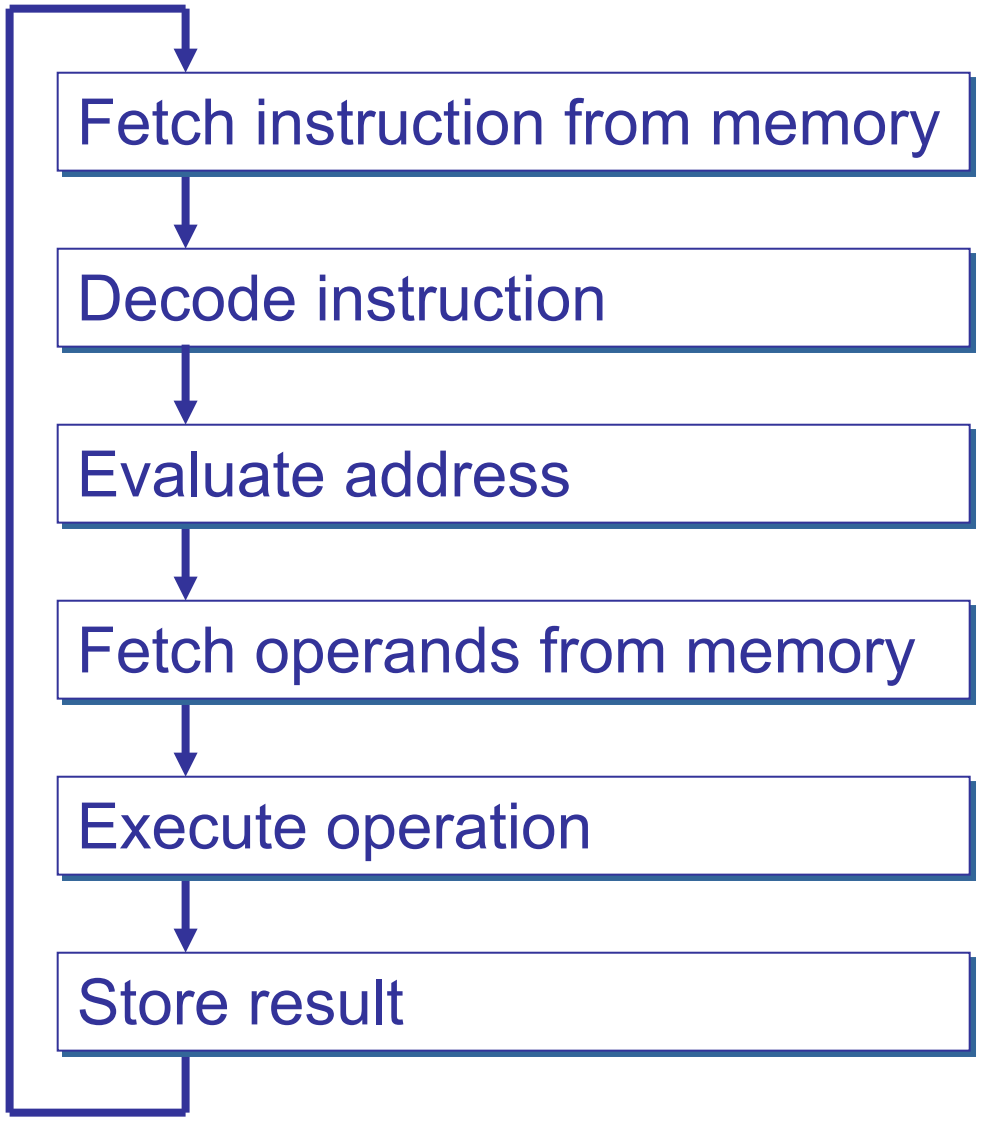
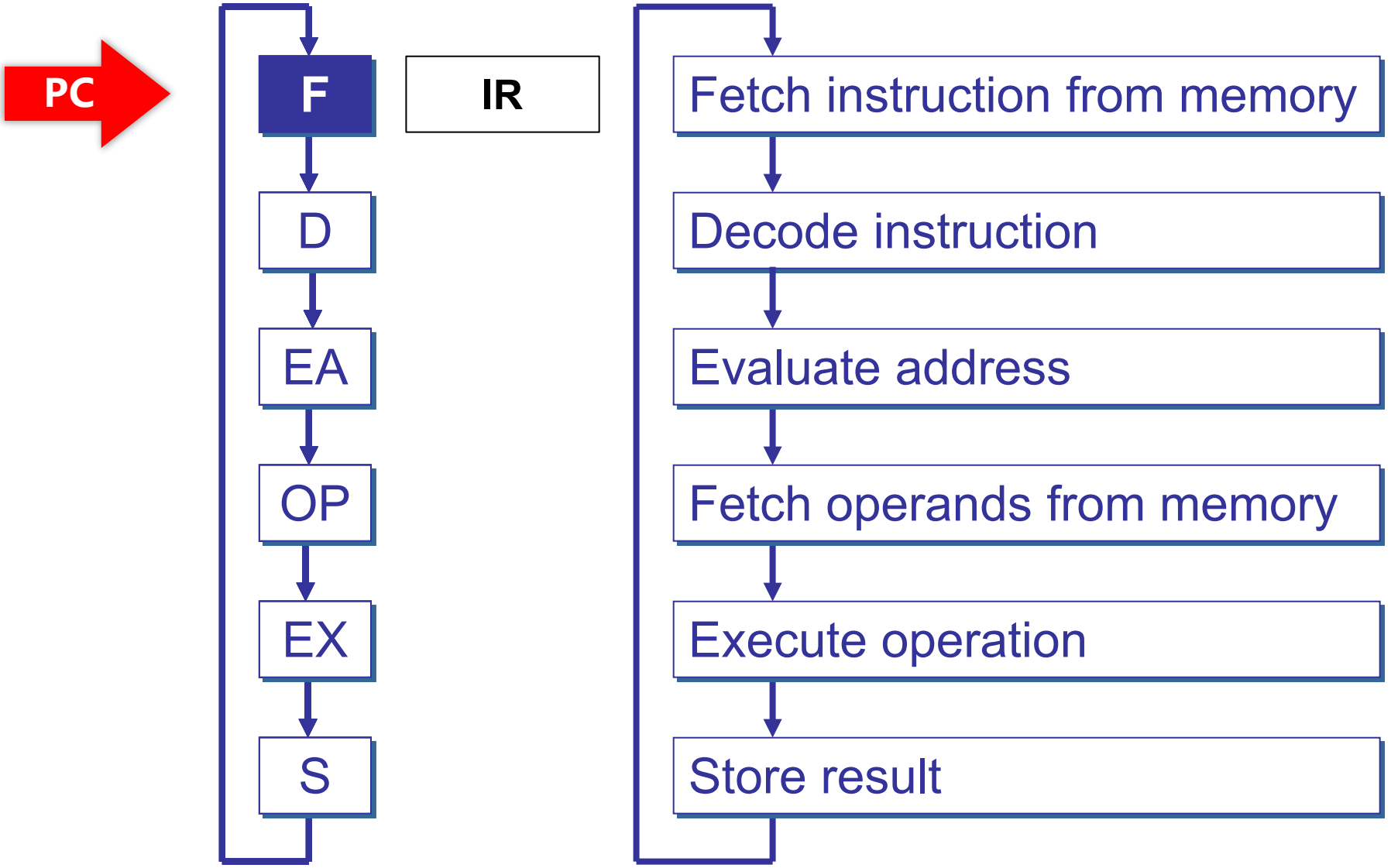
Great Idea #1 Turing Machine (Computataional Model)



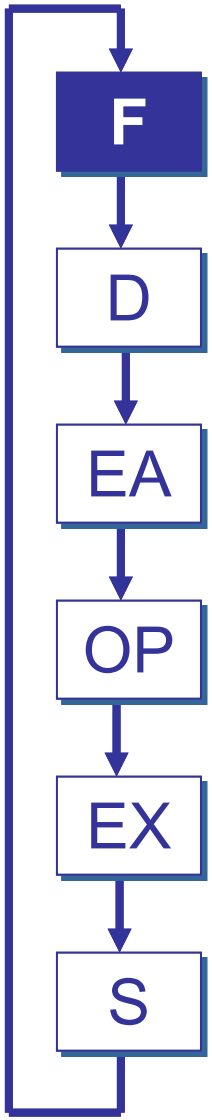
Universal Turing Machine

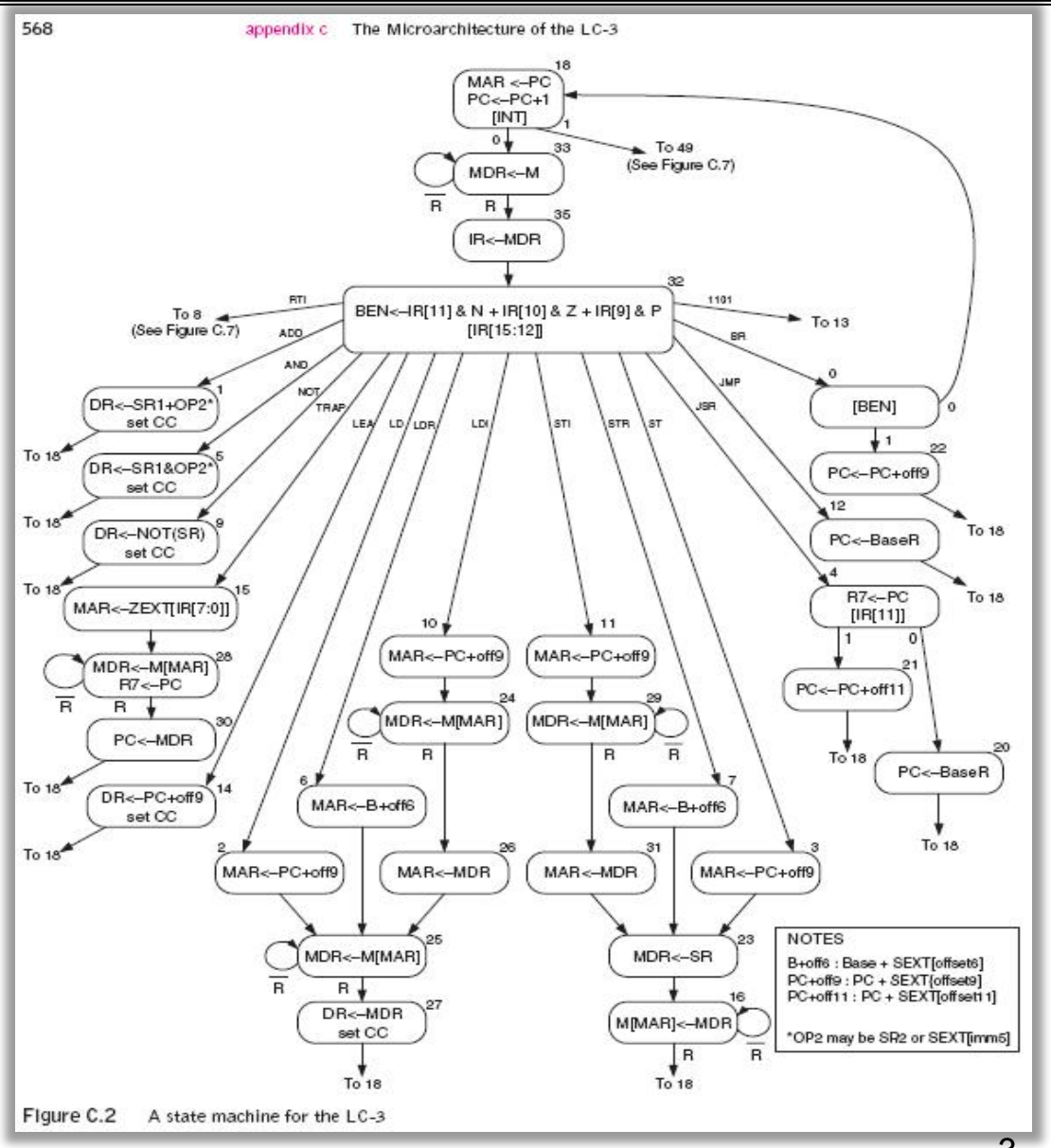


Instruction Processing: State Transtion

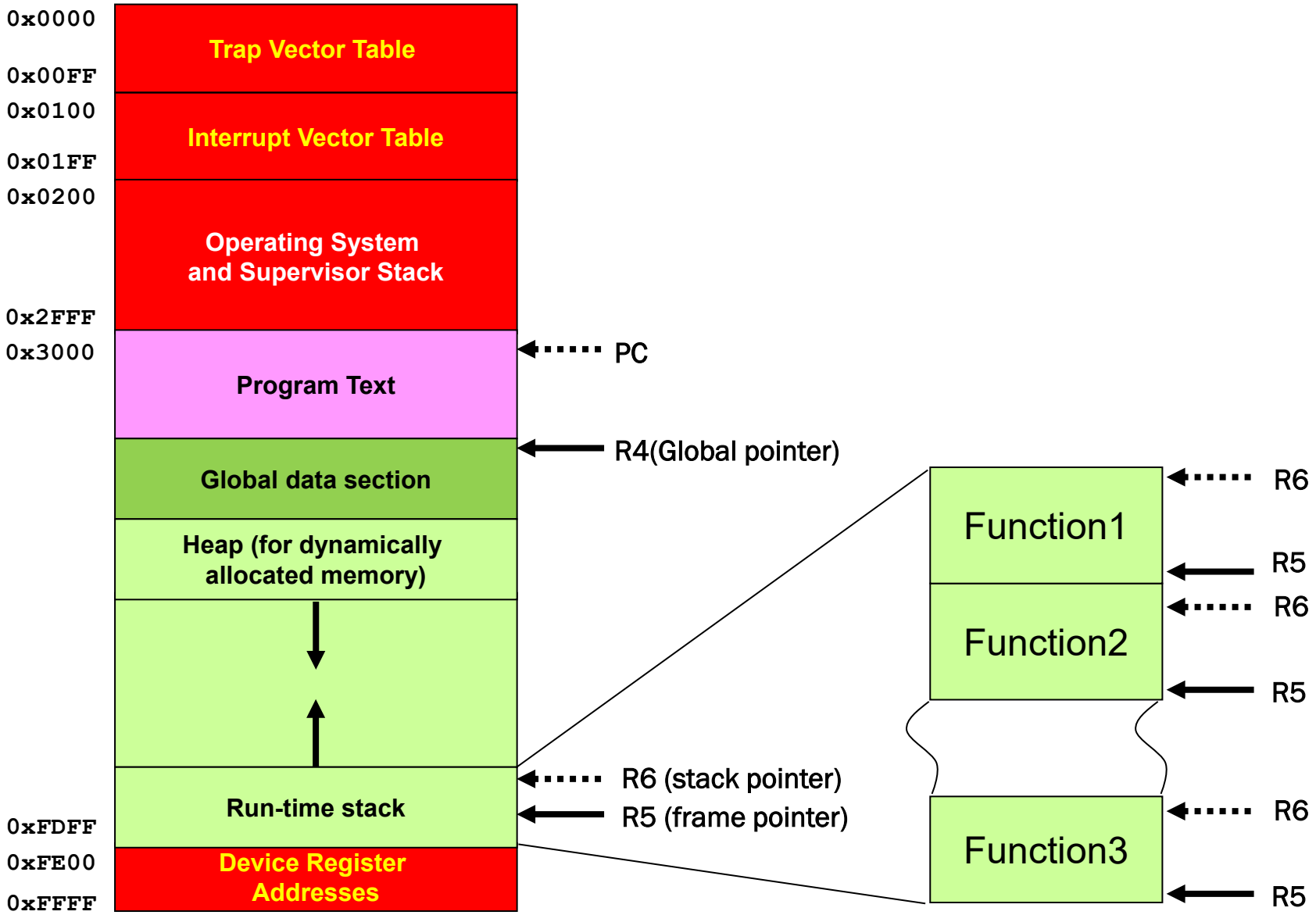


Instruction Processing: Finite State Automata





LC-3 Overview: Memory Map



LC-3 ISA Overview

运算指令(Operate Instructions)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADD	0	0	0	1	DR			SR1			0	0	0	SR2		
ADD	0	0	0	1	DR			SR1			1	Imm5				
AND	0	1	0	1	DR			SR1			0	0	0	SR2		
AND	0	1	0	1	DR			SR1			1	Imm5				
NOT	1	0	0	1	DR			SR1			1	1	1	1	1	1
Reserved	1	1	0	1												

控制指令(Control Instructions)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BR	0	0	0	0	n	z	p	PCoffset9								
JSR	0	1	0	0	1	PCoffset11										
JSRR	0	1	0	0	0	0	0	BaseR			0	0	0	0	0	0
RTI	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
JMP	1	1	0	0	0	0	0	BaseR			0	0	0	0	0	0
RET	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0	0
TRAP	1	1	1	1	0	0	0	0	TrapVector8							

数据移动指令 (Data Movement Instructions)

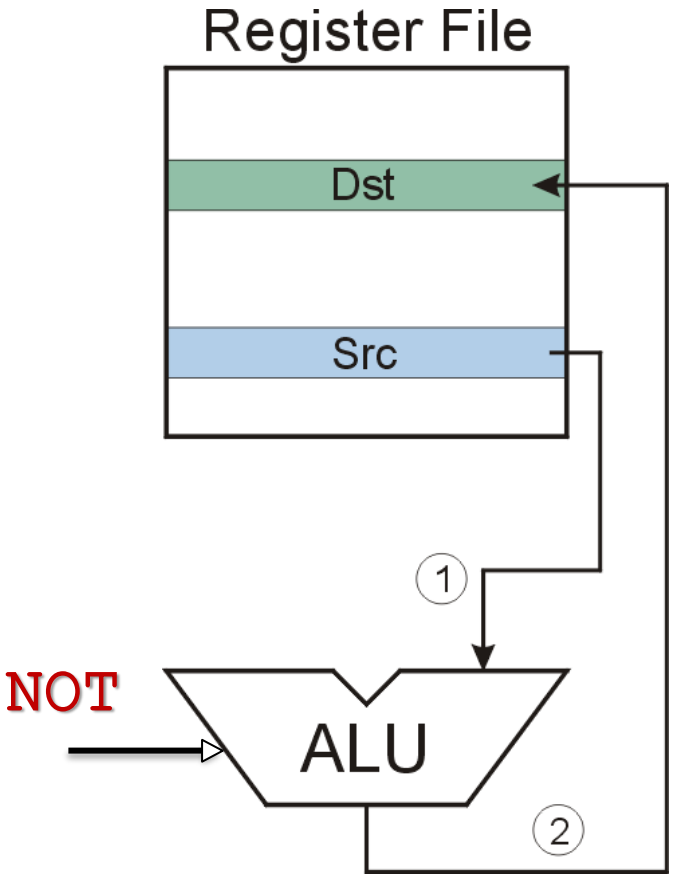
取数指令(Load)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LD	0	0	1	0	DR			PCoffset9								
LDR	0	1	1	0	DR			BaseR			PCoffset6					
LDI	1	0	1	0	DR			PCoffset9								
LEA	1	1	1	0	DR			PCoffset9								

存数指令(Store)

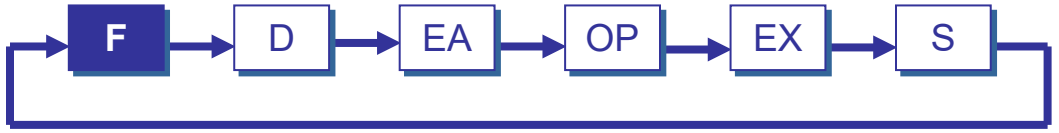
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ST	0	0	1	1	SR			PCoffset9								
STR	0	1	1	1	SR			BaseR			PCoffset6					
STI	1	0	1	1	SR			PCoffset9								

NOT (Register)



Note: Src and Dst could be the same register.

NOT (Register):



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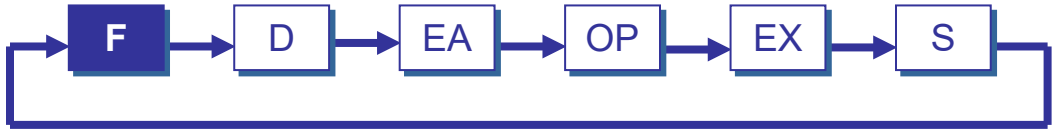

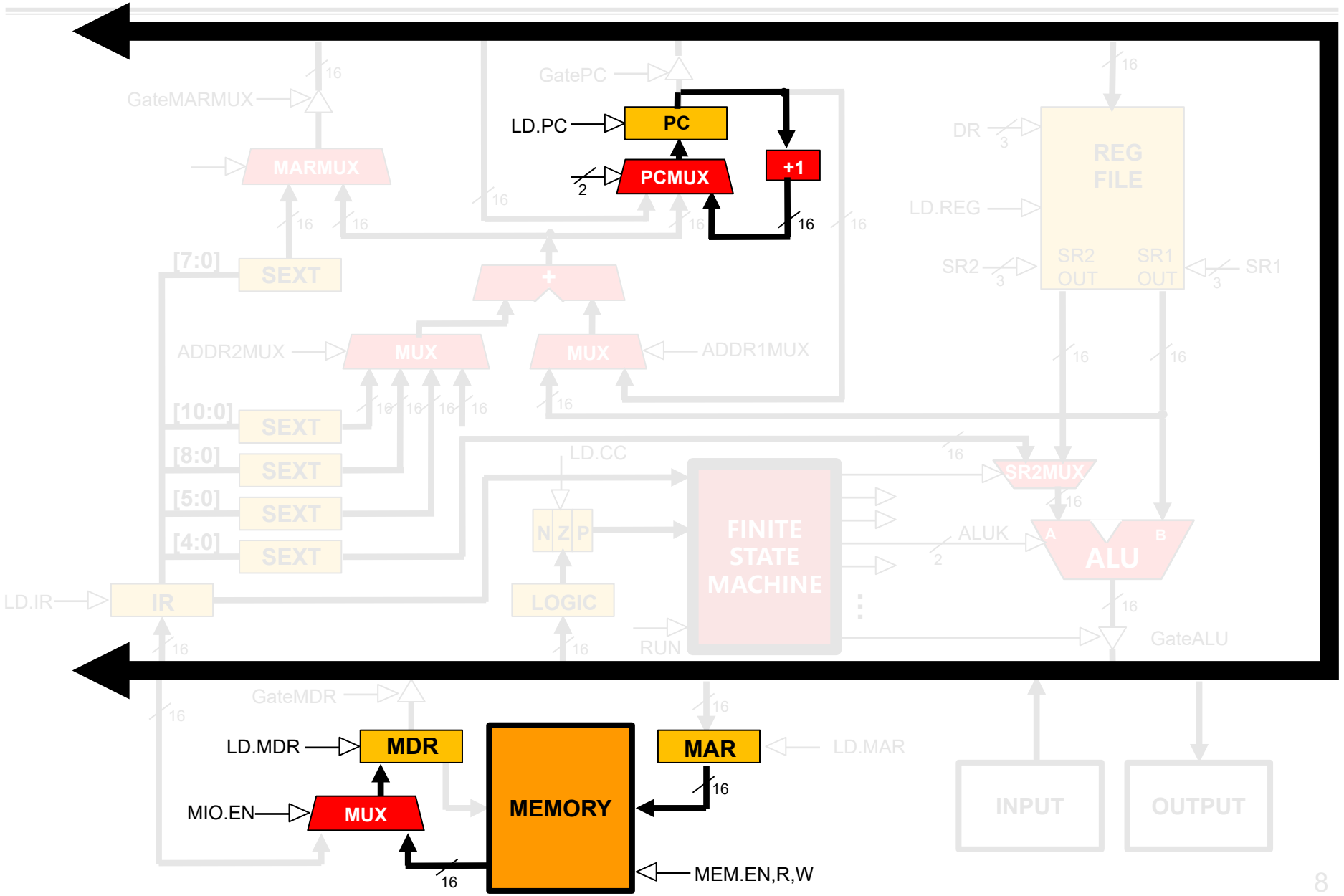

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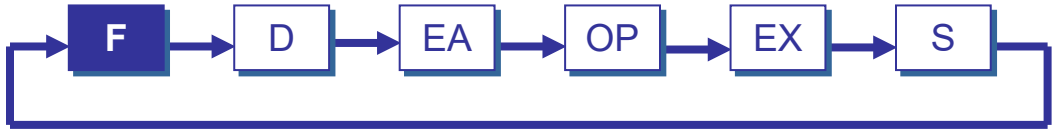
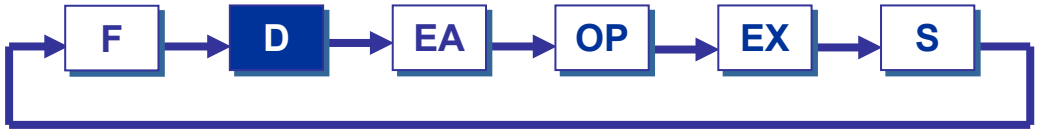
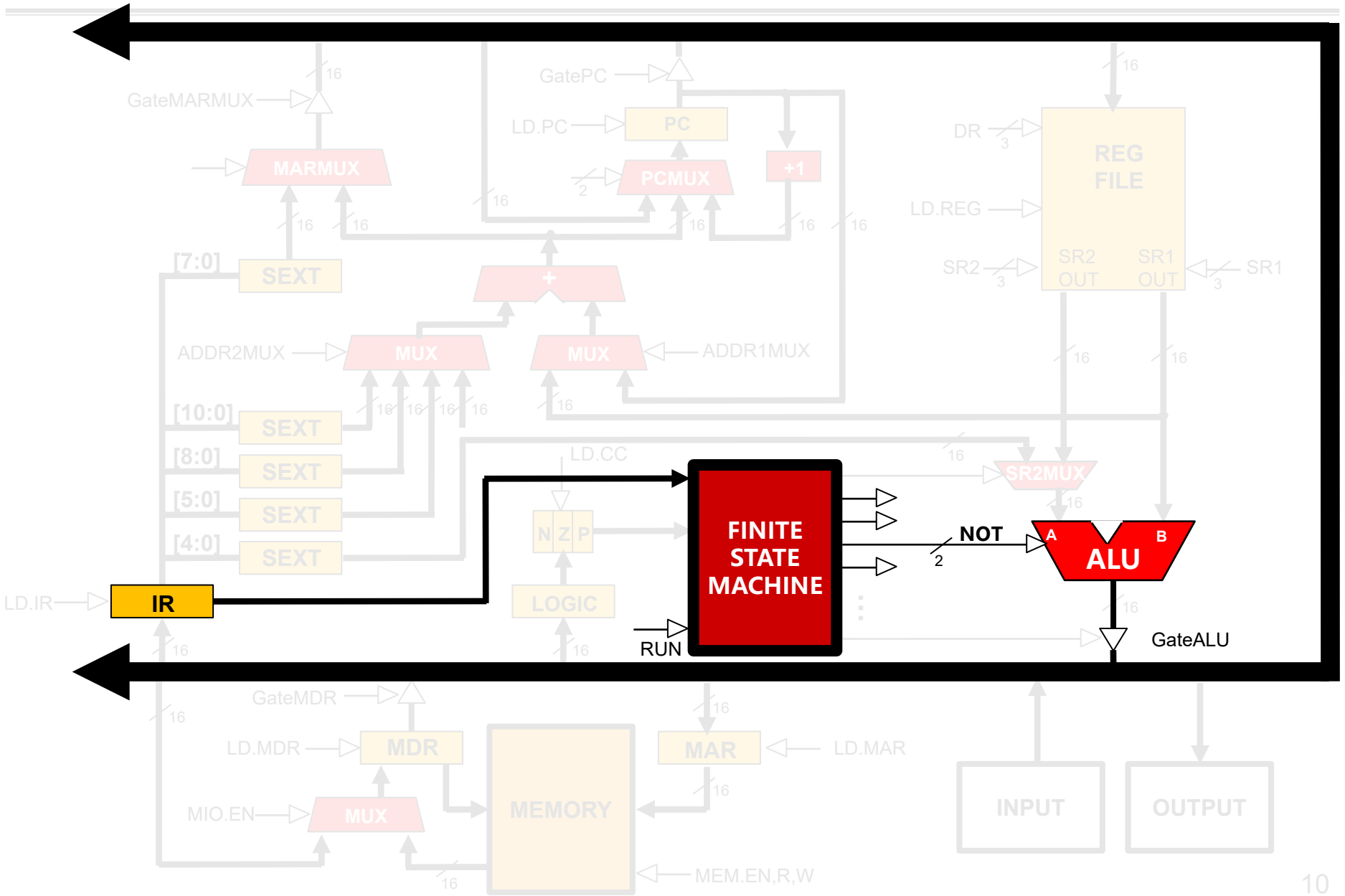


NOT (Register):





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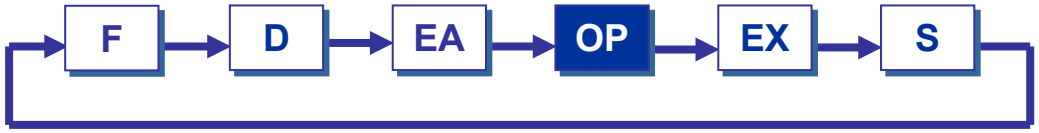

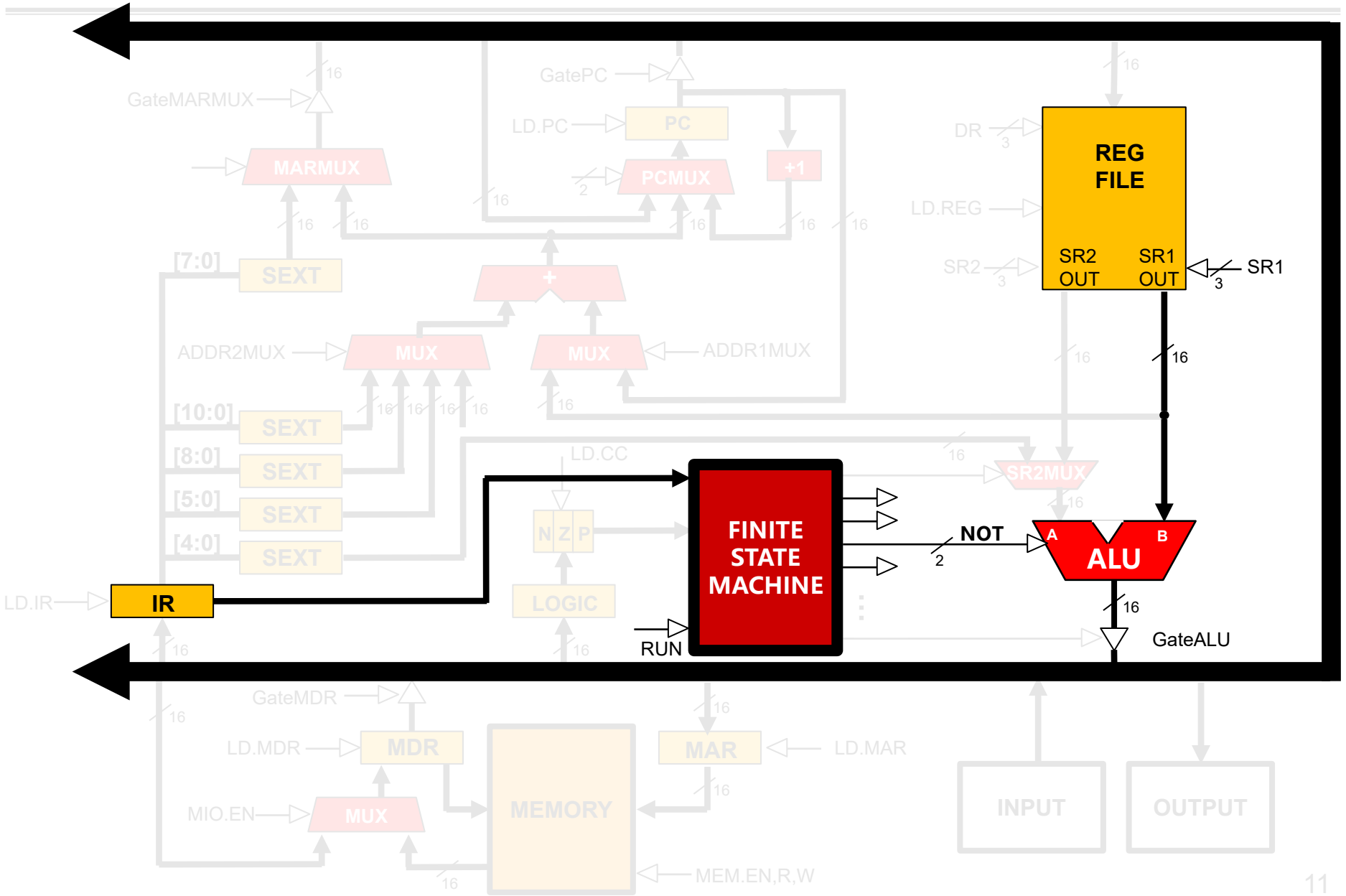

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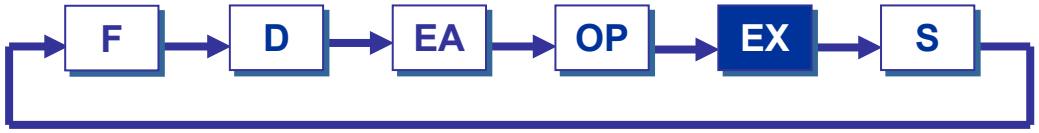

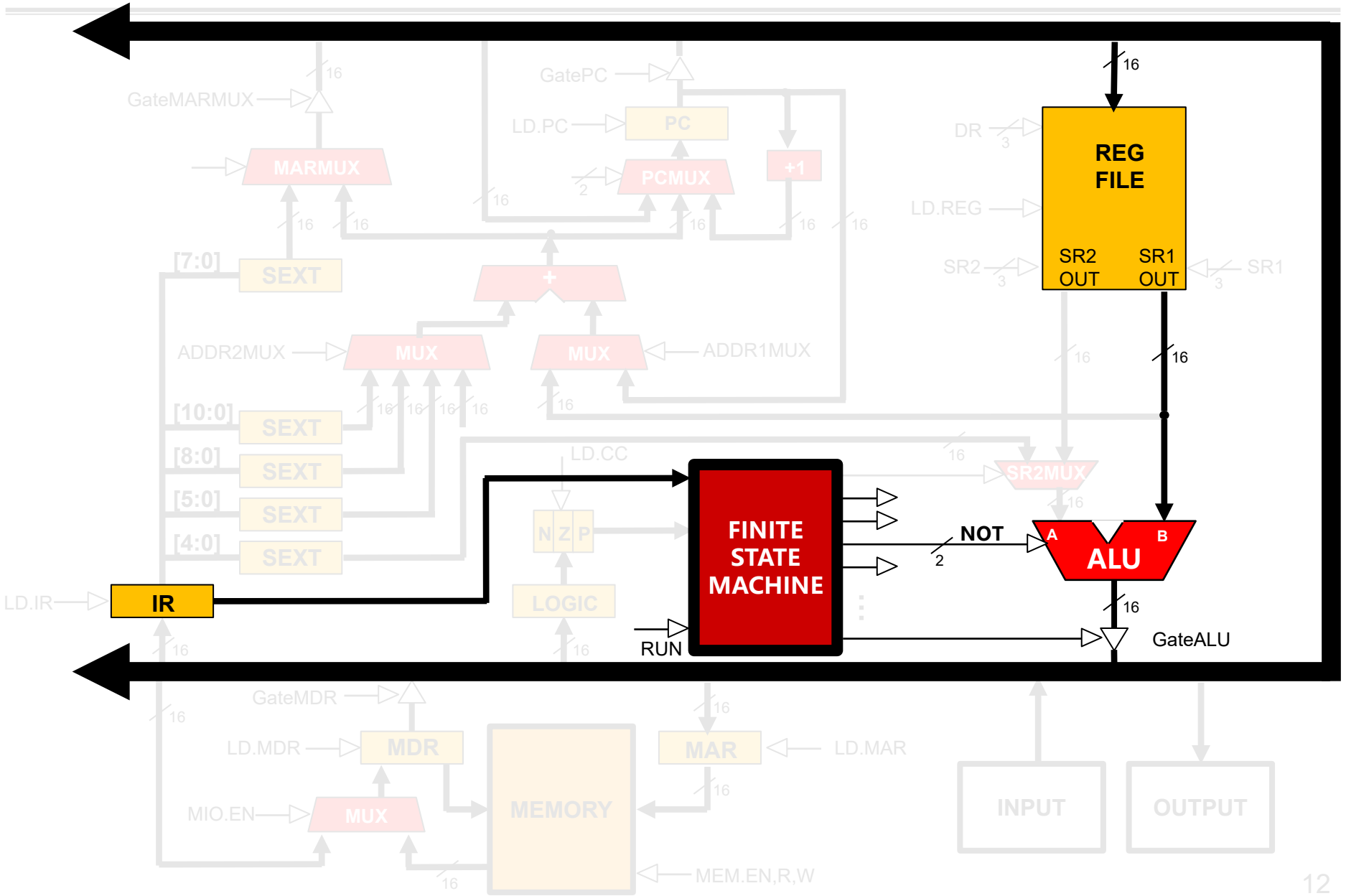

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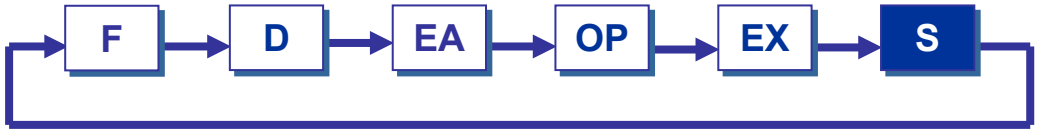
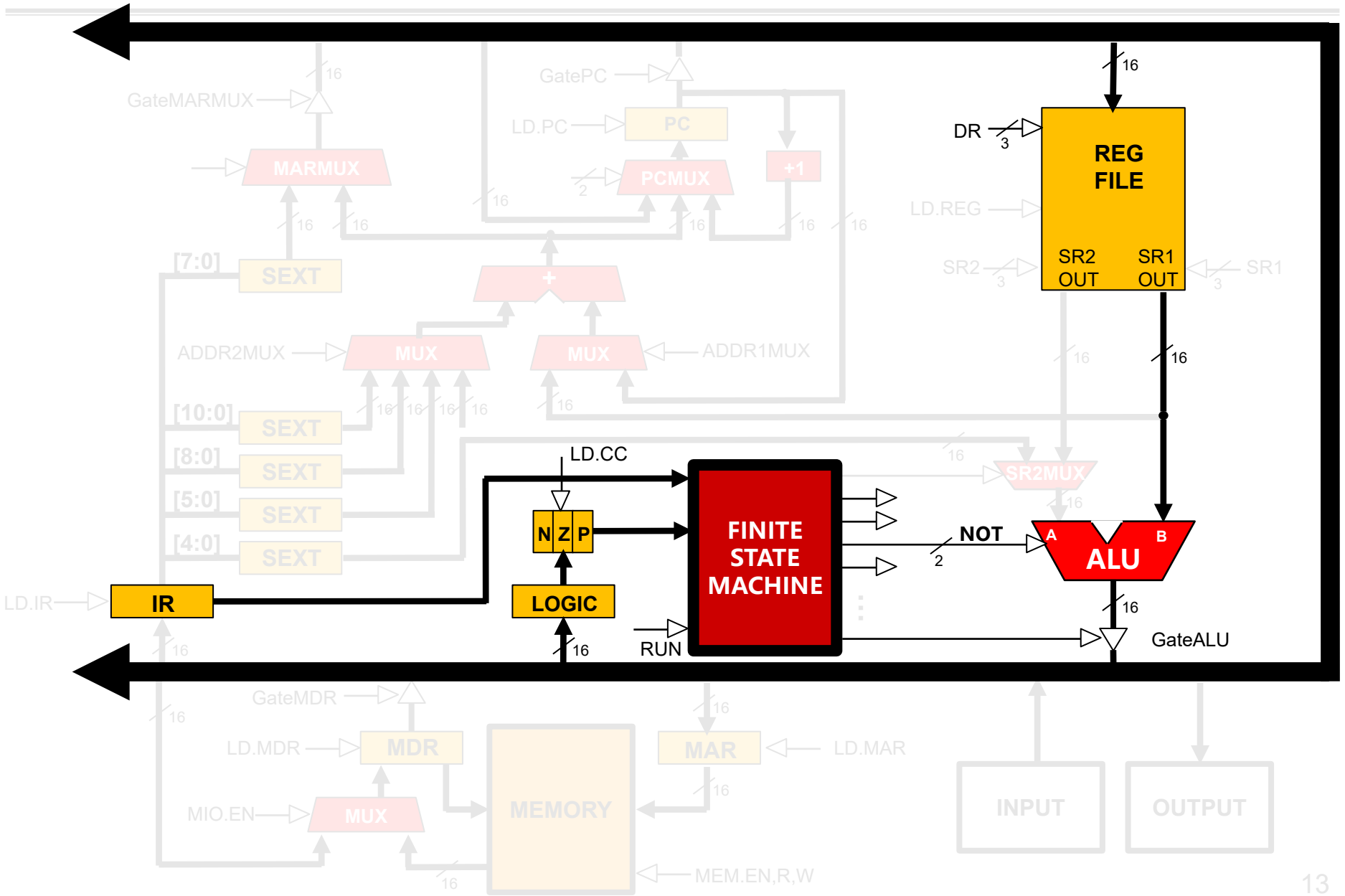
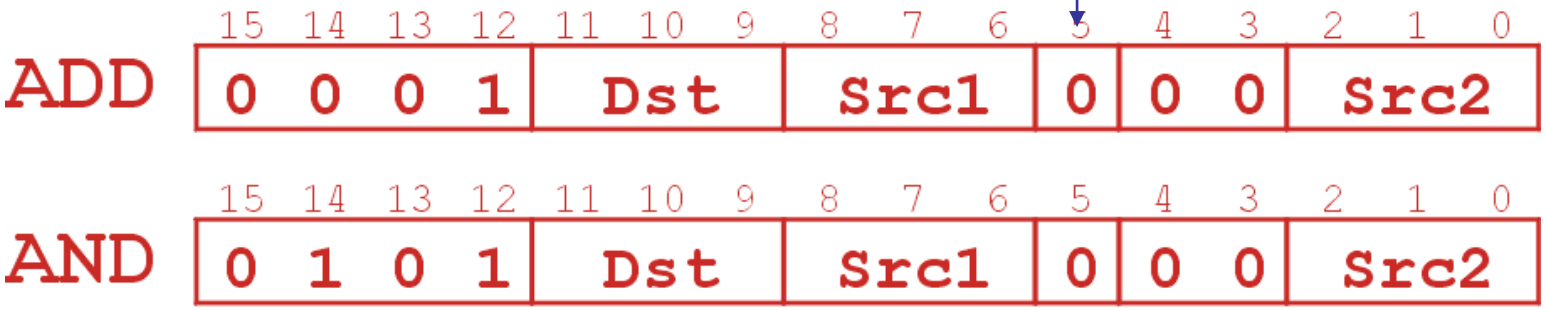
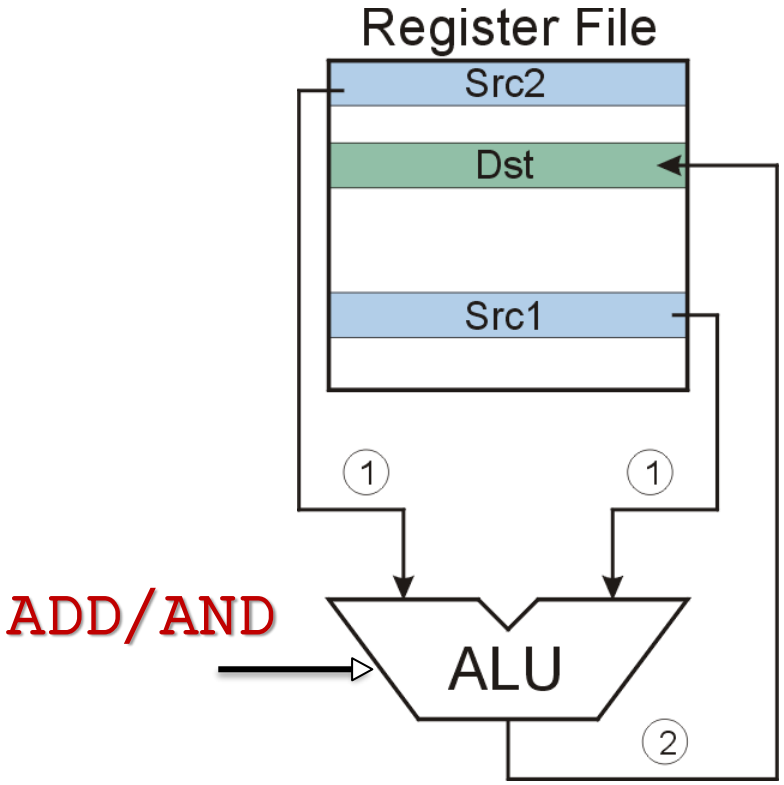




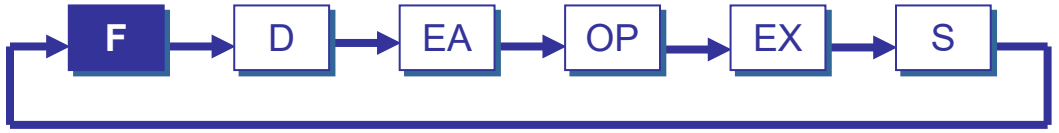
ADD/AND (Register)

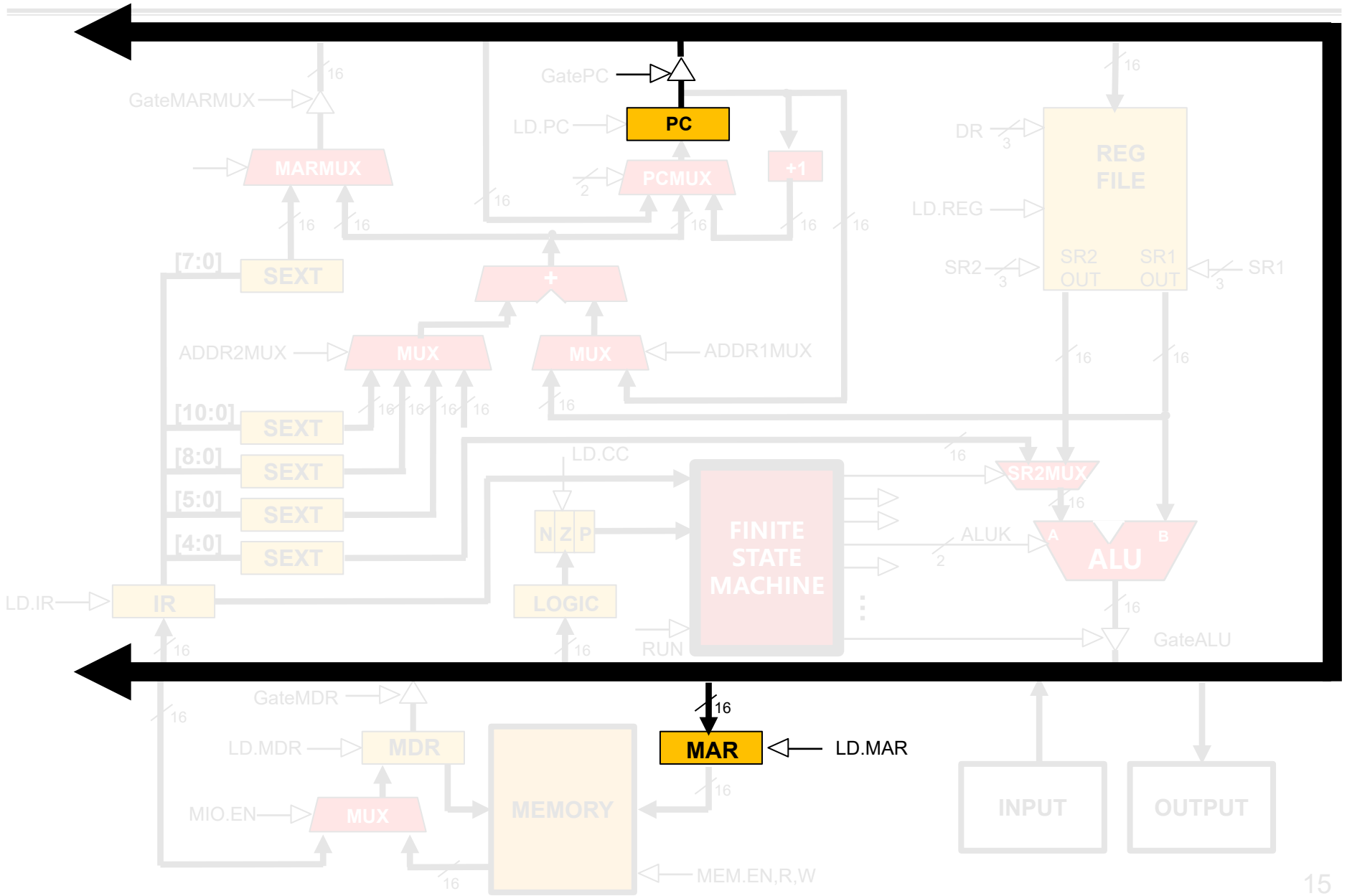
this zero means "register mode"



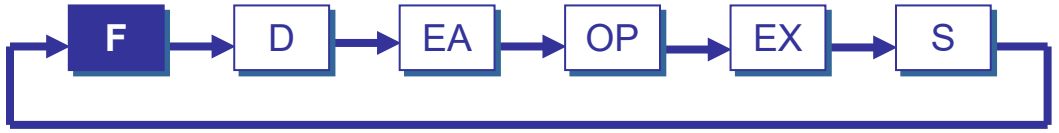


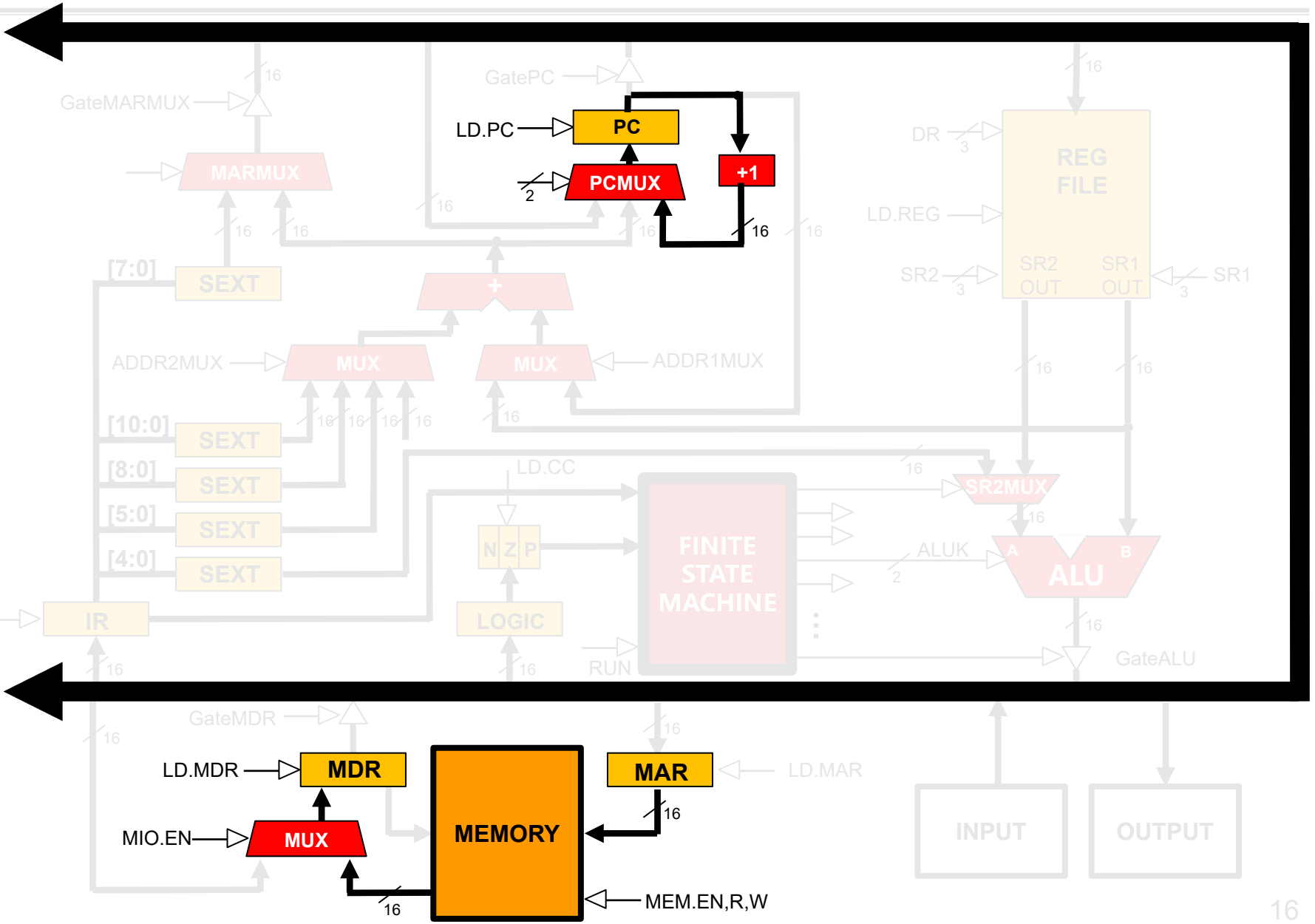
ADD/AND (Register)



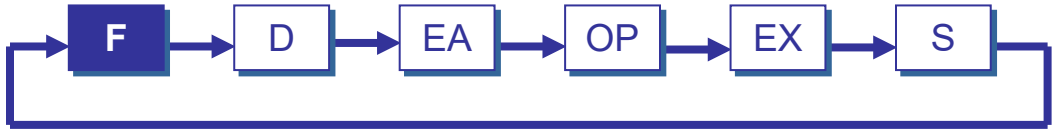


ADD/AND (Register)

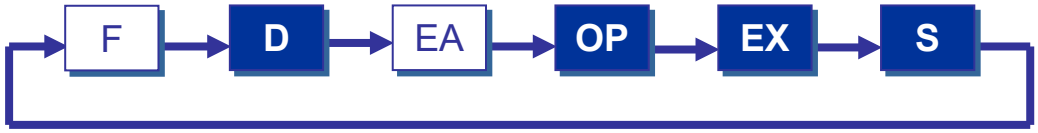


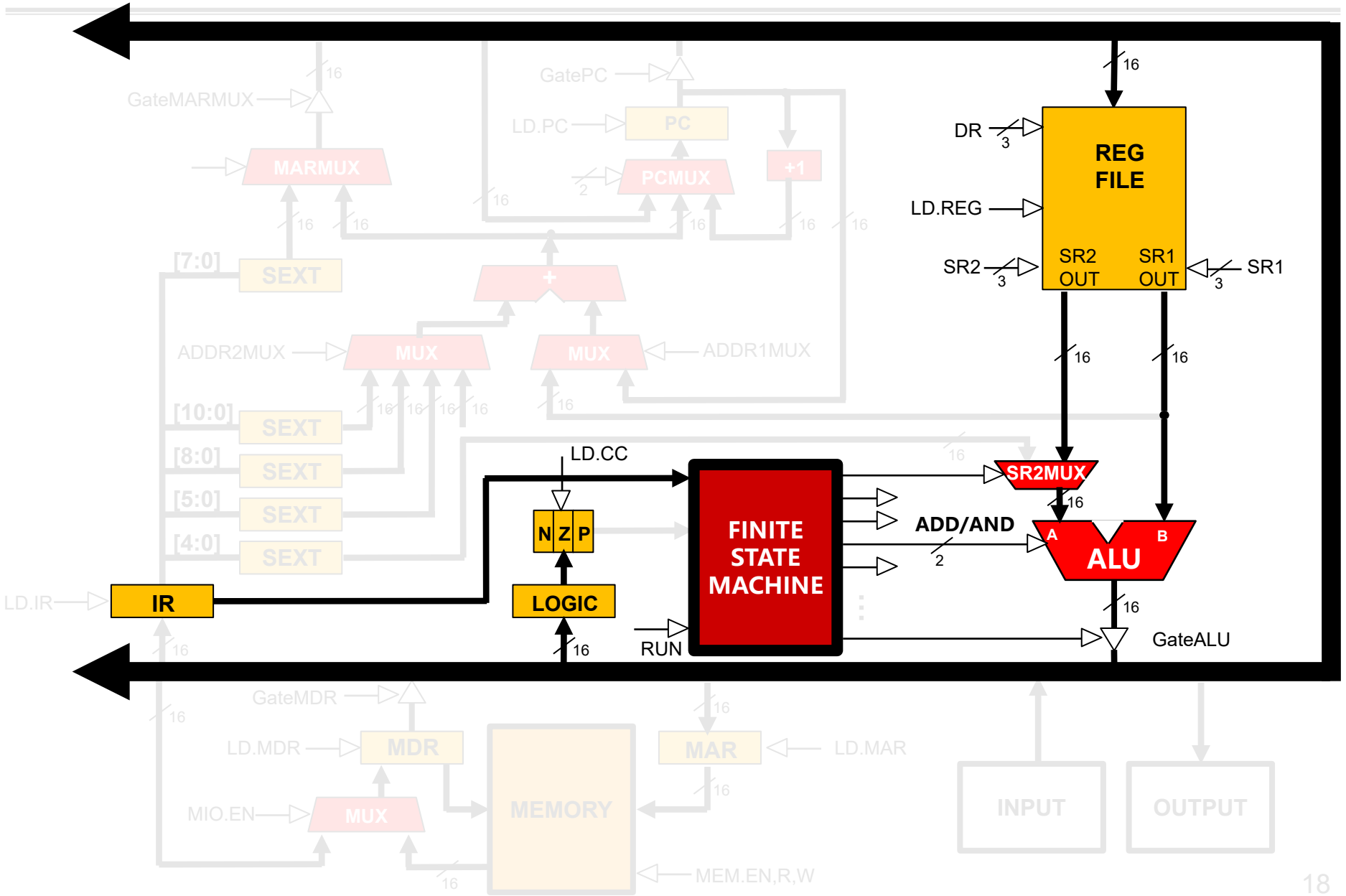


ADD/AND (Register)



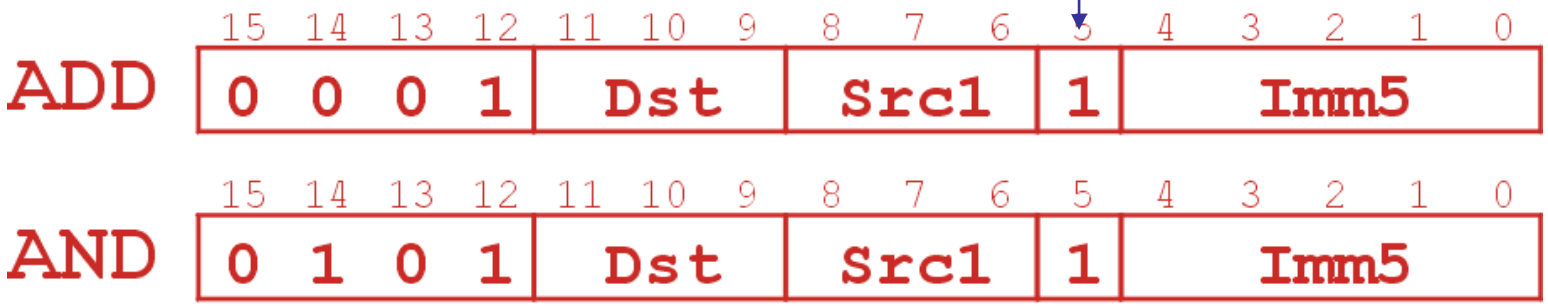
ADD/AND (Register)



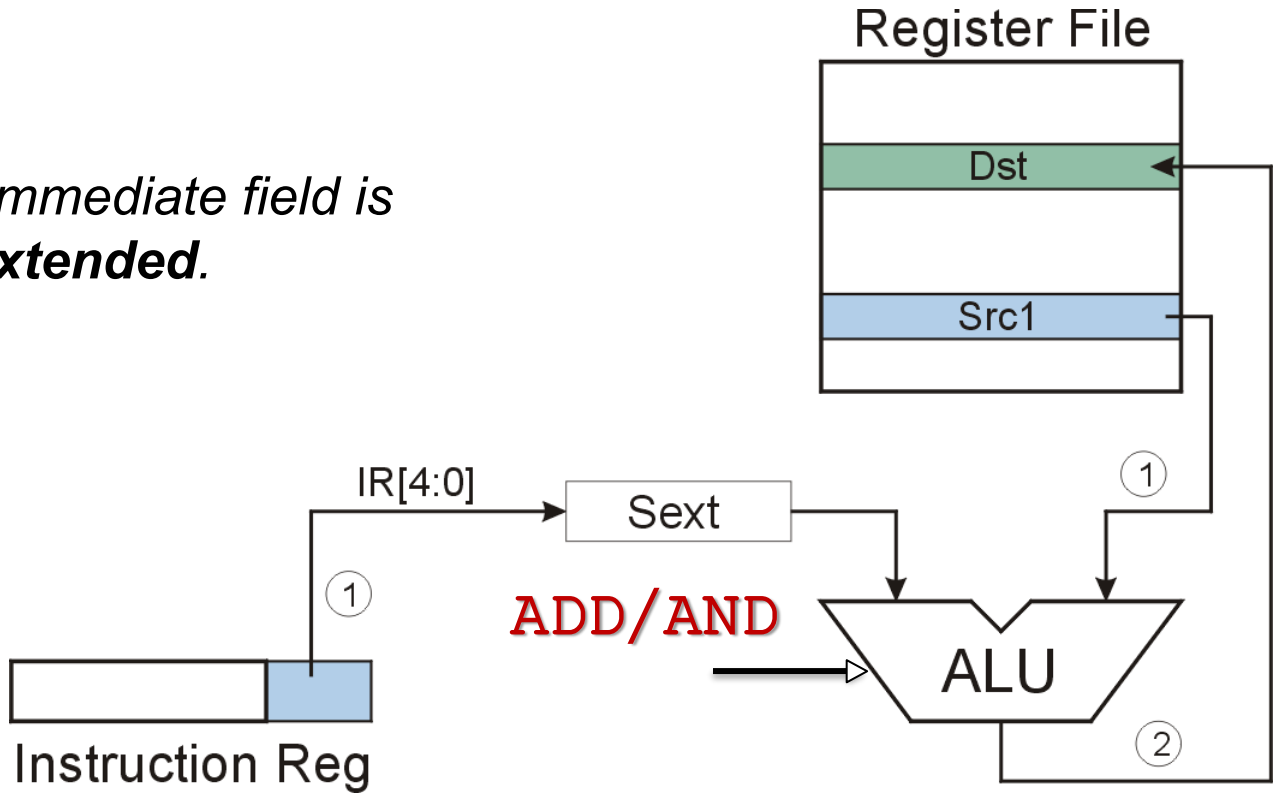


ADD/AND (Immediate)

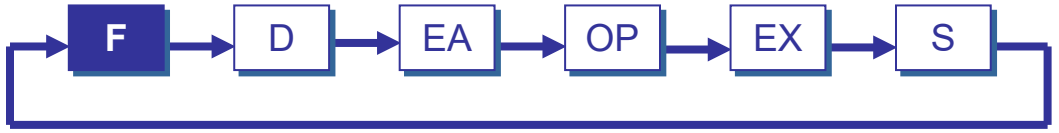
this one means "immediate mode"

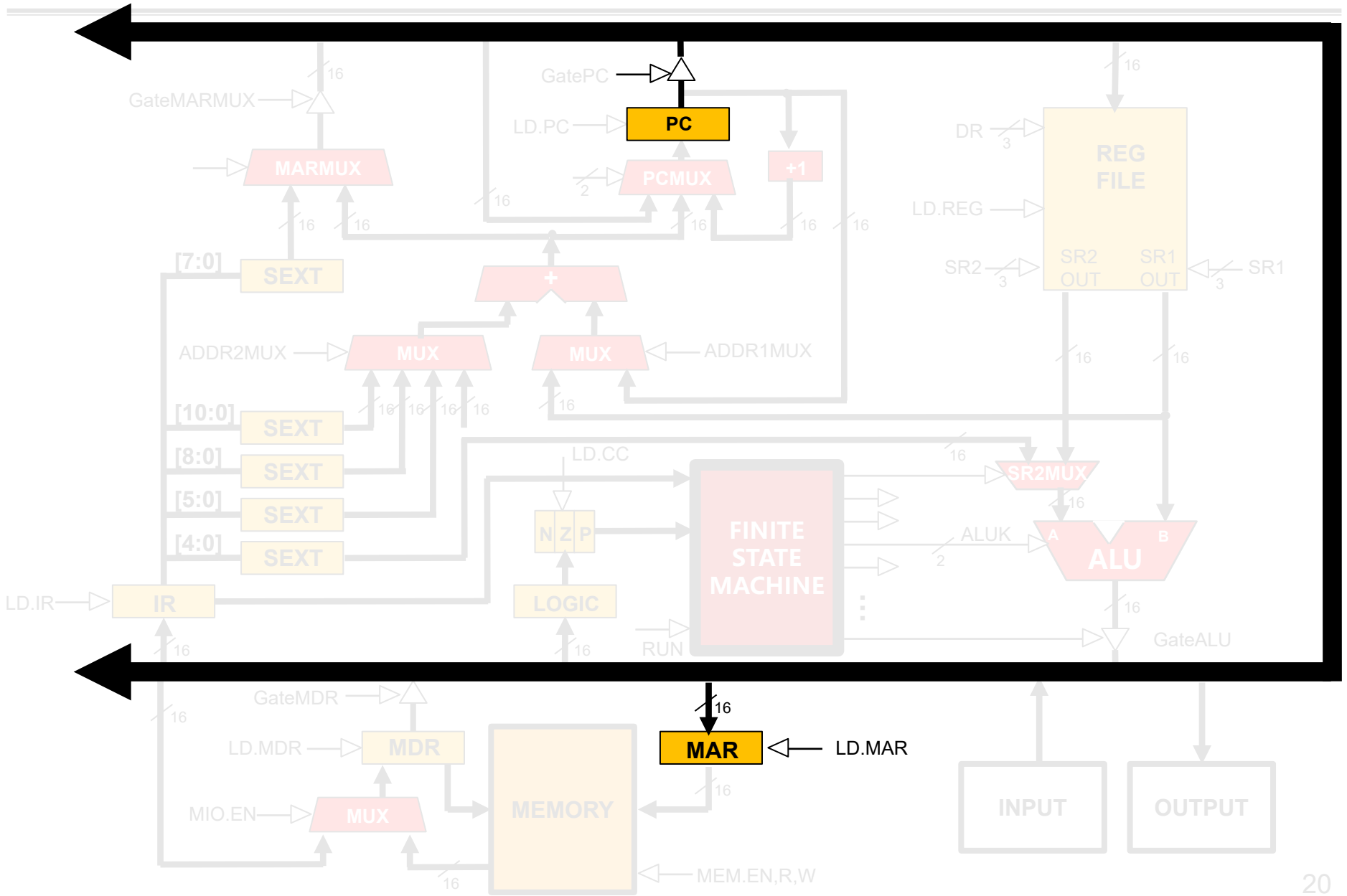


Note: Immediate field is ***sign-extended****.*

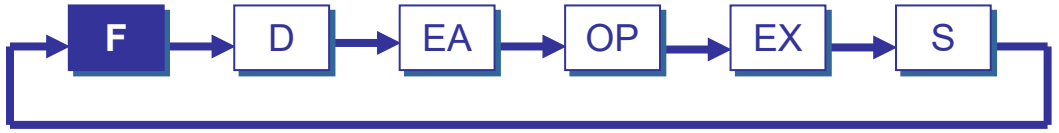


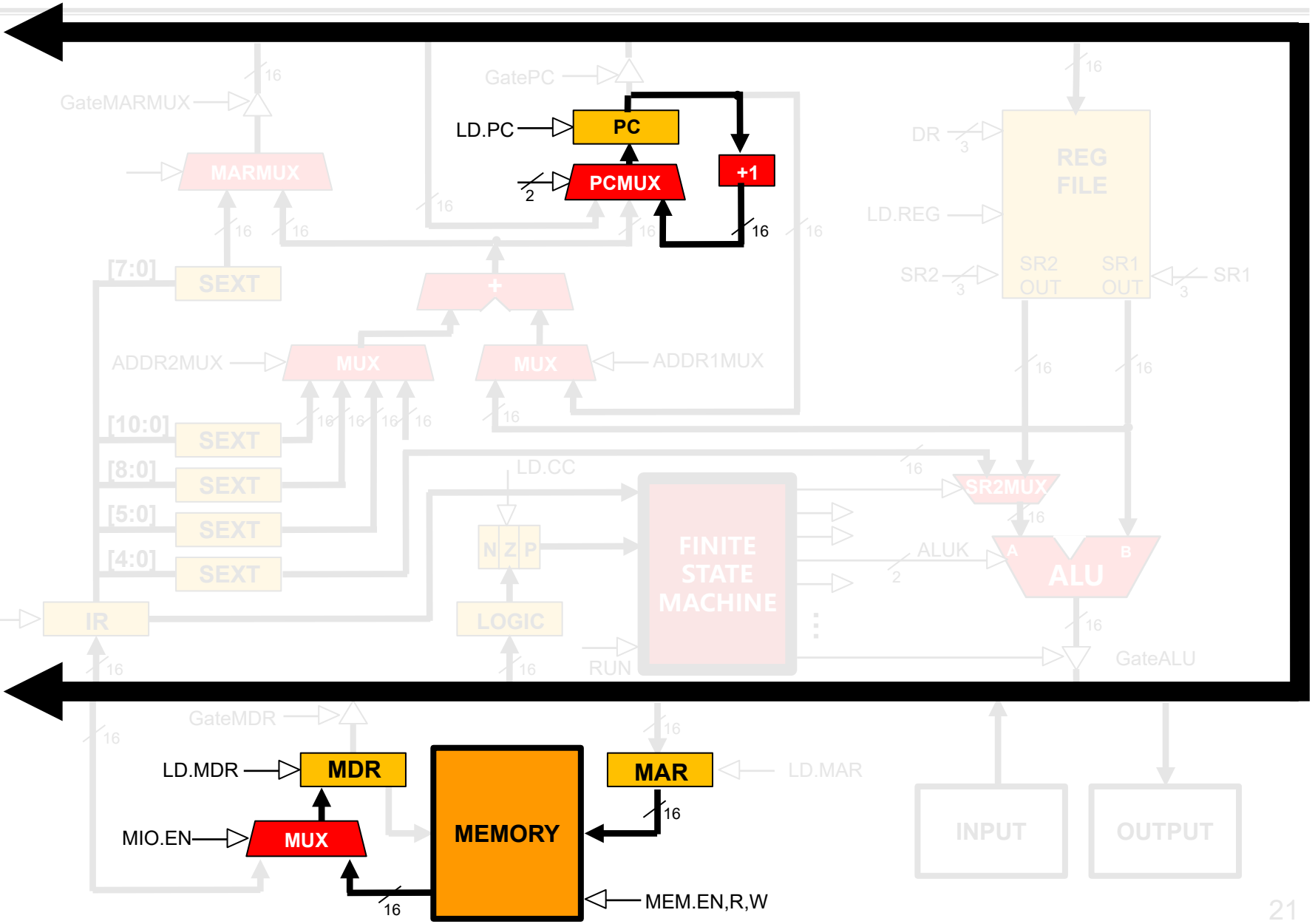
ADD/AND (Immediate)



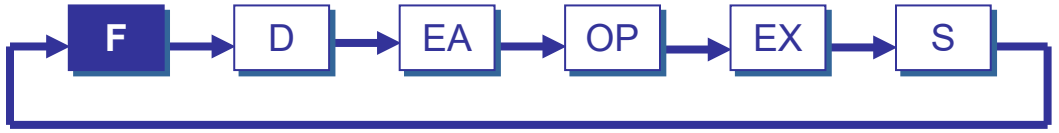


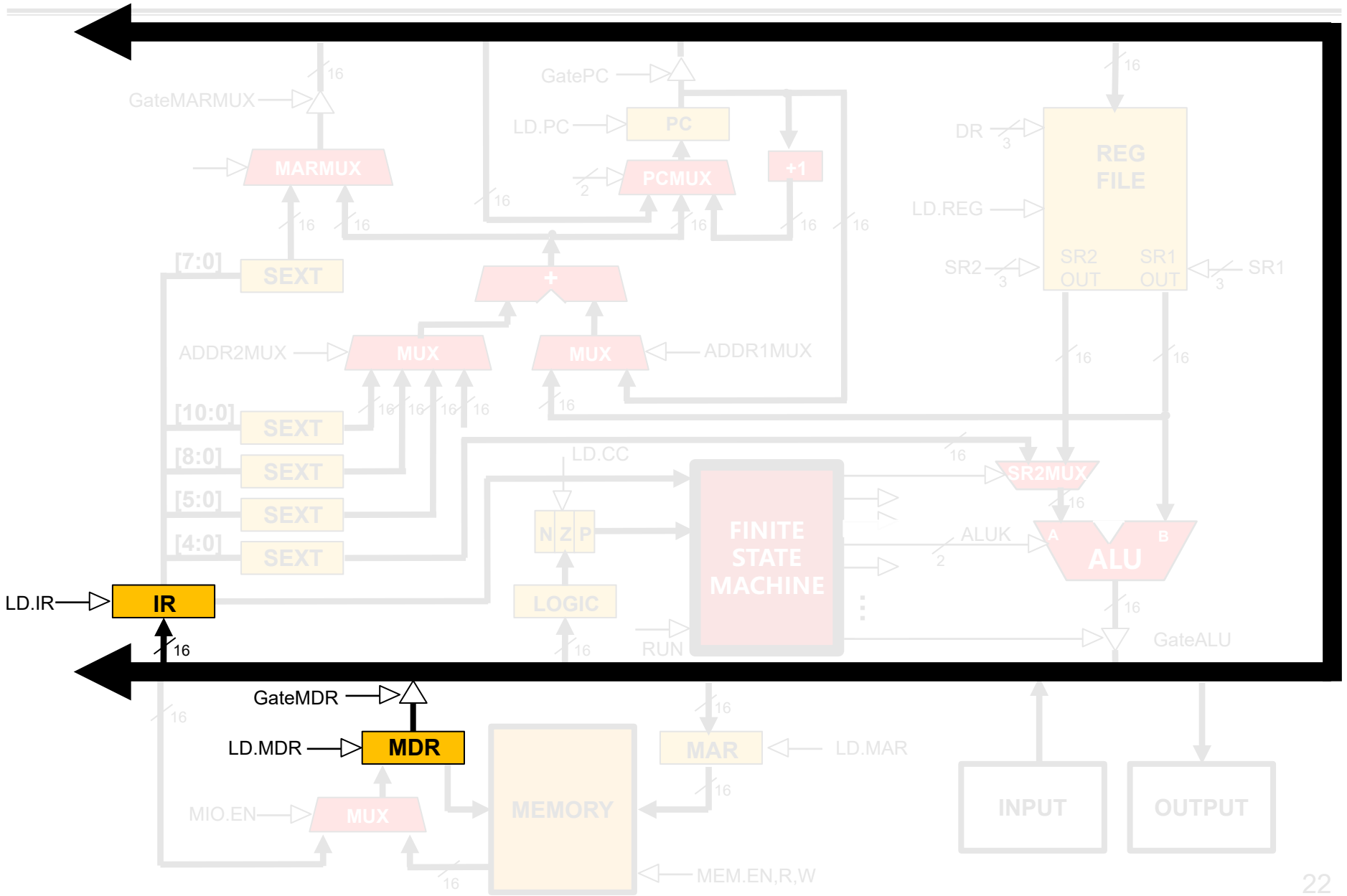
ADD/AND (Immediate)





ADD/AND (Immediate)





ADD/AND (Immediate)