Data Movement Instructions

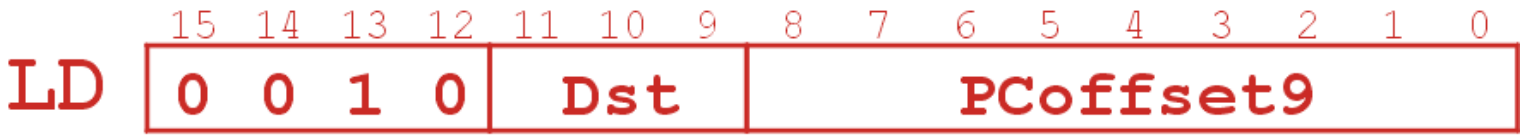
取数指令

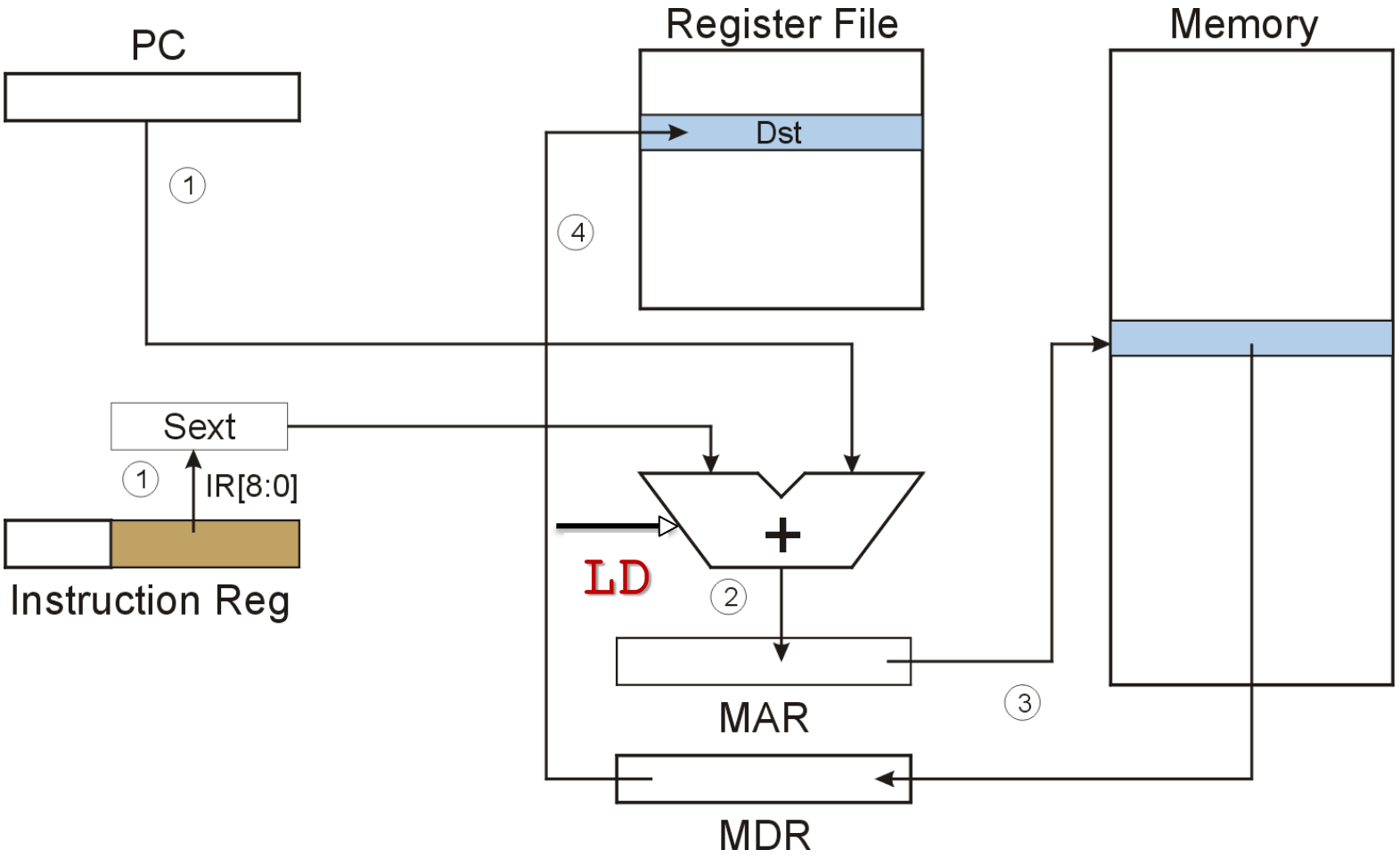
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LD	0	0	1	0	DR			PCoffset9								
LDR	0	1	1	0	DR			BaseR			PCoffset6					
LDI	1	0	1	0	DR			PCoffset9								
LEA	1	1	1	0	DR			PCoffset9								

存数指令

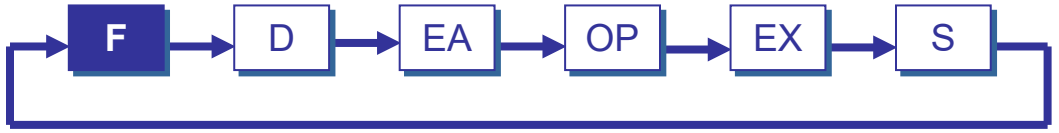
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ST	0	0	1	1	SR			PCoffset9								
STR	0	1	1	1	SR			BaseR			PCoffset6					
STI	1	0	1	1	SR			PCoffset9								

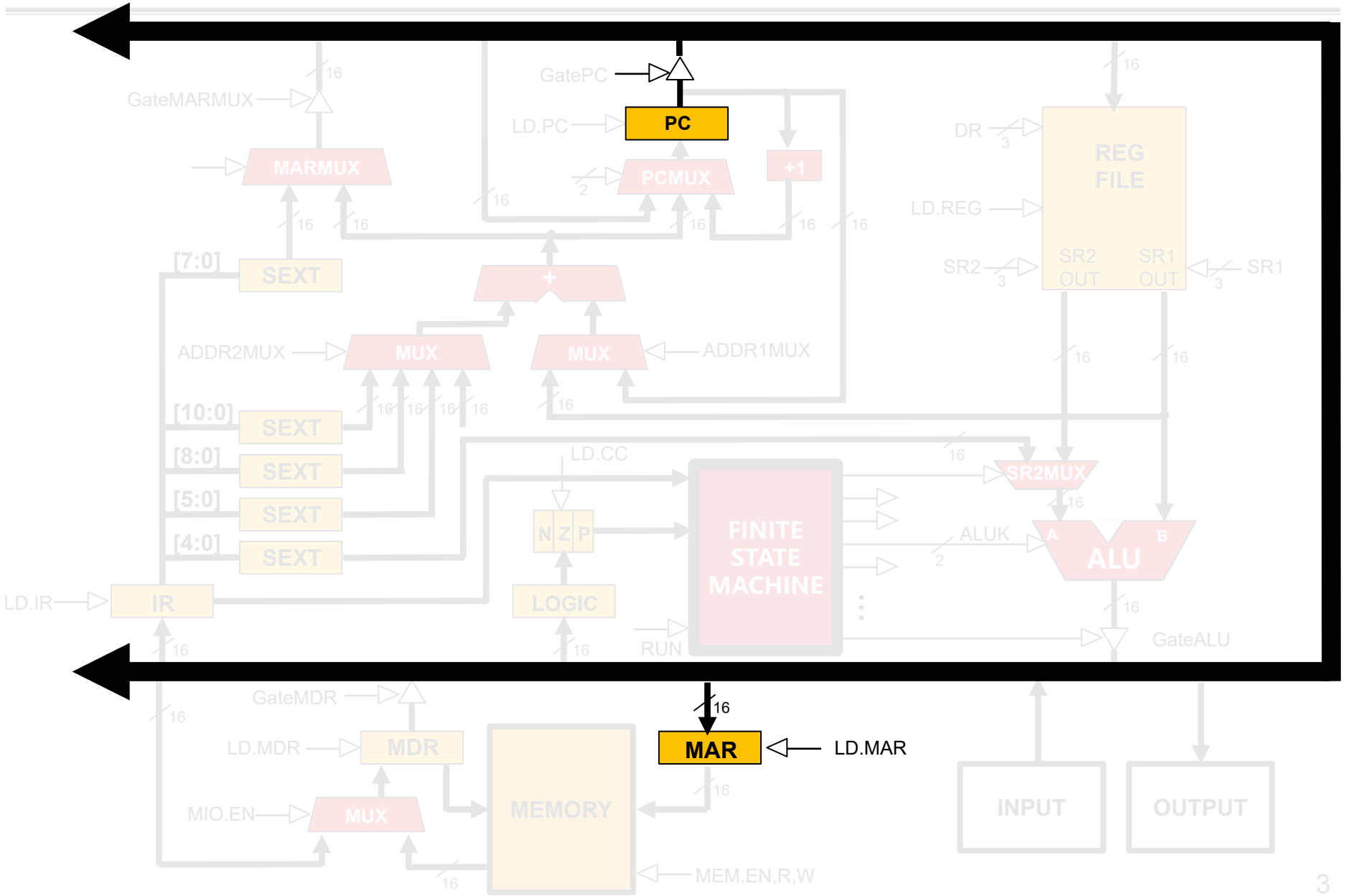
LD (PC-Relative) LD DR, PCoffset9



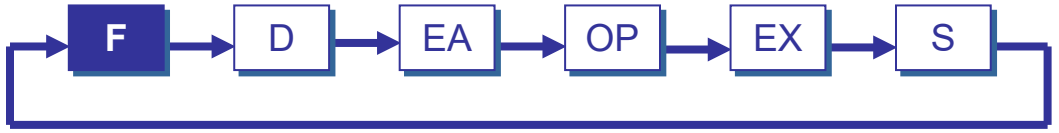


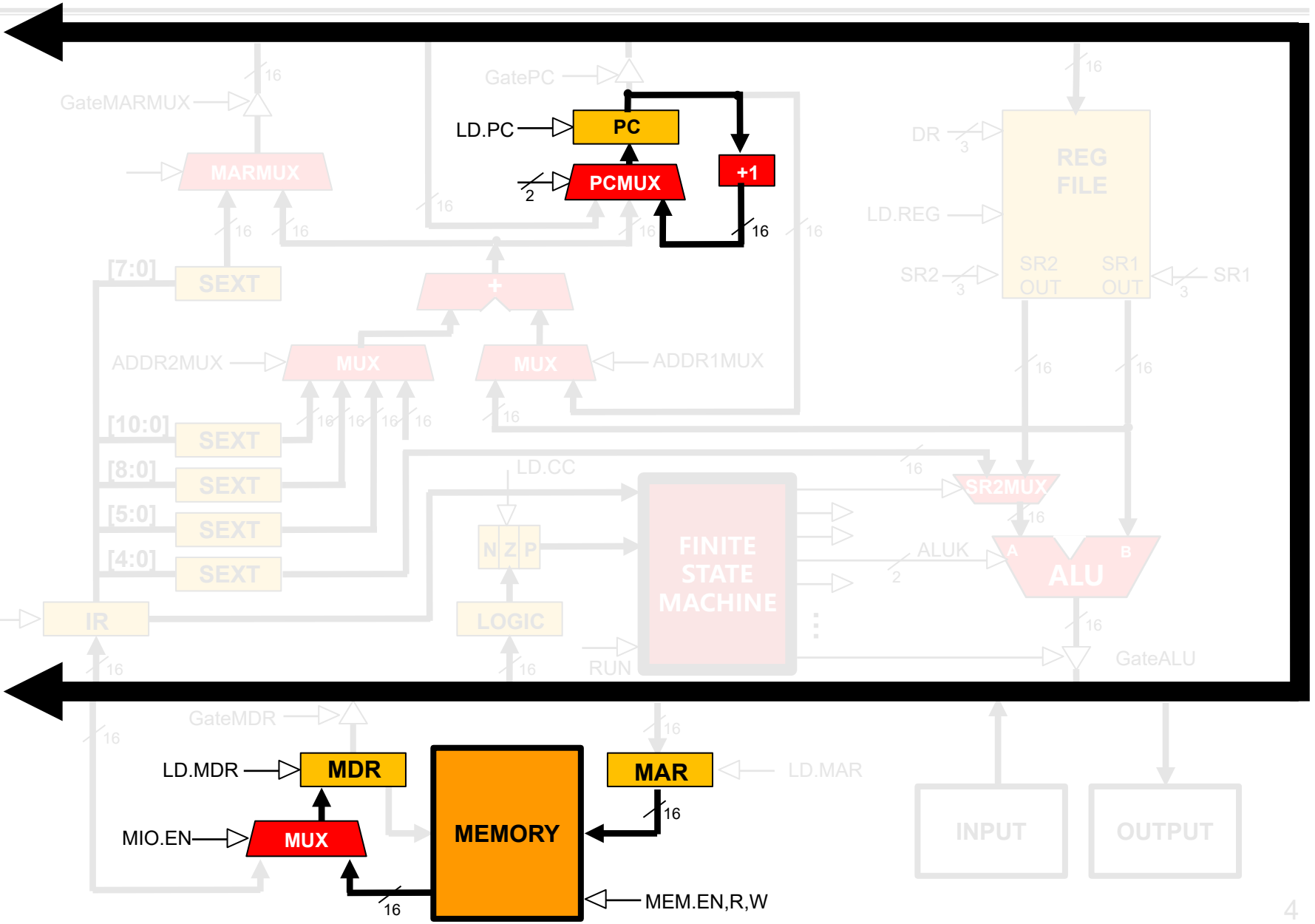
LD (PC-Relative)



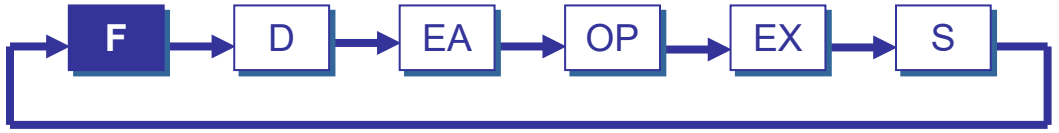


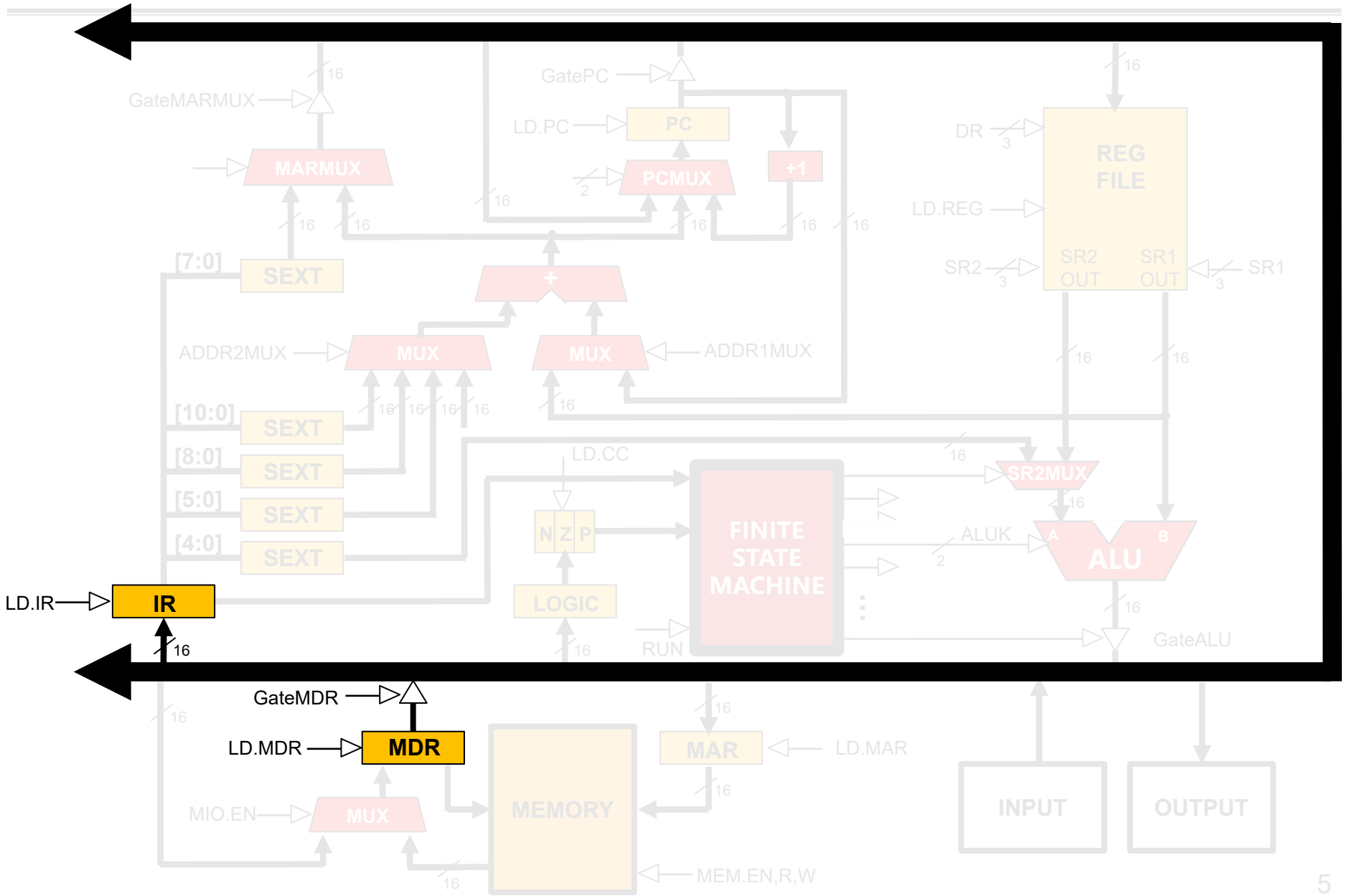
LD (PC-Relative)



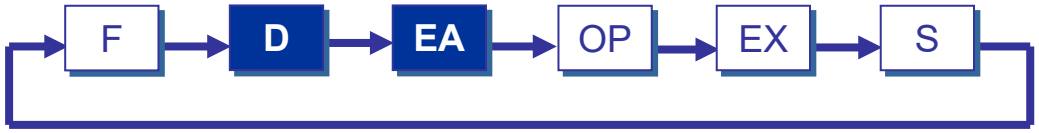


LD (PC-Relative)



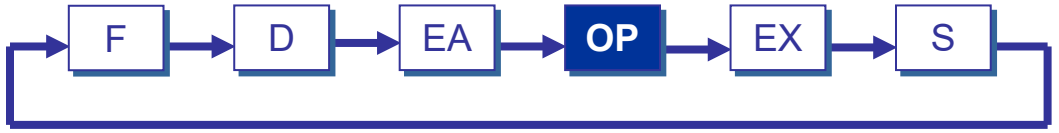


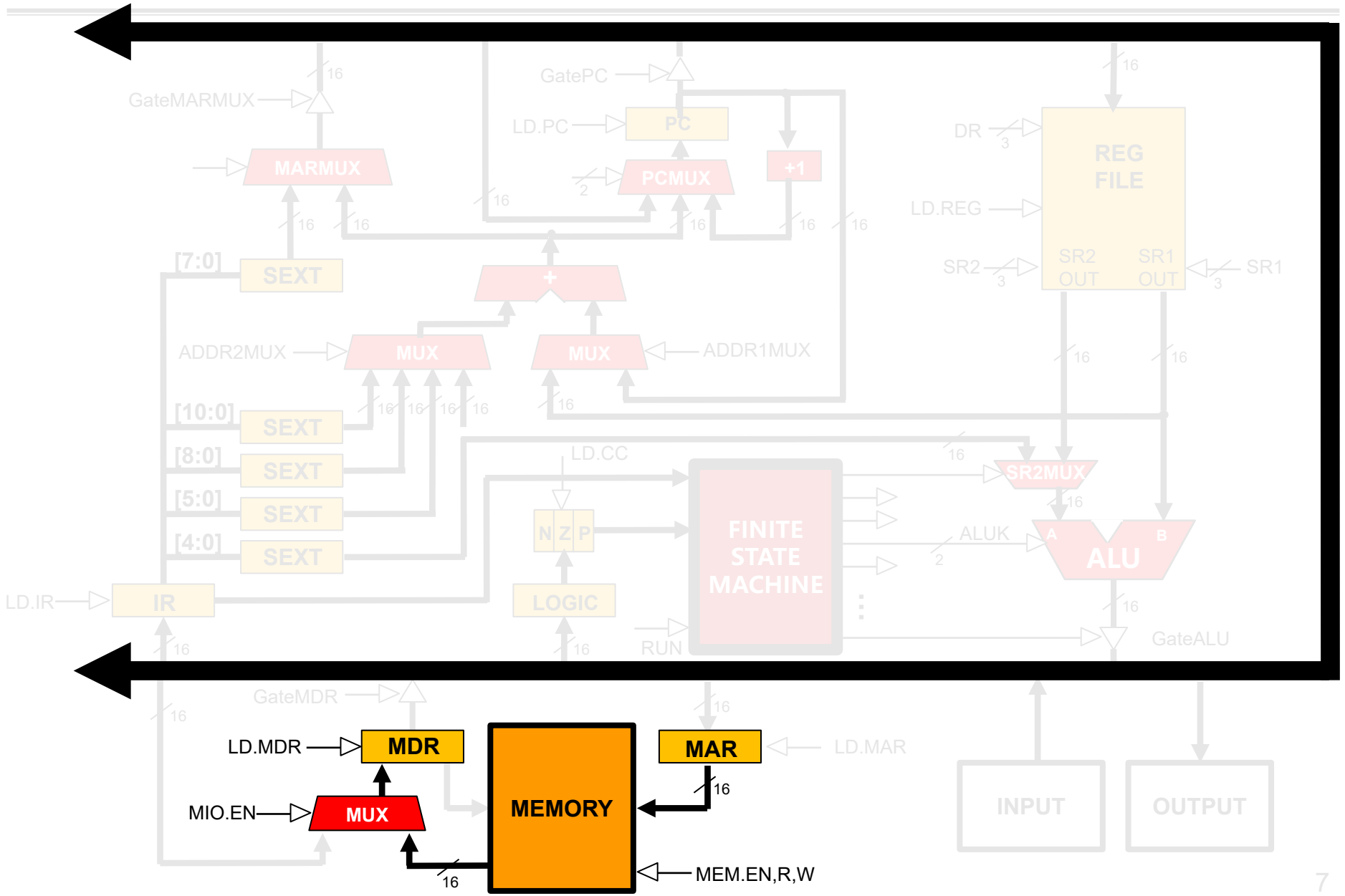
LD (PC-Relative)



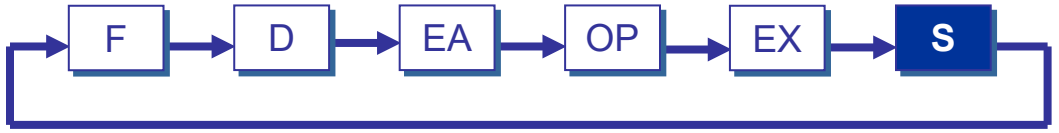
GateMARMUX
MARMUX
16
PC
LD.PC
GatePC
PCMUX
+1
+
ADDR2MUX
MUX
MUX
ADDR1MUX
[7:0]
SEXT
[10:0]
SEXT
[8:0]
SEXT
[5:0]
SEXT
[4:0]
SEXT
IR
LD.IR
LD.CC
N Z P
LOGIC
FINITE STATE MACHINE
RUN
REG FILE
DR
LD.REG
SR2
SR1
SR2 OUT
SR1 OUT
SR2MUX
ALUK
ALU
GateALU
MAR
LD.MAR
GateMDR
MDR
LD.MDR
MIO.EN
MUX
MEMORY
MEM.EN,R,W
INPUT
OUTPUT

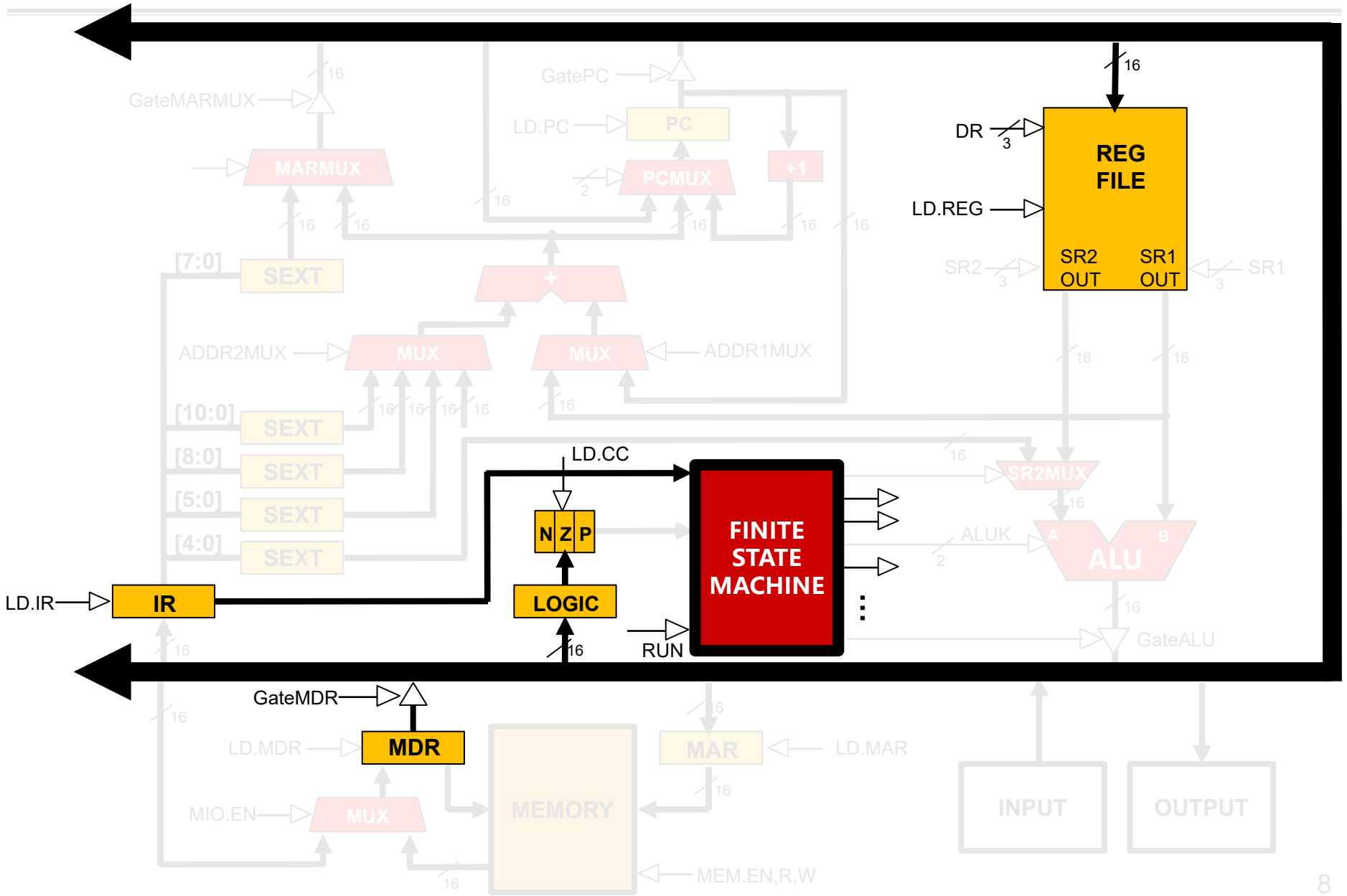
LD (PC-Relative)



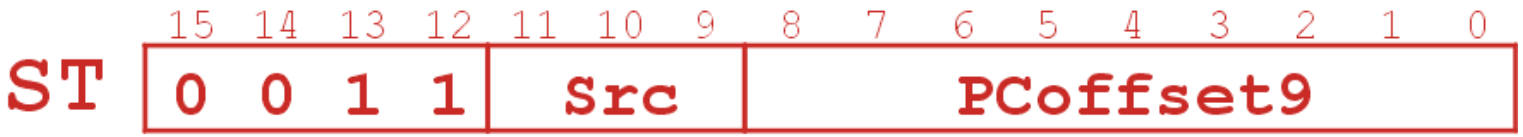


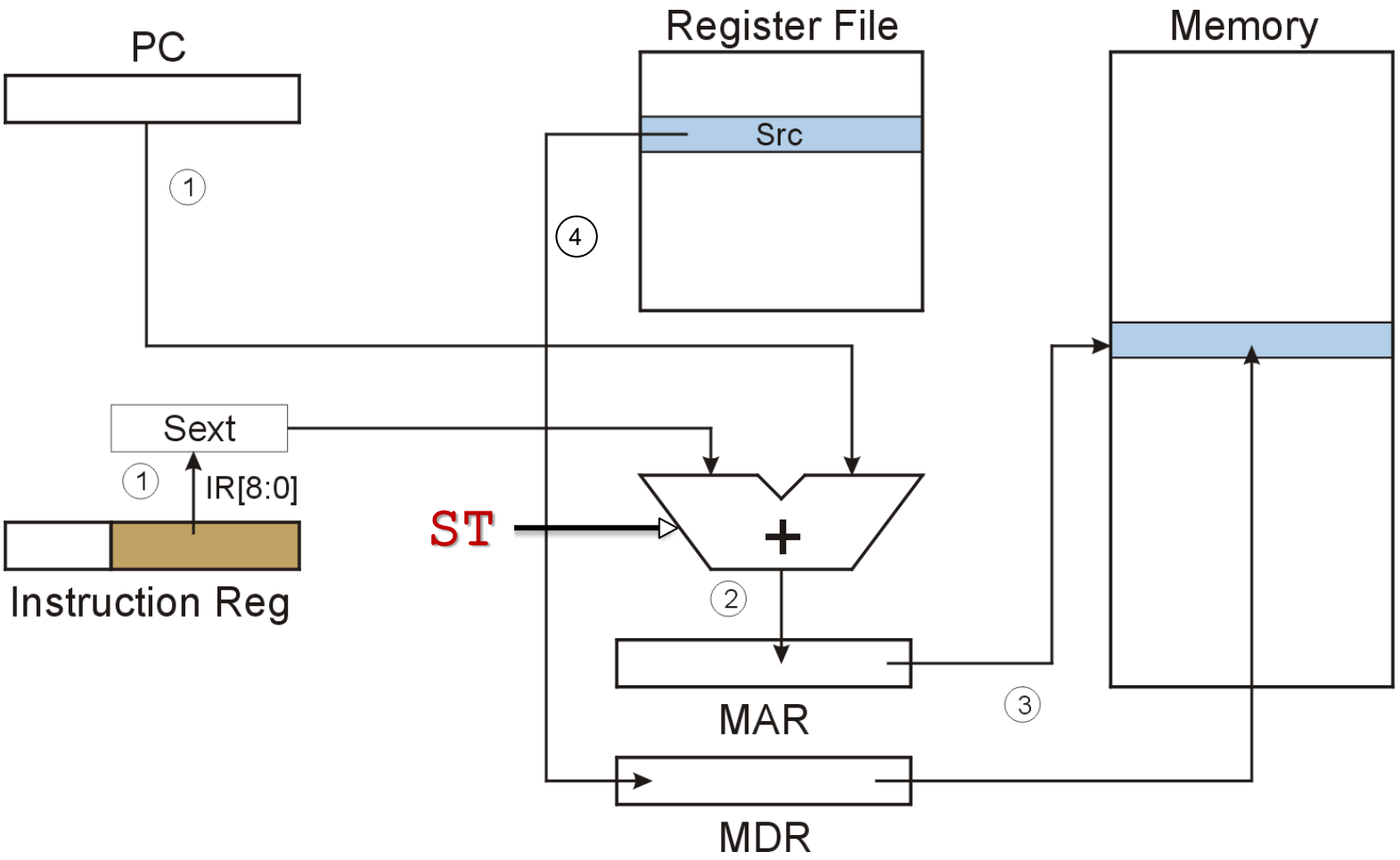
LD (PC-Relative)



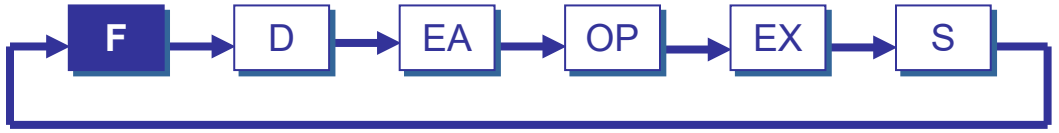


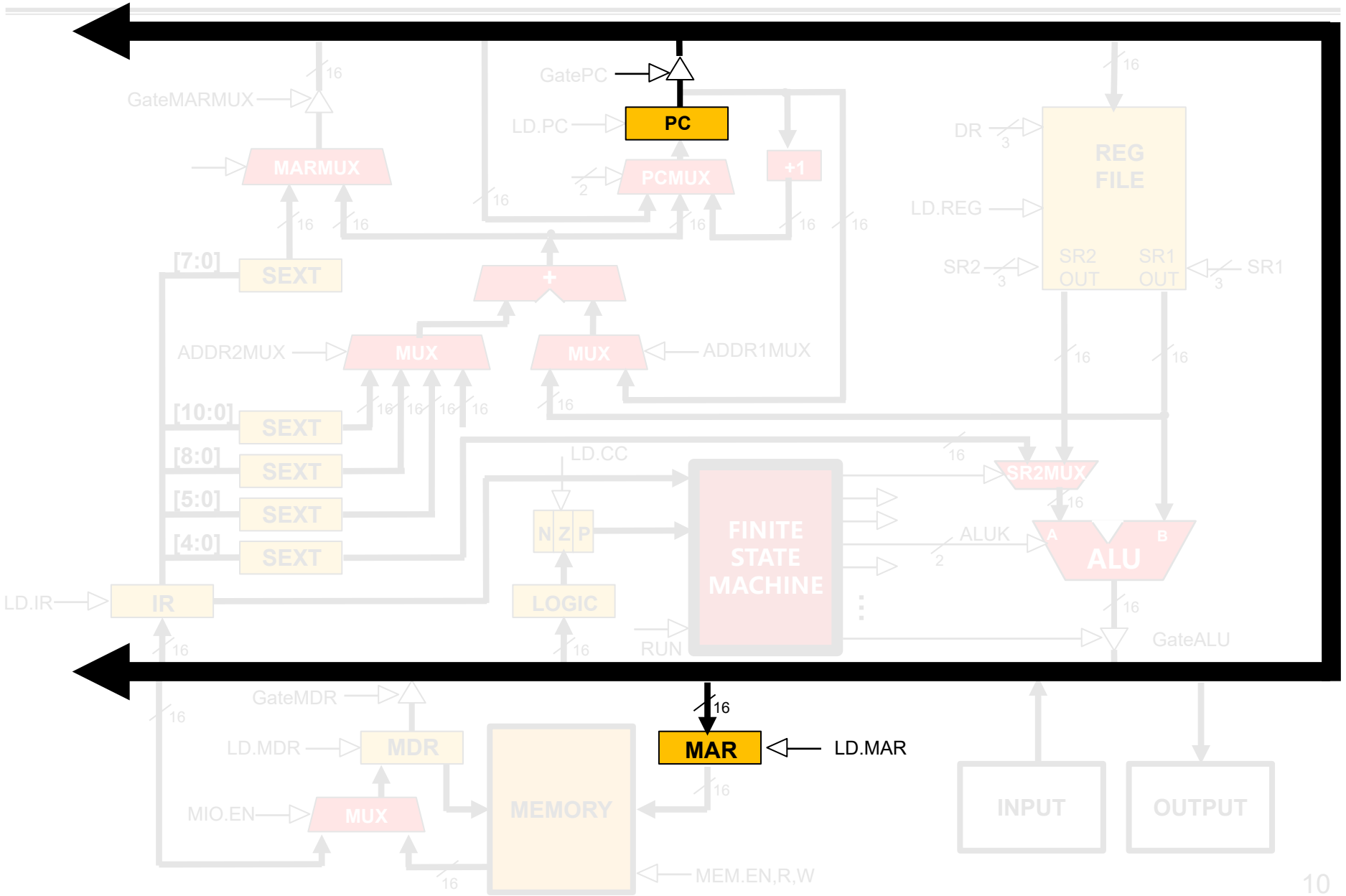
ST (PC-Relative) ST SR, PCoffset9



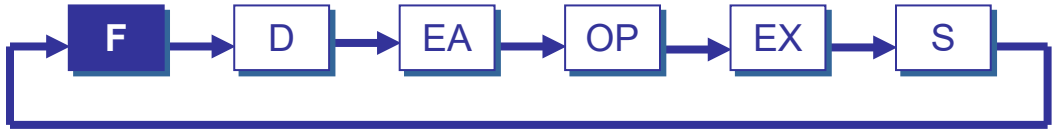


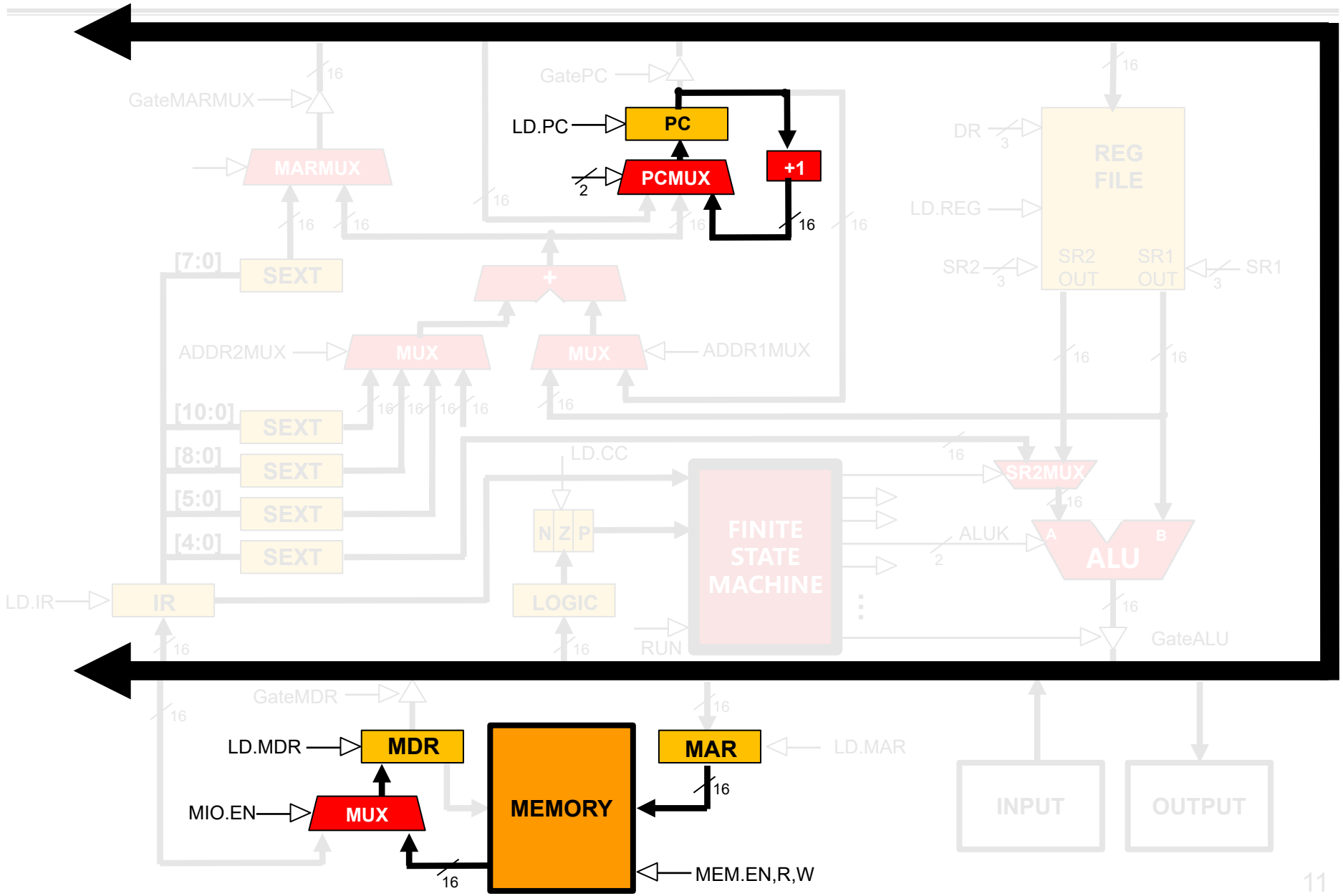
ST (PC-Relative)



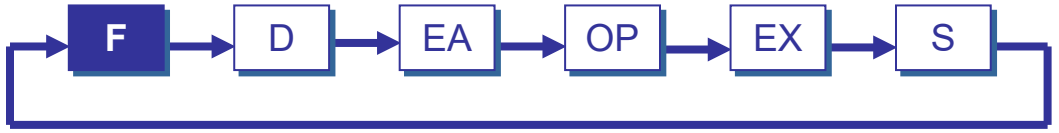


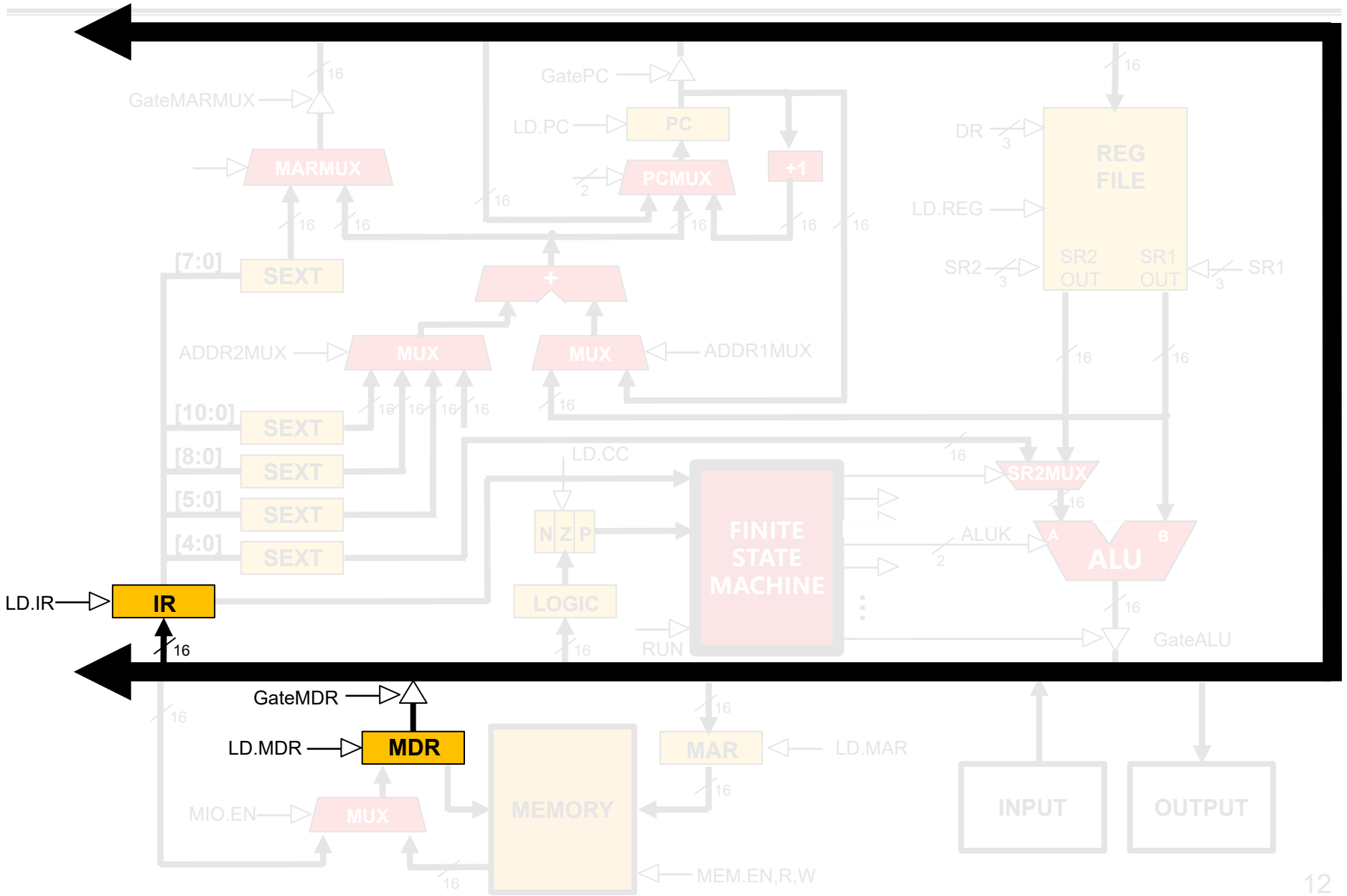
ST (PC-Relative)



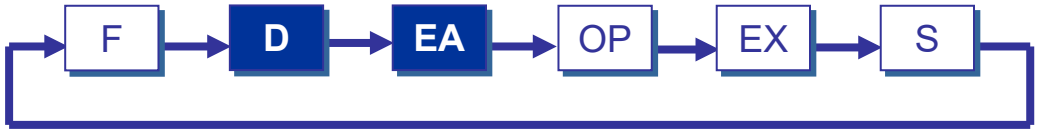


ST (PC-Relative)



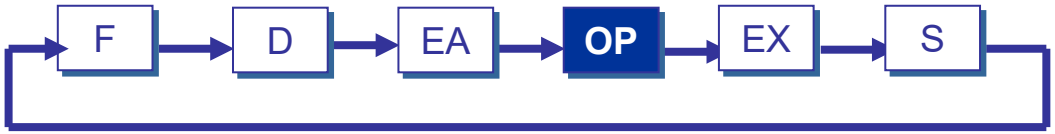


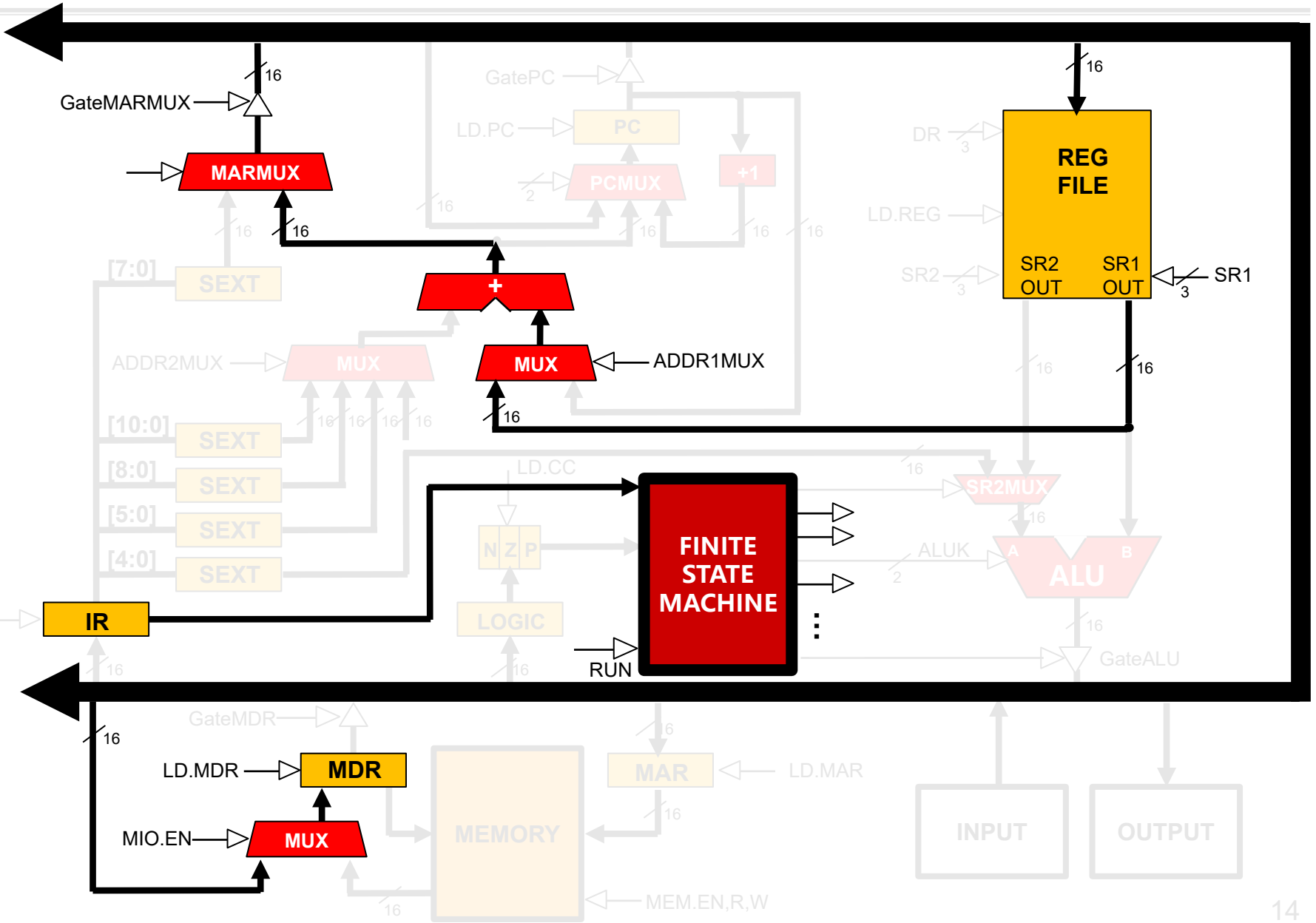
ST (PC-Relative)



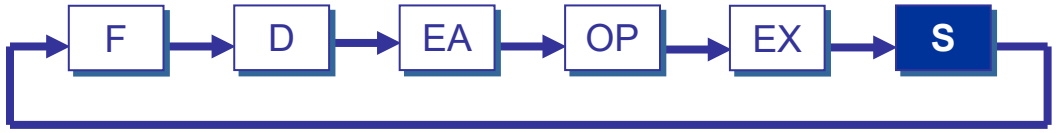
GateMARMUX
MARMUX
16
PC
LD.PC
GatePC
PCMUX
+1
+
ADDR2MUX
MUX
MUX
ADDR1MUX
[7:0]
SEXT
[10:0]
SEXT
[8:0]
SEXT
[5:0]
SEXT
[4:0]
SEXT
LD.IR
IR
LD.CC
N Z P
LOGIC
FINITE STATE MACHINE
RUN
DR
REG FILE
LD.REG
SR2
SR2 OUT
SR1 OUT
SR1
SR2MUX
ALUK
A
B
ALU
GateALU
GateMDR
LD.MDR
MDR
MIO.EN
MUX
MEMORY
MEM.EN,R,W
MAR
LD.MAR
INPUT
OUTPUT

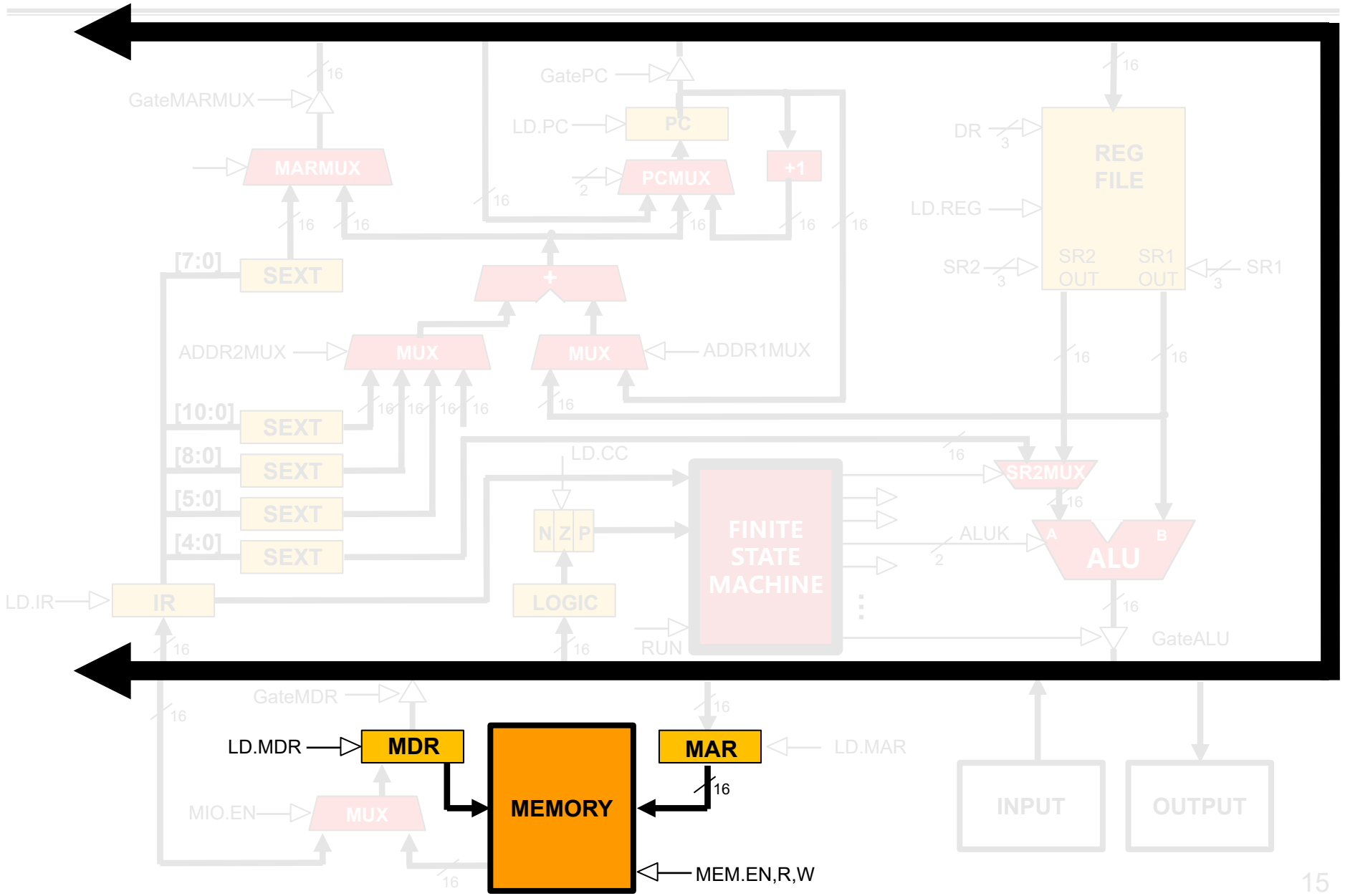
ST (PC-Relative)



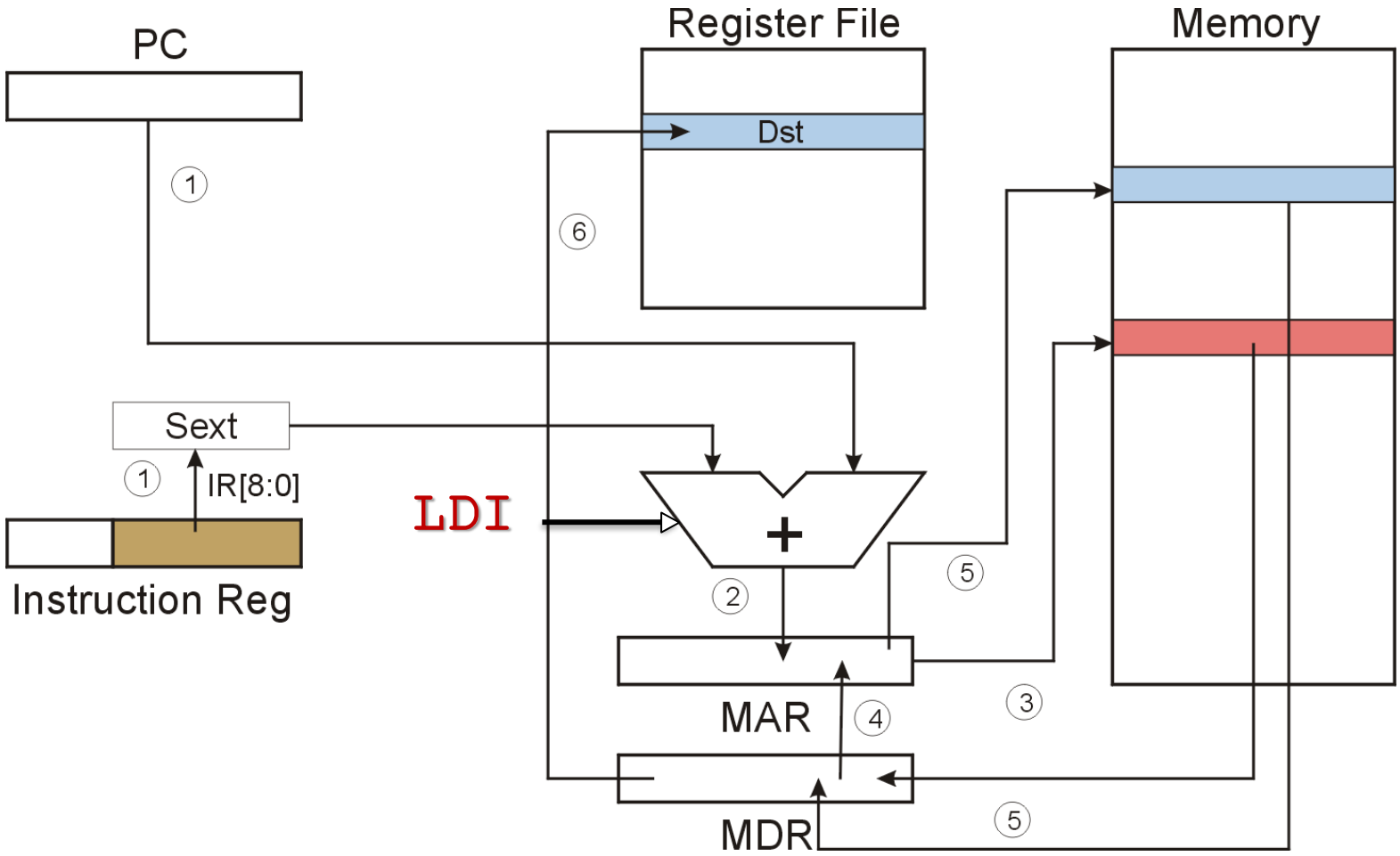


ST (PC-Relative)

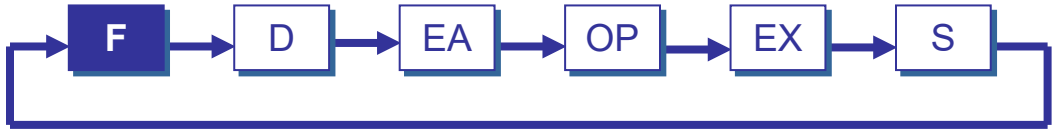


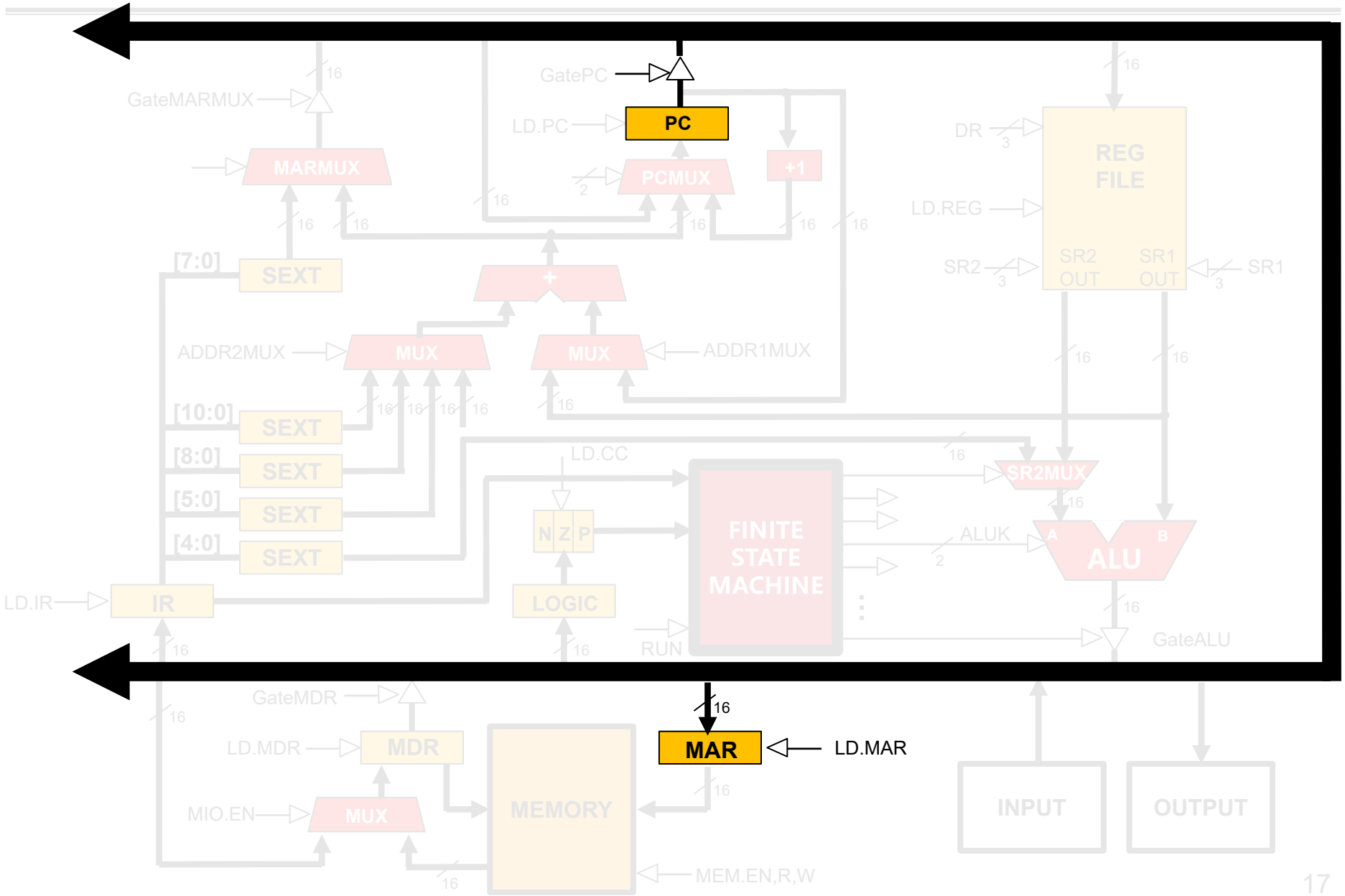


LDI (Indirect) LDI DR, PCoffset9

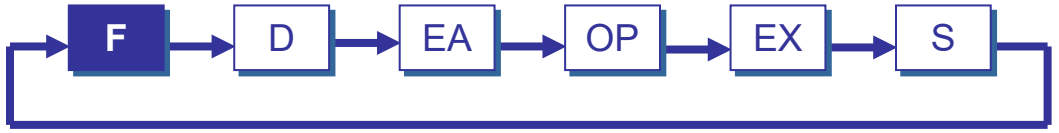


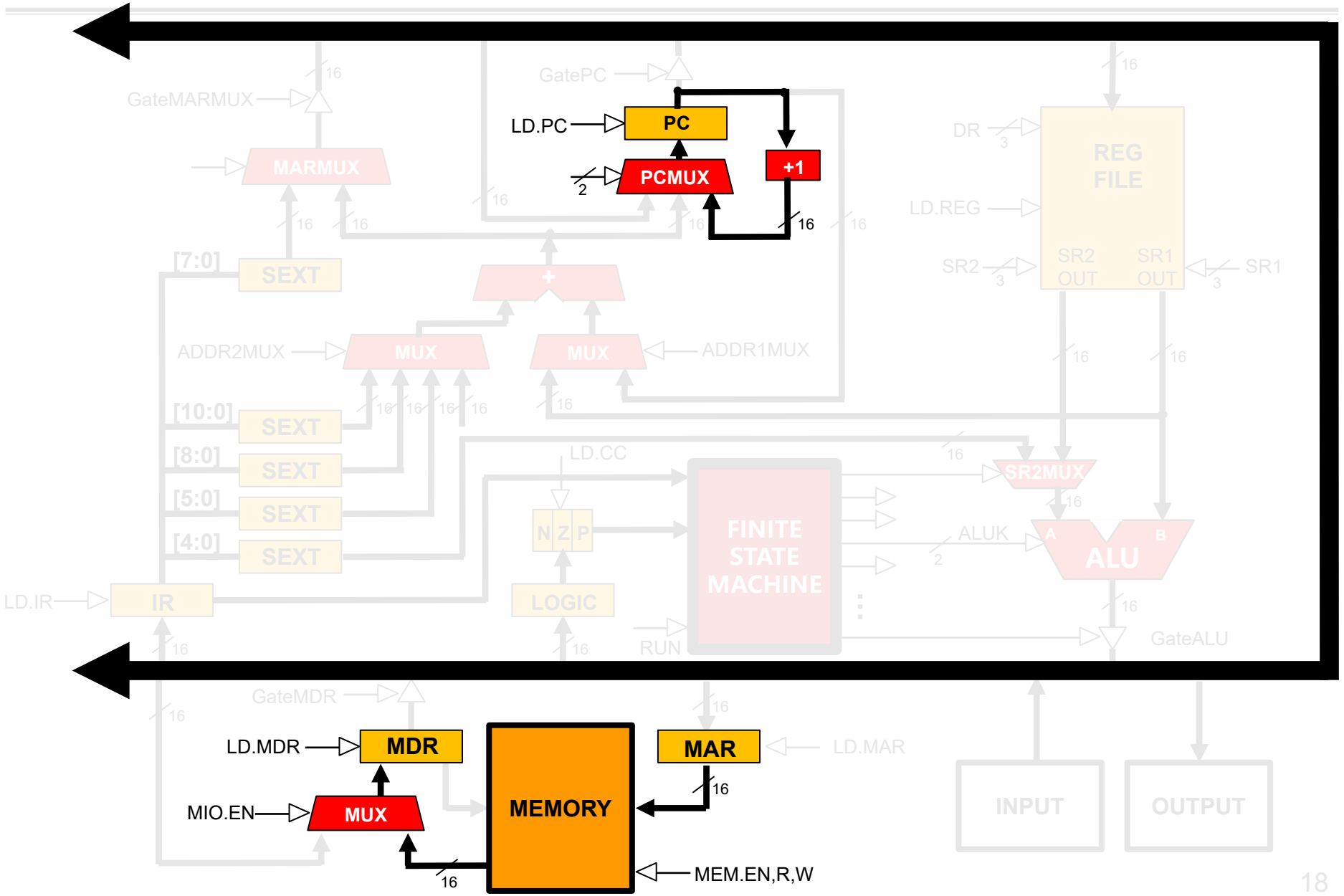
LDI (Indirect)



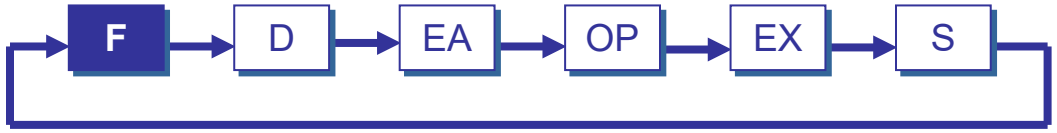


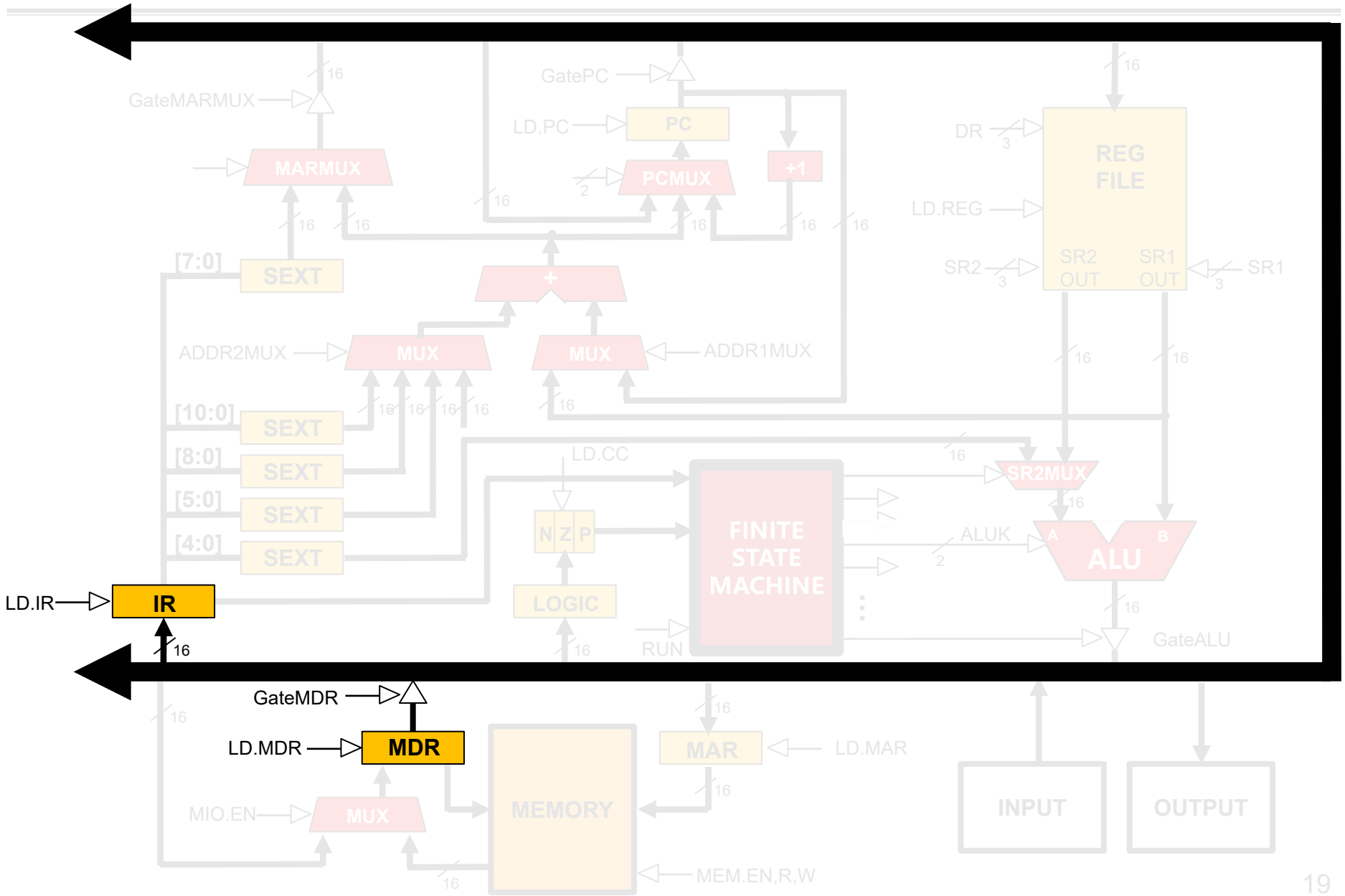
LDI (Indirect)



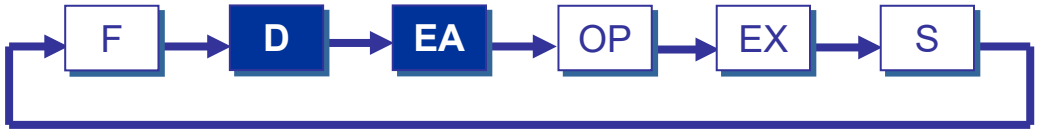


LDI (Indirect)





LDI (Indirect)



GateMARMUX
MARMUX
16
GatePC
LD.PC
PC
PCMUX
+1
+
ADDR2MUX
MUX
MUX
ADDR1MUX
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SEXT
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SEXT
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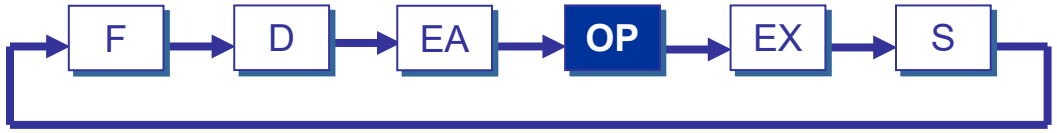
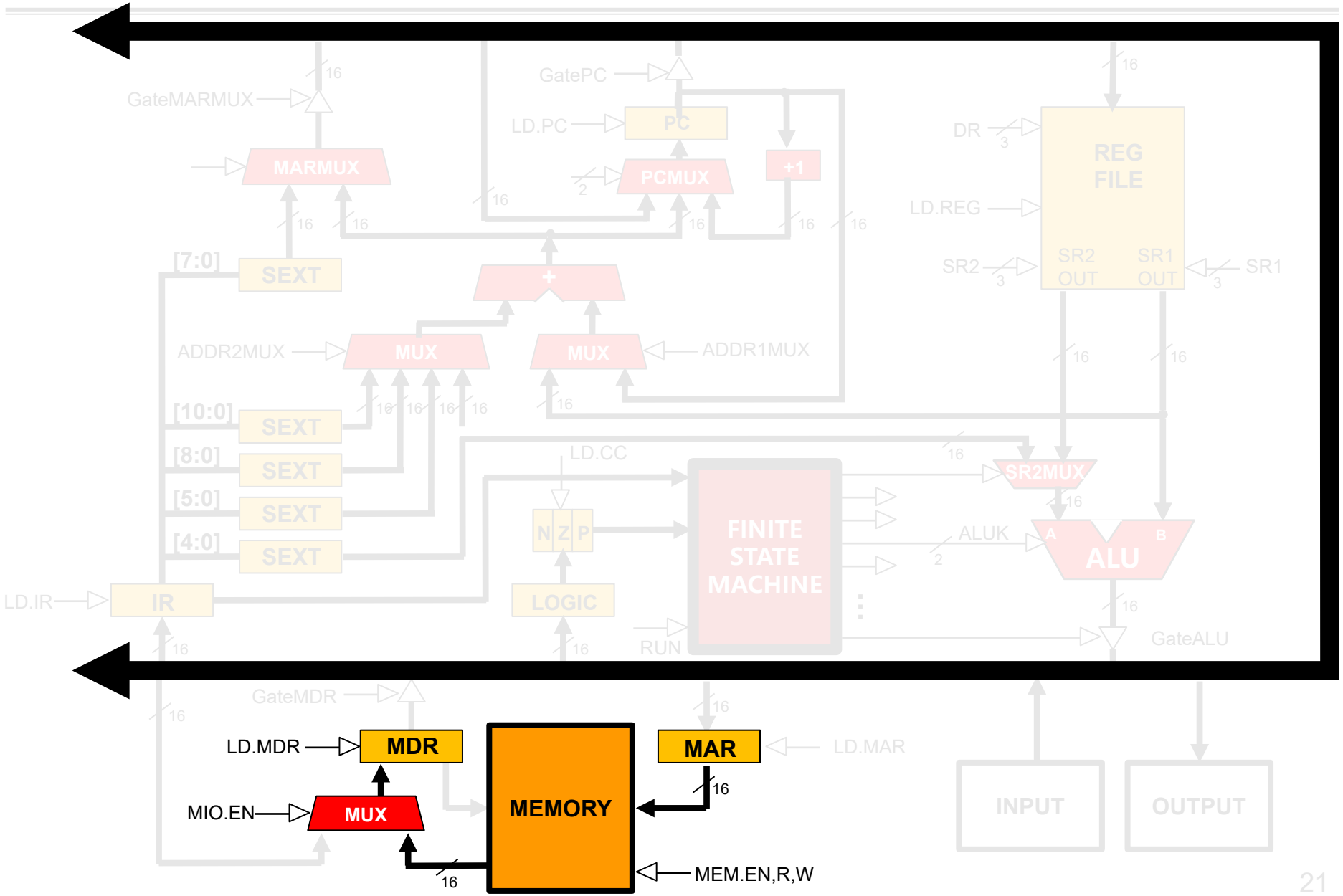
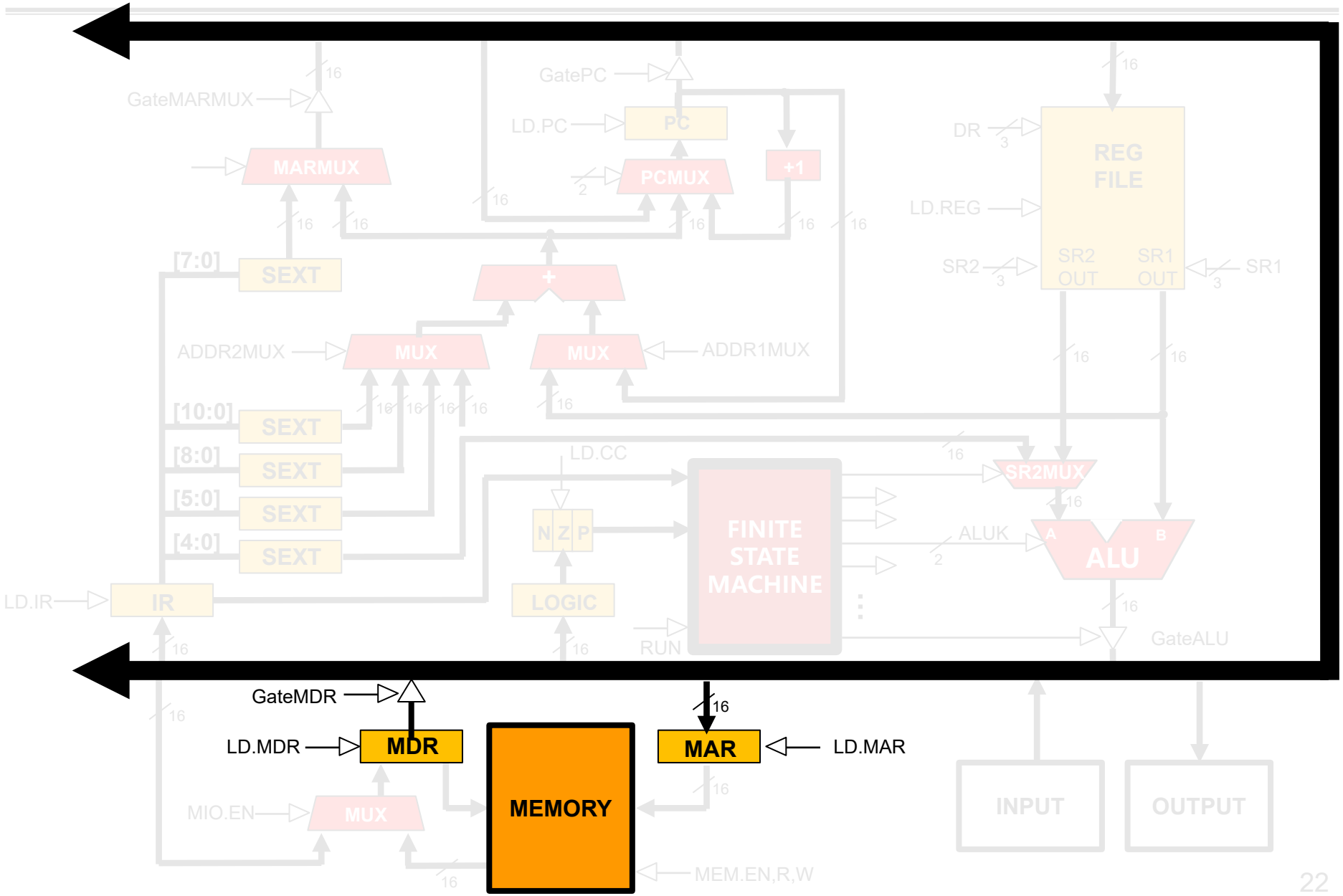
SEXT
LD.CC
N Z P
LOGIC
FINITE STATE MACHINE
RUN
LD.IR
IR
DR
REG FILE
LD.REG
SR2
SR2 OUT
SR1 OUT
SR1
SR2MUX
ALUK
A
B
ALU
GateALU
GateMDR
LD.MDR
MDR
MIO.EN
MUX
MEMORY
MEM.EN,R,W
MAR
LD.MAR
INPUT
OUTPUT

LDI (Indirect)

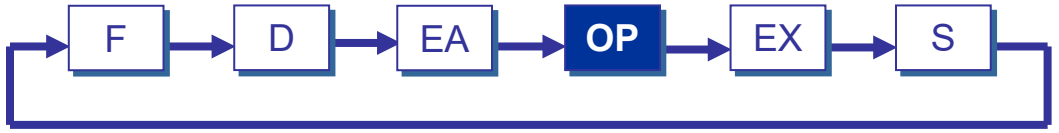


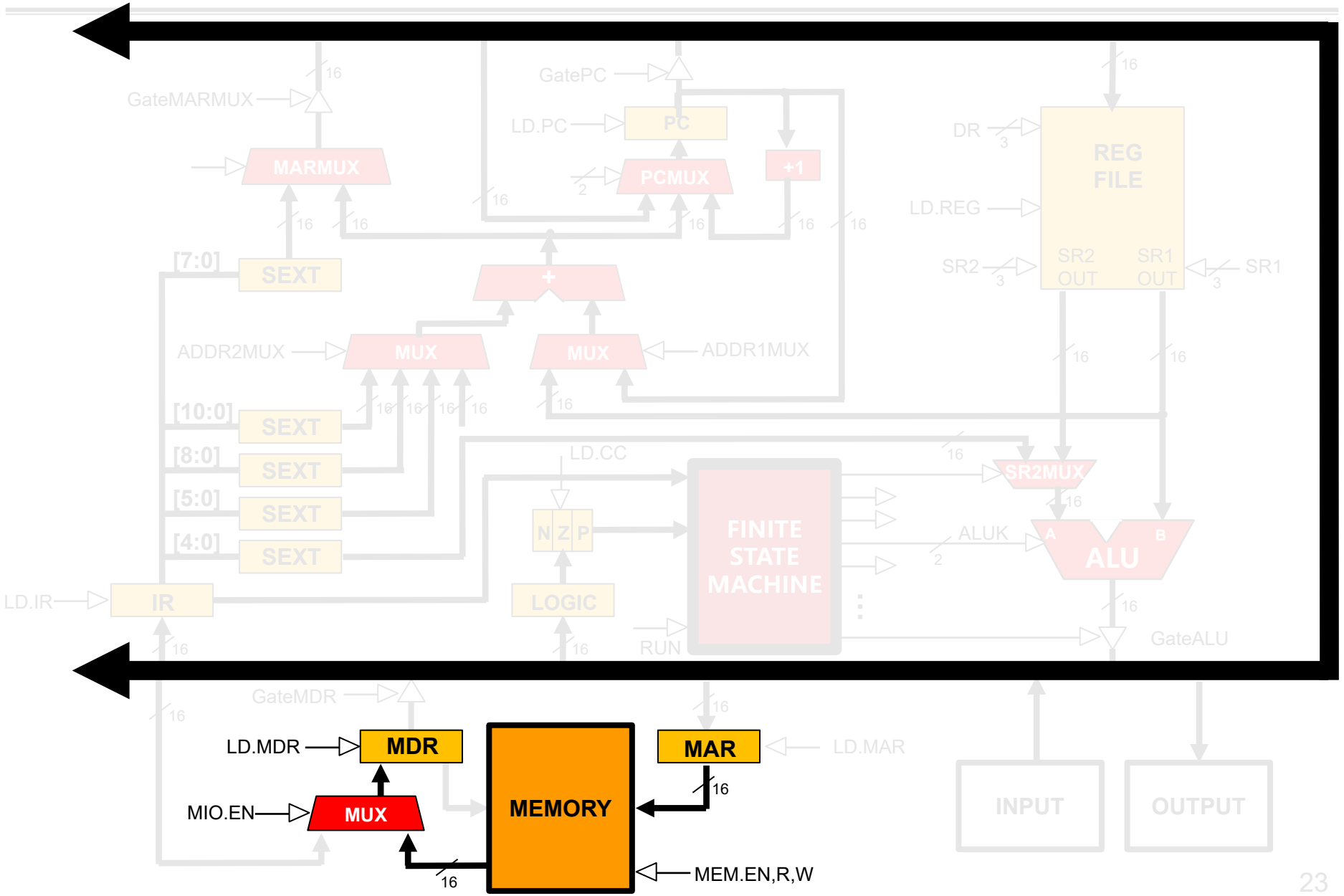


LDI (Indirect)

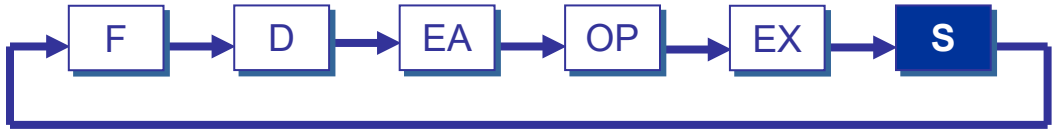


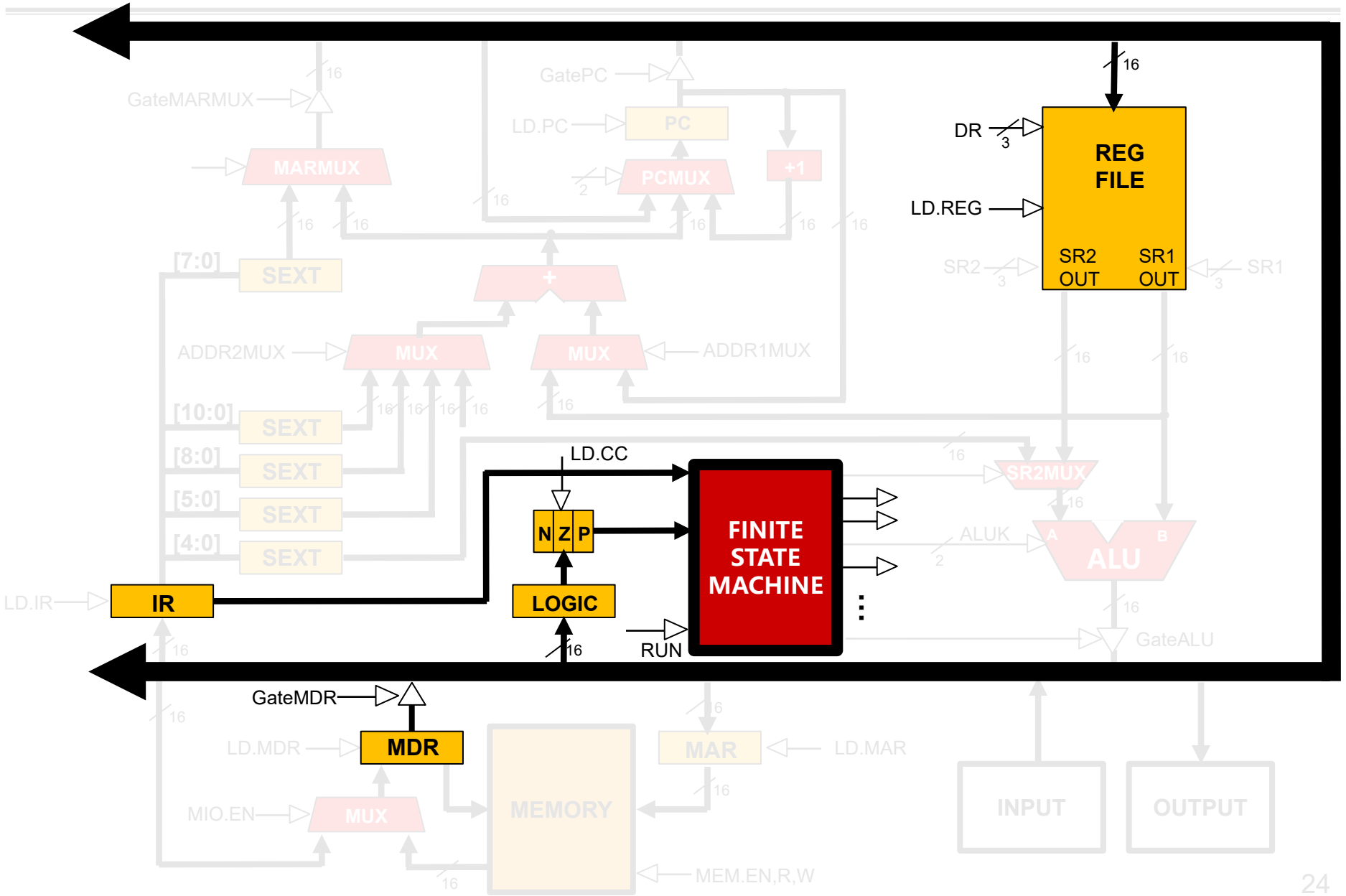
LDI (Indirect)



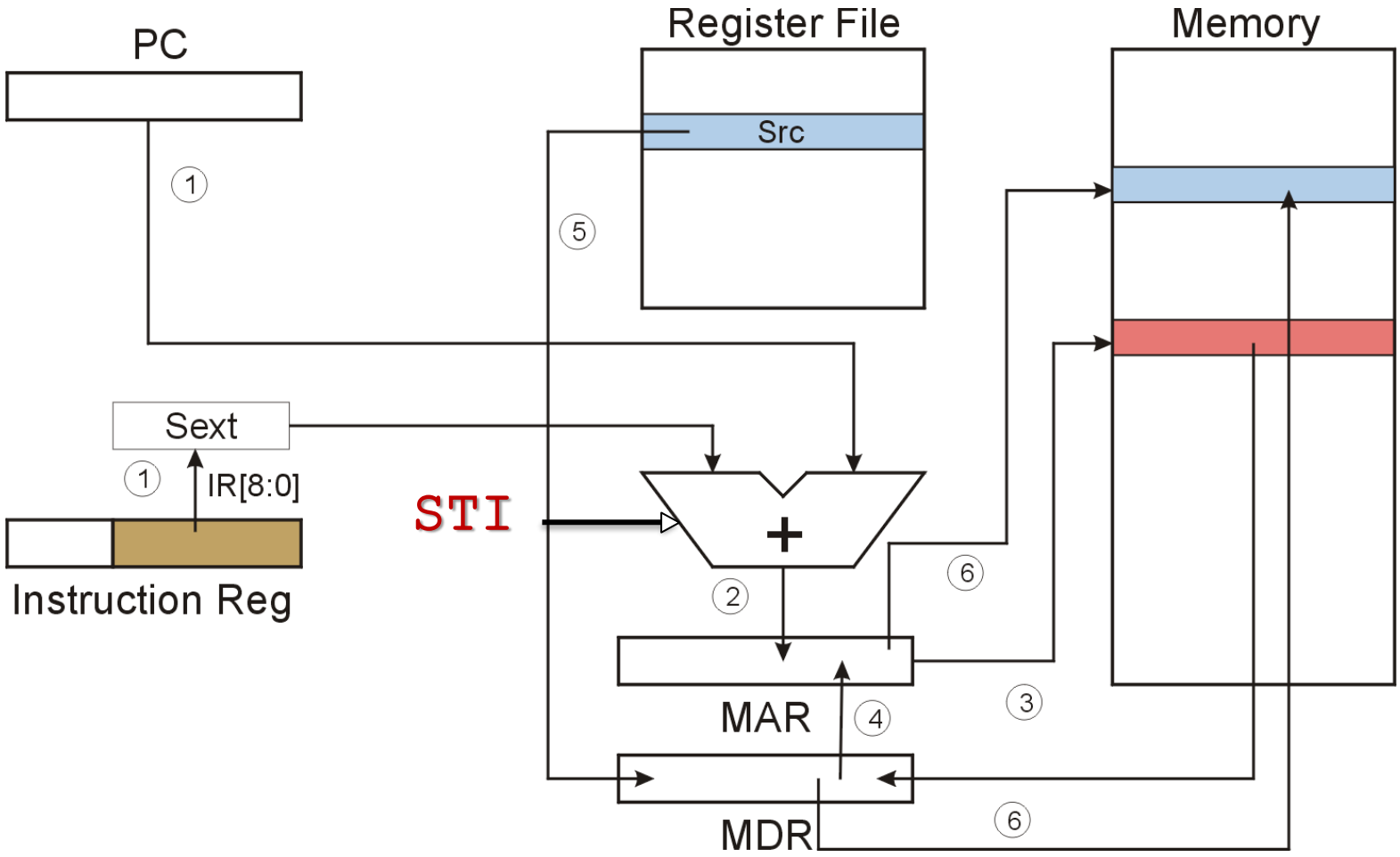


LDI (Indirect)

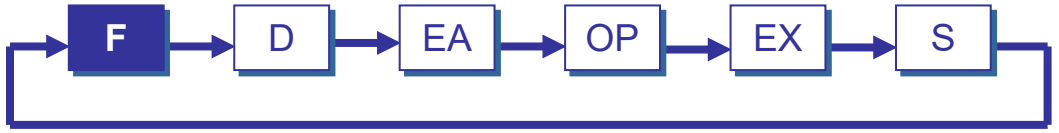


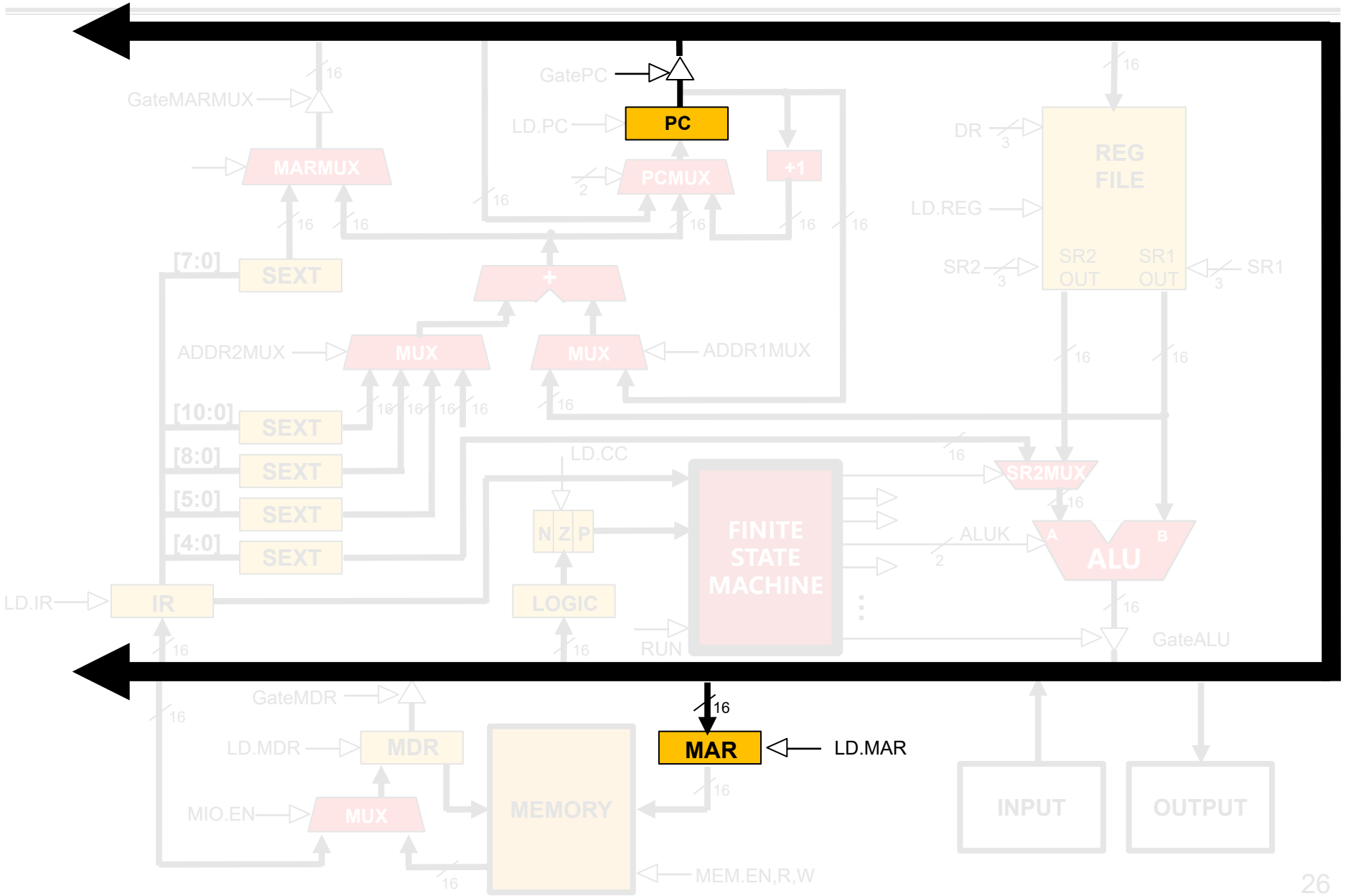


STI (Indirect) STI SR, PCoffset9

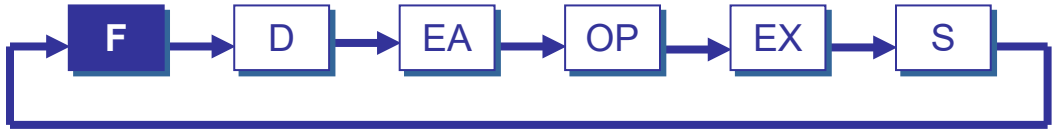


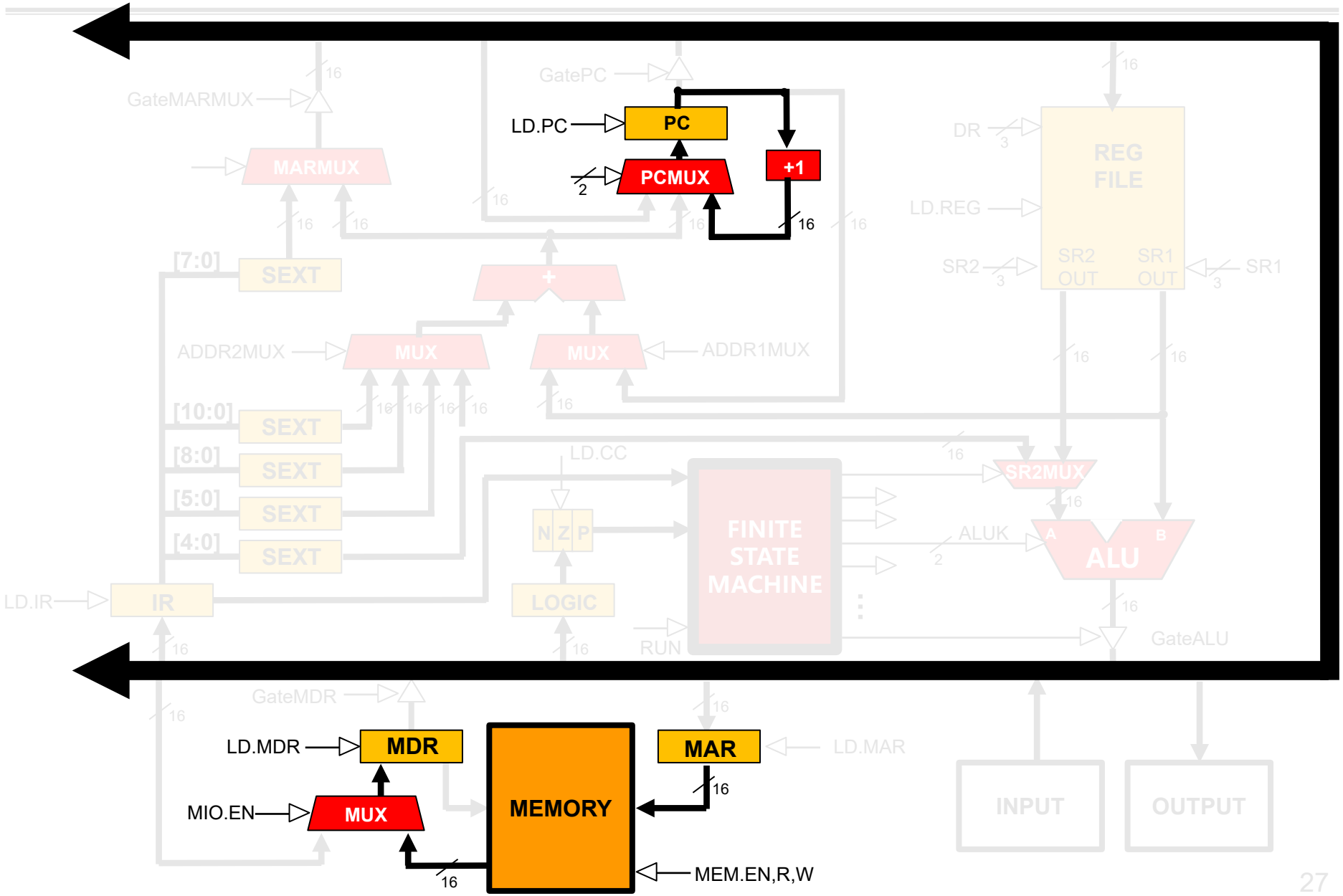
STI (Indirect)



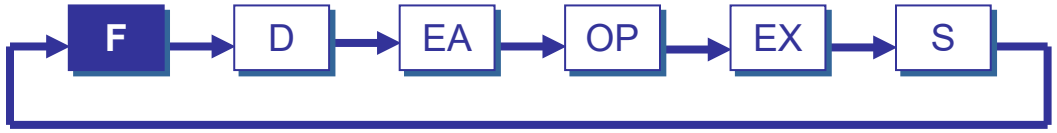


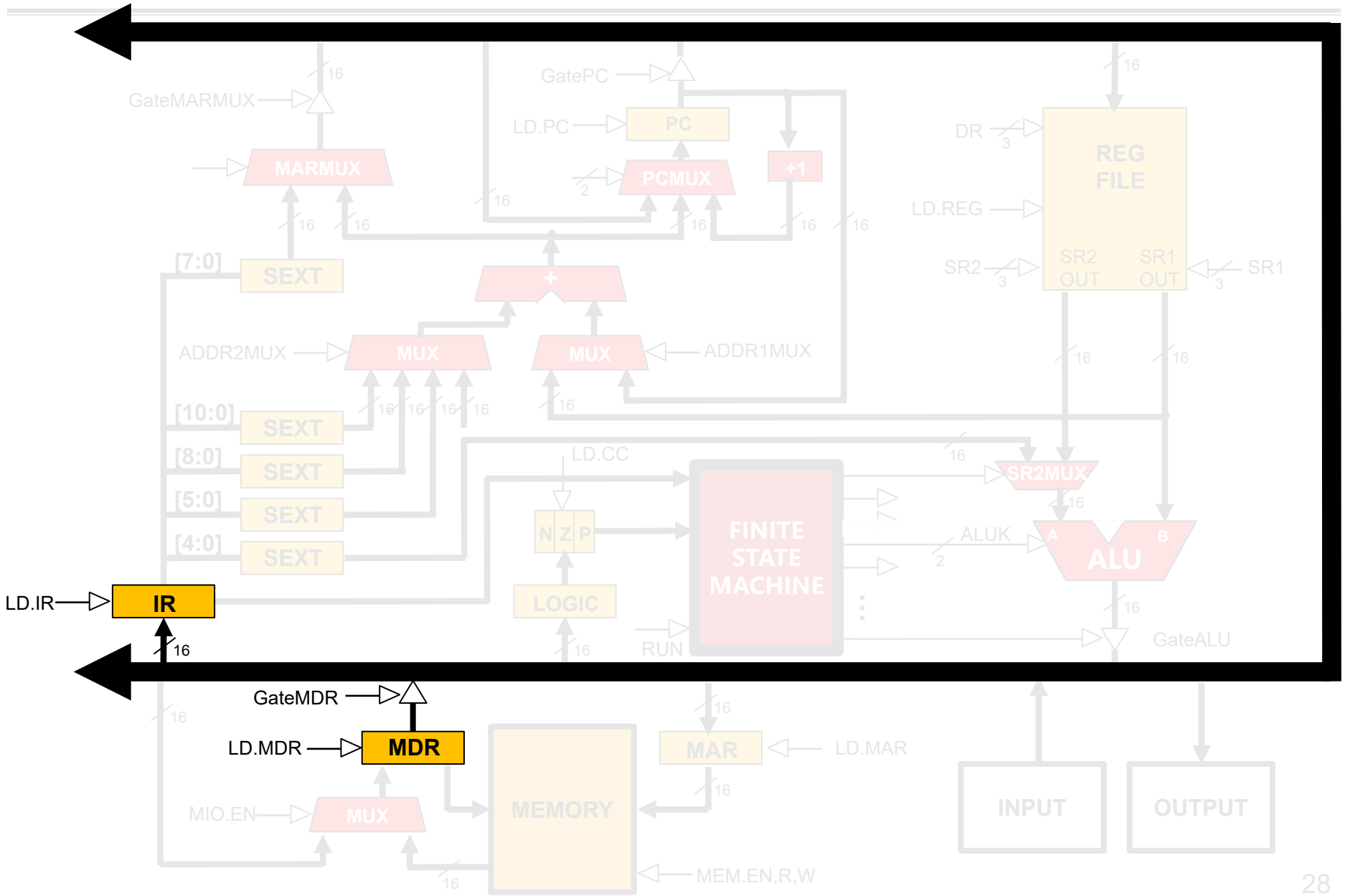
STI (Indirect)





STI (Indirect)





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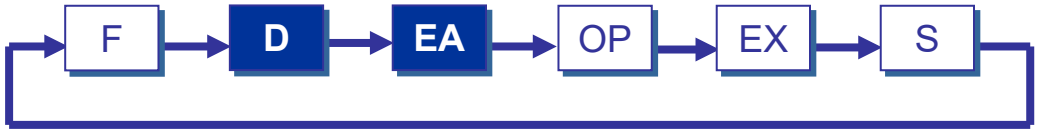

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LD.PC
PC
PCMUX
+1
+
ADDR2MUX
MUX
MUX
ADDR1MUX
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SEXT
[5:0]
SEXT
[4:0]
SEXT
LD.IR
IR
LD.CC
N Z P
LOGIC
FINITE STATE MACHINE
RUN
DR
REG FILE
LD.REG
SR2
SR2 OUT
SR1 OUT
SR1
SR2MUX
ALUK
A
B
ALU
GateALU
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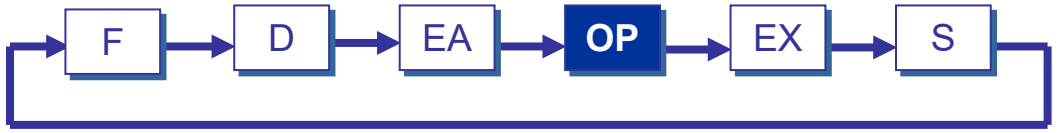
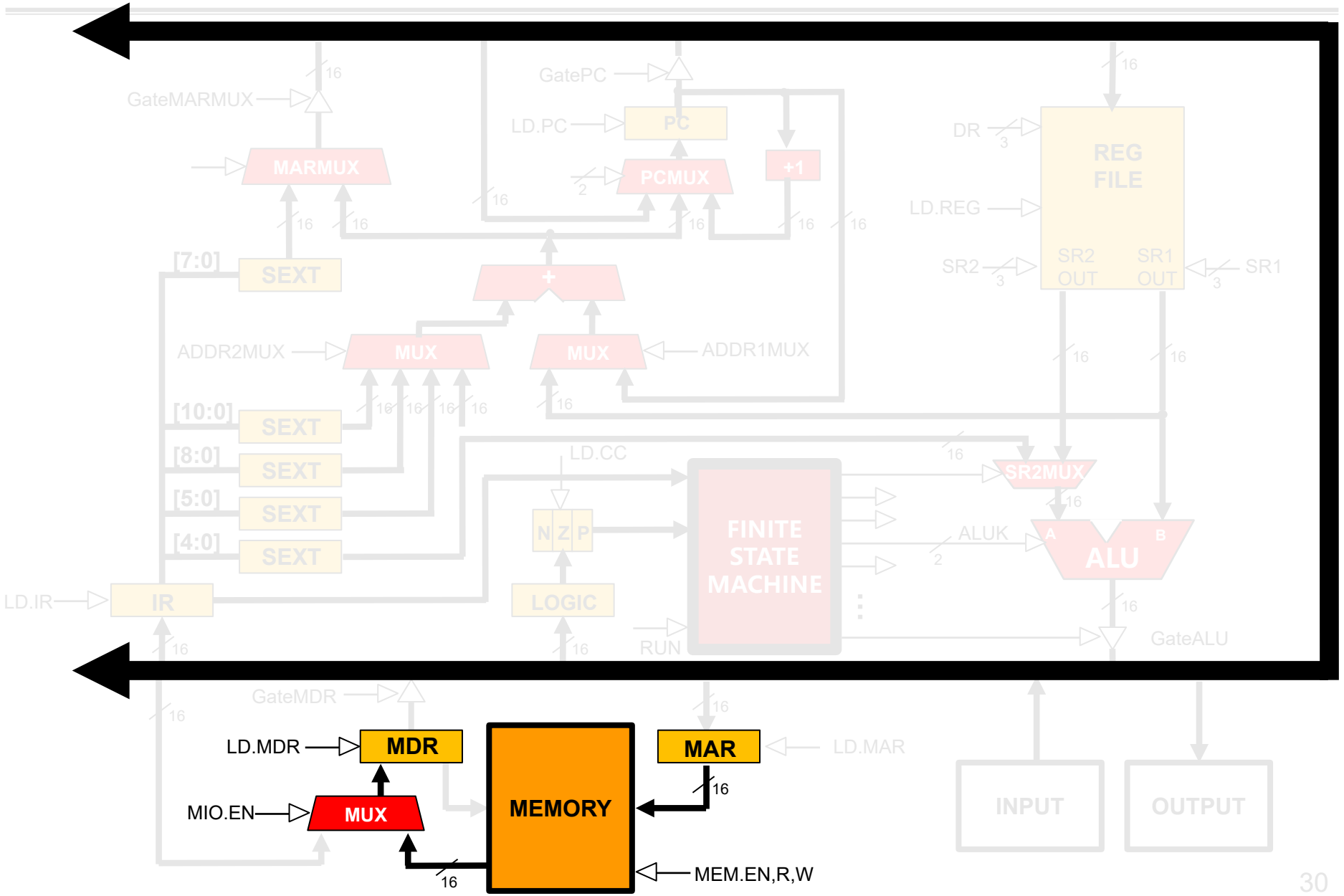
MDR
MIO.EN
MUX
MEMORY
MEM.EN,R,W
MAR
LD.MAR
INPUT
OUTPUT

STI (Indirect)





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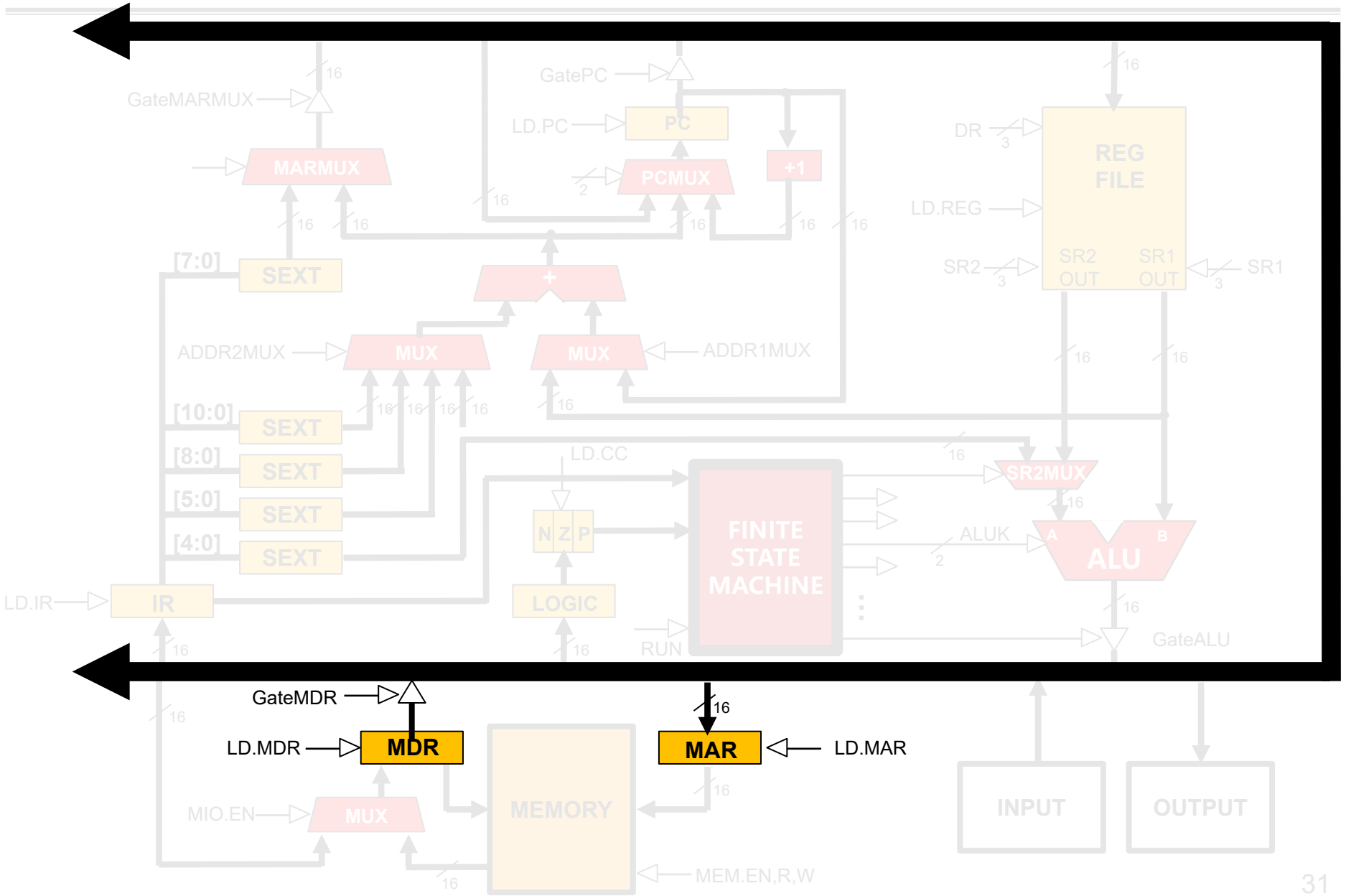
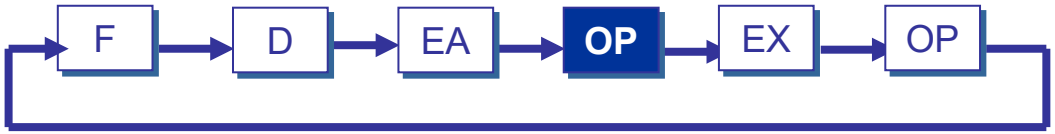


STI (Indirect)



GateMARMUX
MARMUX
16
+
MUX
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SEXT
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[8:0]
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[4:0]
ADDR2MUX
REG FILE
DR
SR1
SR2
LD.REG
SR2 OUT
SR1 OUT
LD.CC
N Z P
FINITE STATE MACHINE
RUN
SR2MUX
ALUK
ALU
GateALU
LD.IR
IR
LOGIC
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LD.PC
PC
PCMUX
+1
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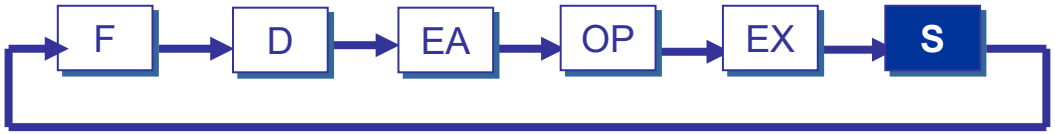
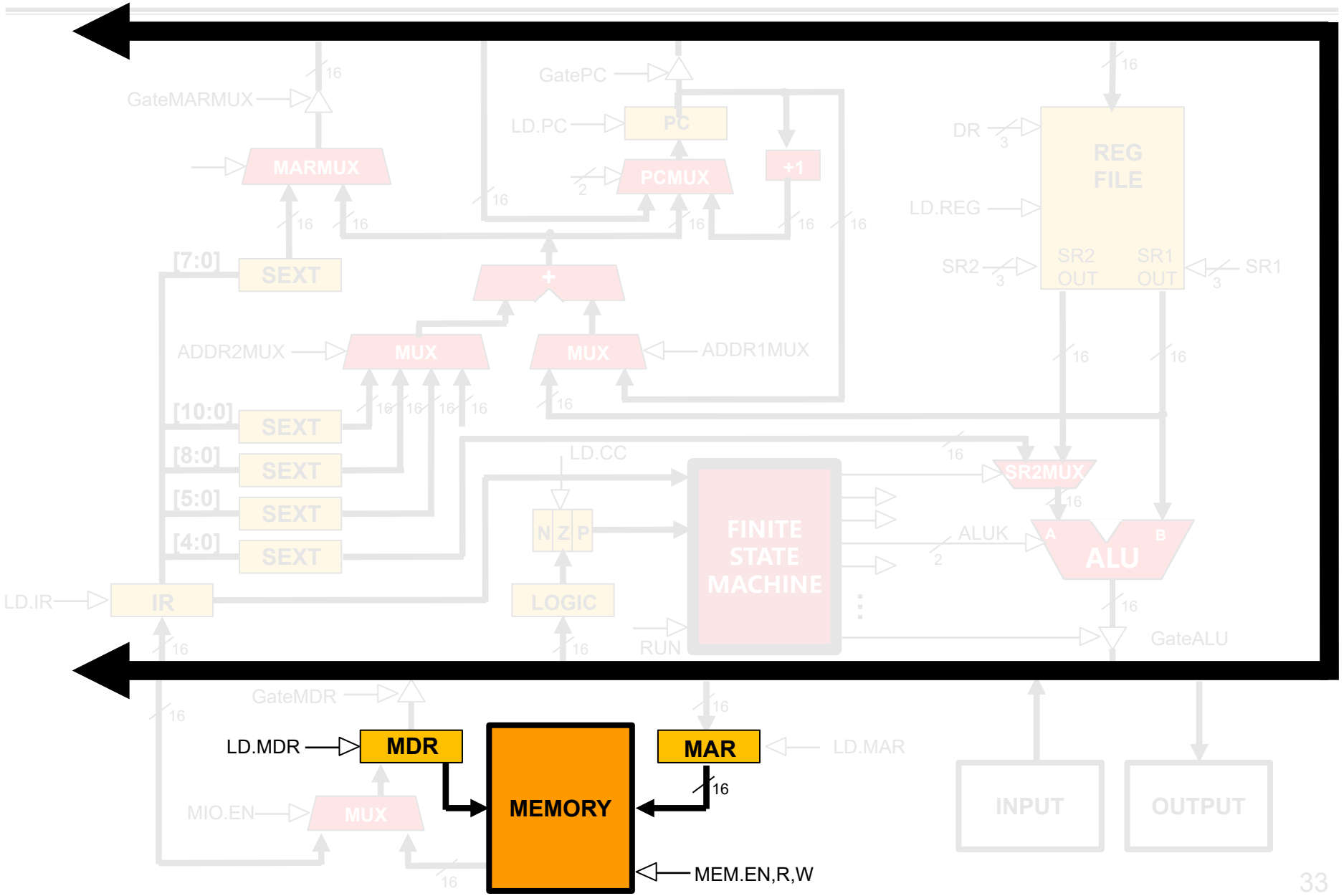
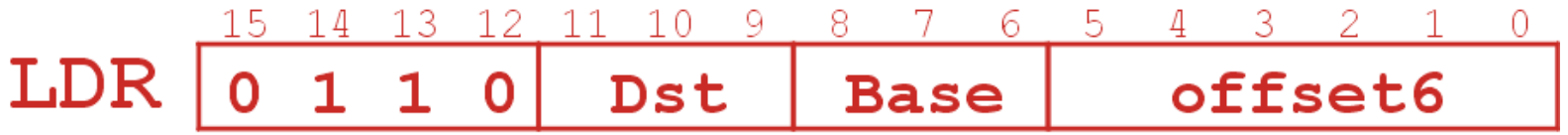
MEMORY
MAR
LD.MAR
MEM.EN,R,W
INPUT
OUTPUT

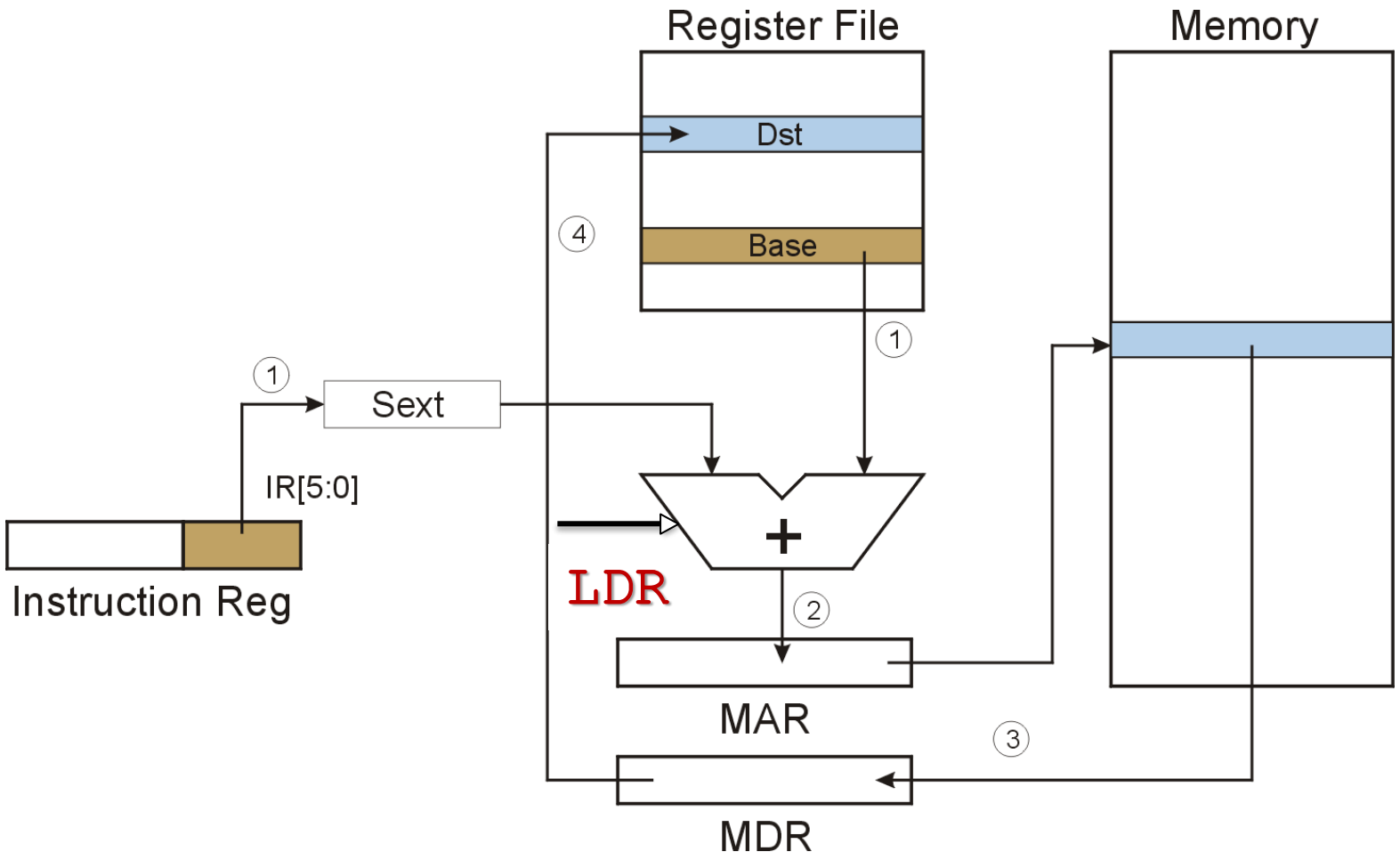
STI (Indirect)



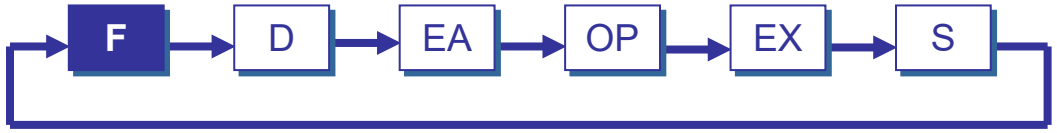


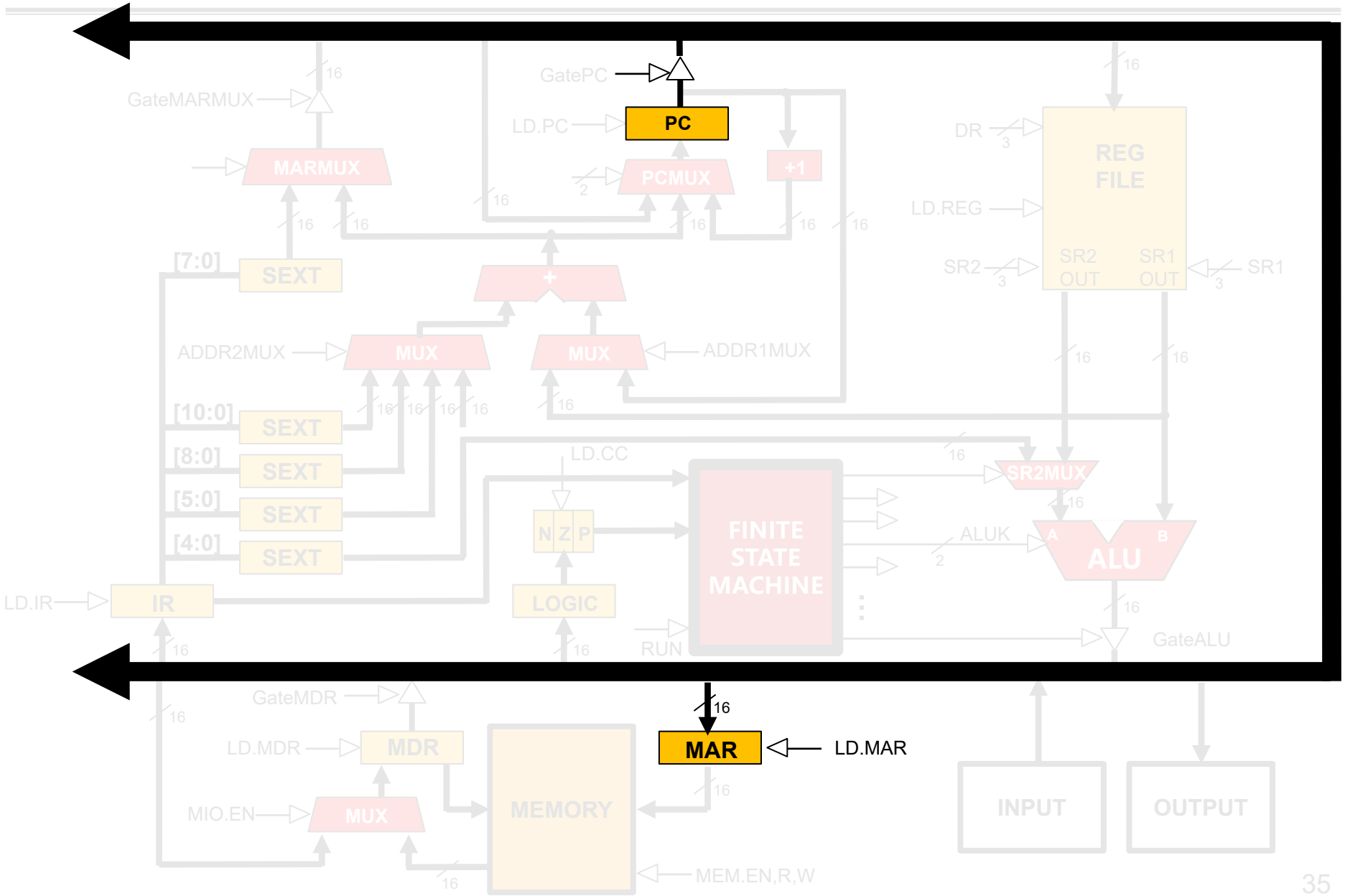
LDR (Base+Offset) LDR DR, BaseR, offset6



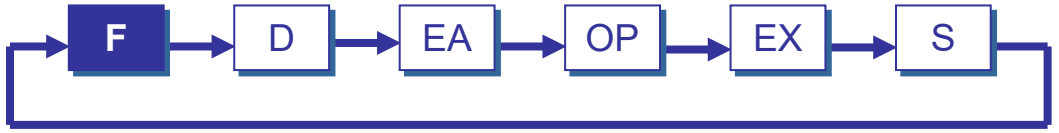


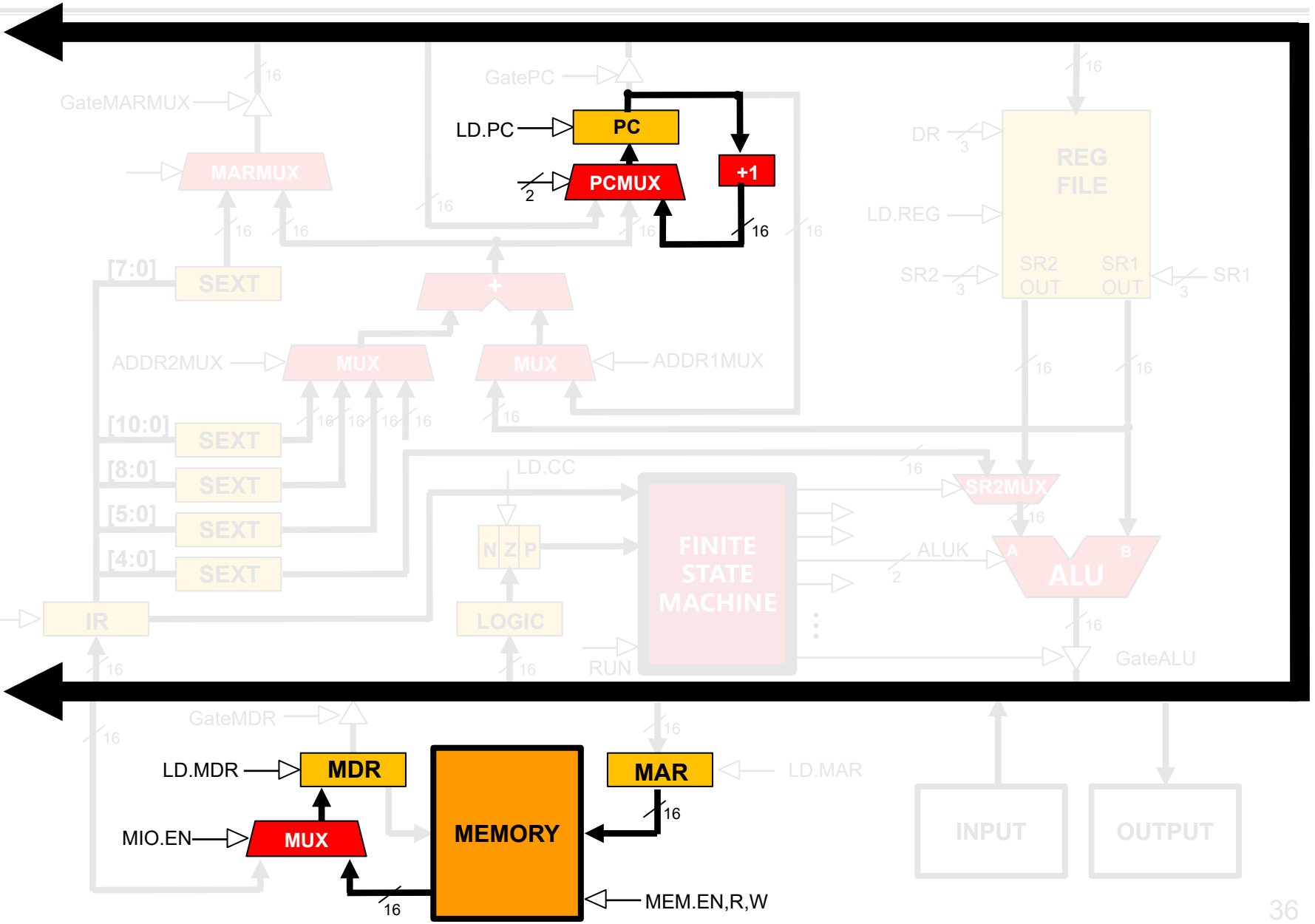
LDR (Base+Offset)



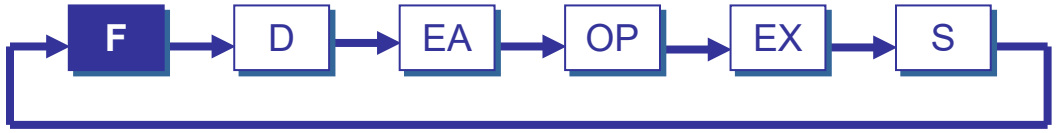


LDR (Base+Offset)

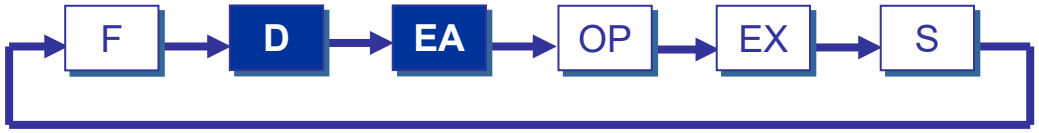




LDR (Base+Offset)



LDR (Base+Offset)



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MARMUX
16
+
ADDR2MUX
MUX
MUX
ADDR1MUX
16
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SEXT
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SEXT
LD.IR
IR
GatePC
LD.PC
PC
PCMUX
+1
2
16
DR
3
REG FILE
LD.REG
SR2
3
SR2 OUT
SR1 OUT
SR1
3
16
16
16
LD.CC
N Z P
LOGIC
FINITE STATE MACHINE
RUN
SR2MUX
ALUK
2
A
B
ALU
GateALU
GateMDR
LD.MDR
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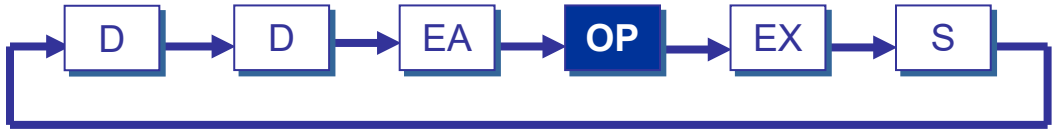
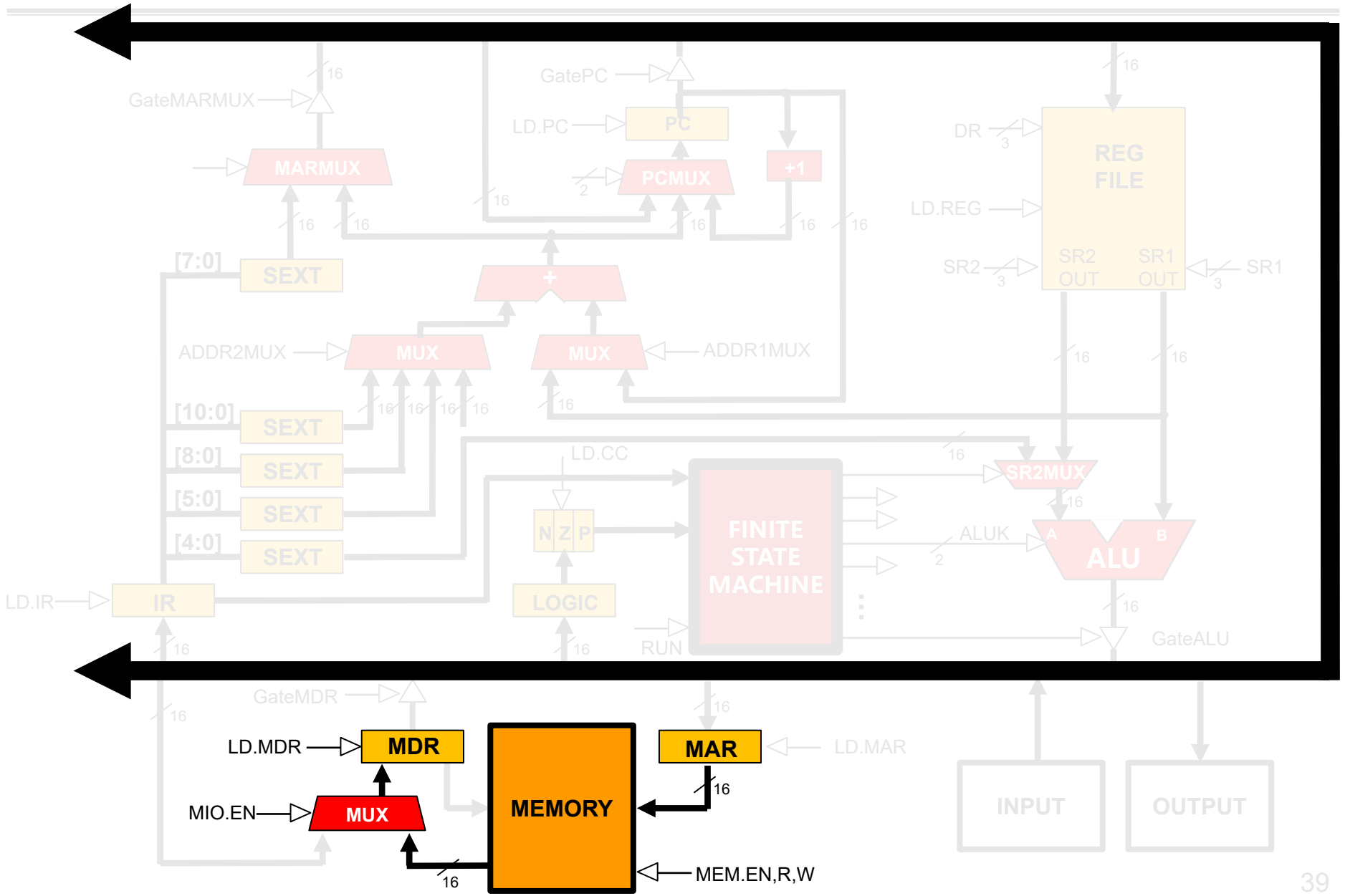
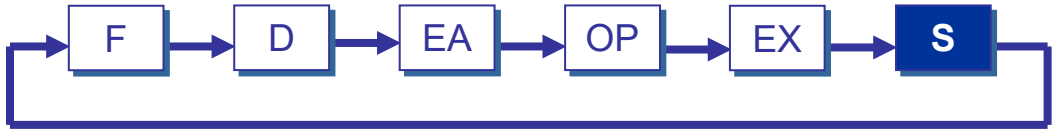
MIO.EN
MUX
MEMORY
MEM.EN,R,W
16
MAR
LD.MAR
INPUT
OUTPUT

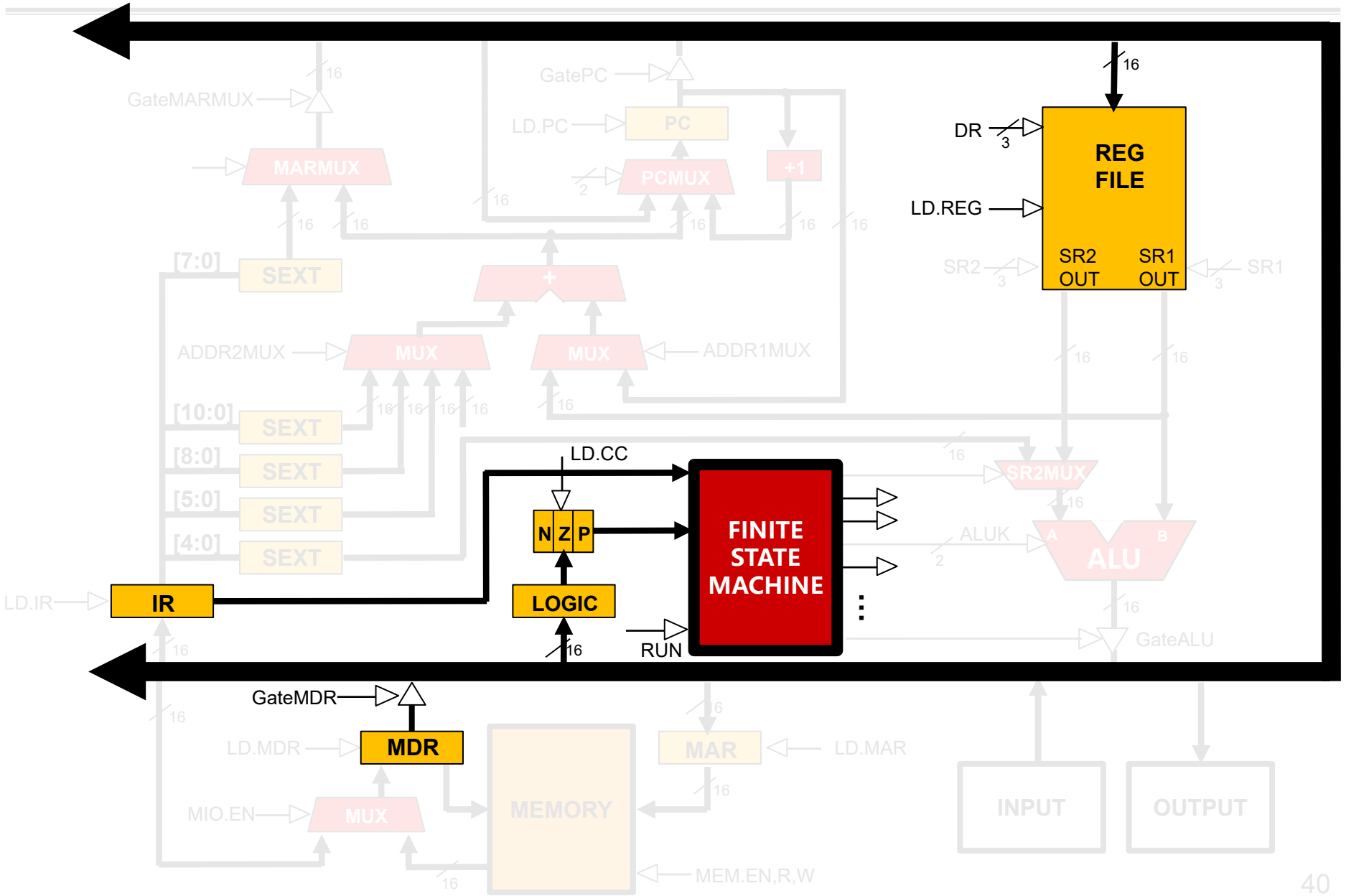
LDR (Base+Offset)



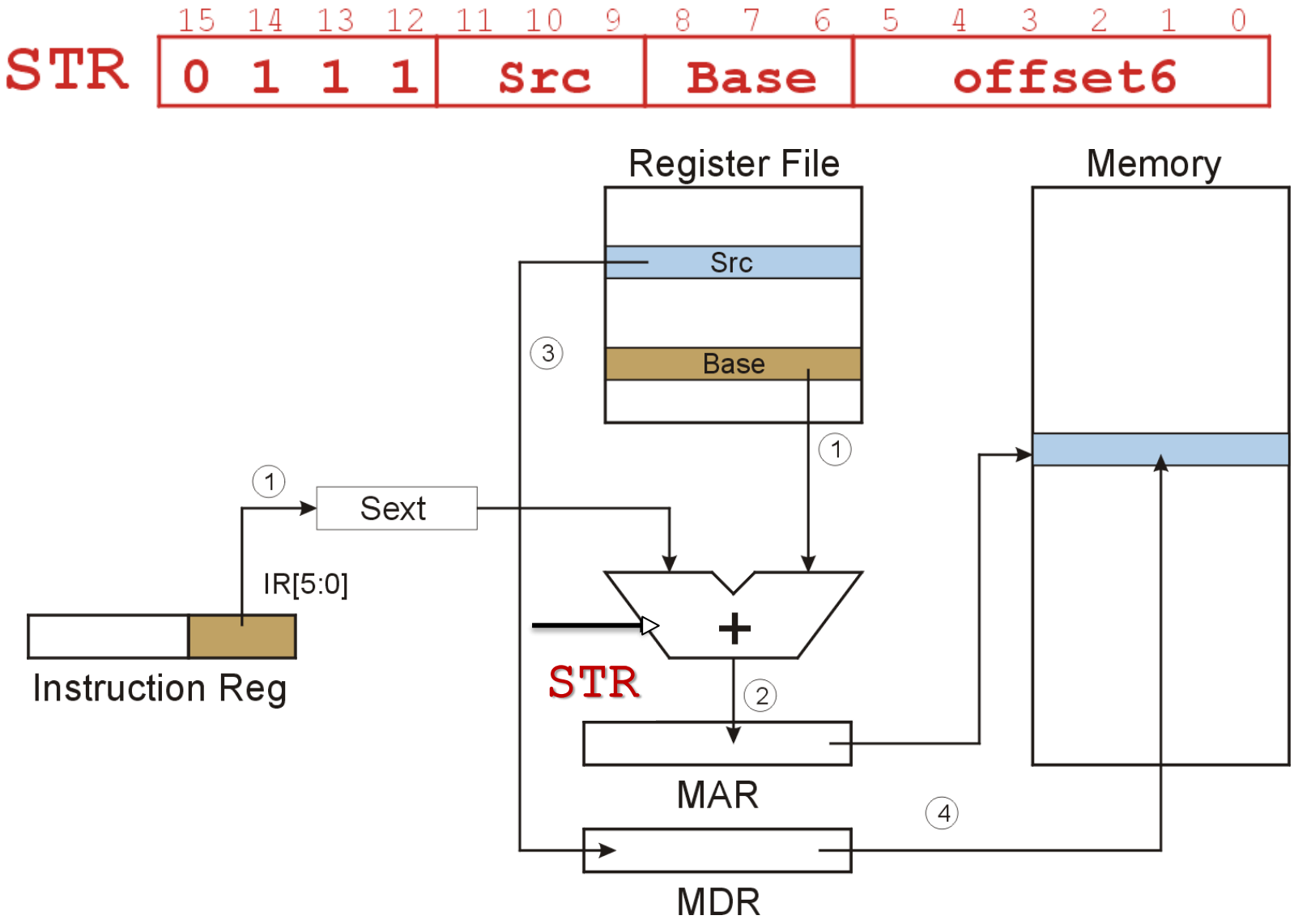


LDR (Base+Offset)

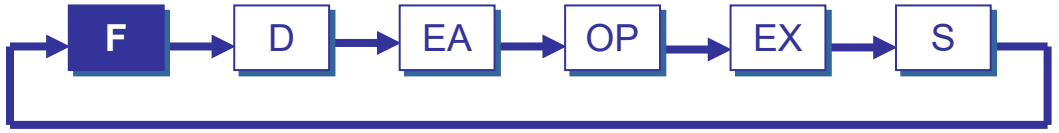


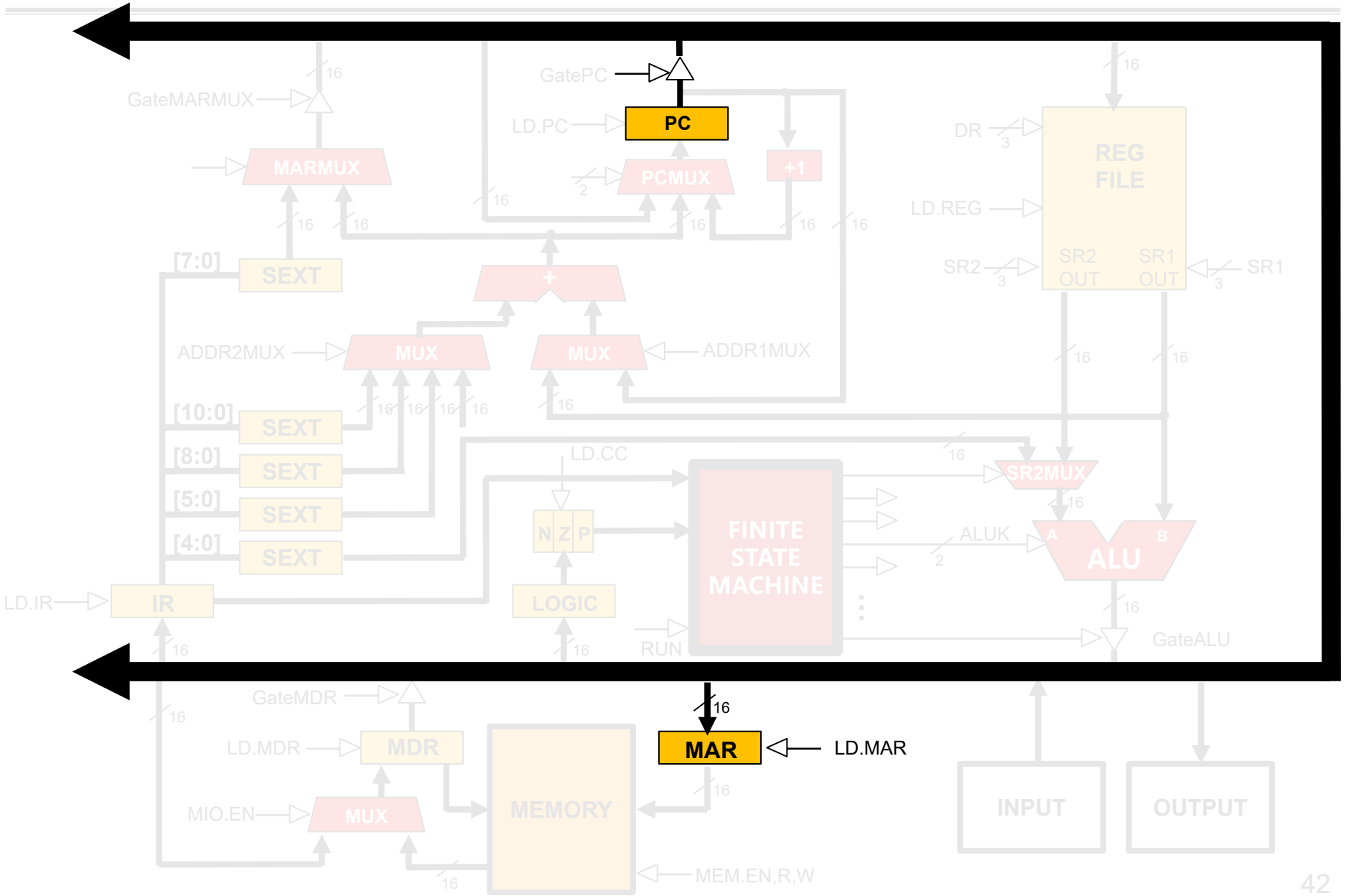


STR (Base+Offset) STR SR, BaseR, offset6



STR (Base+Offset)





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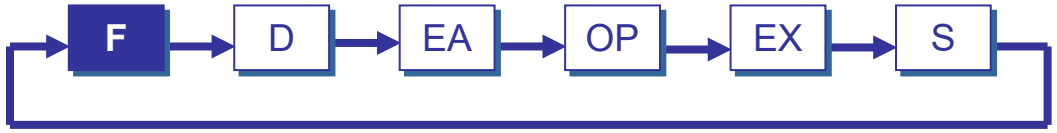

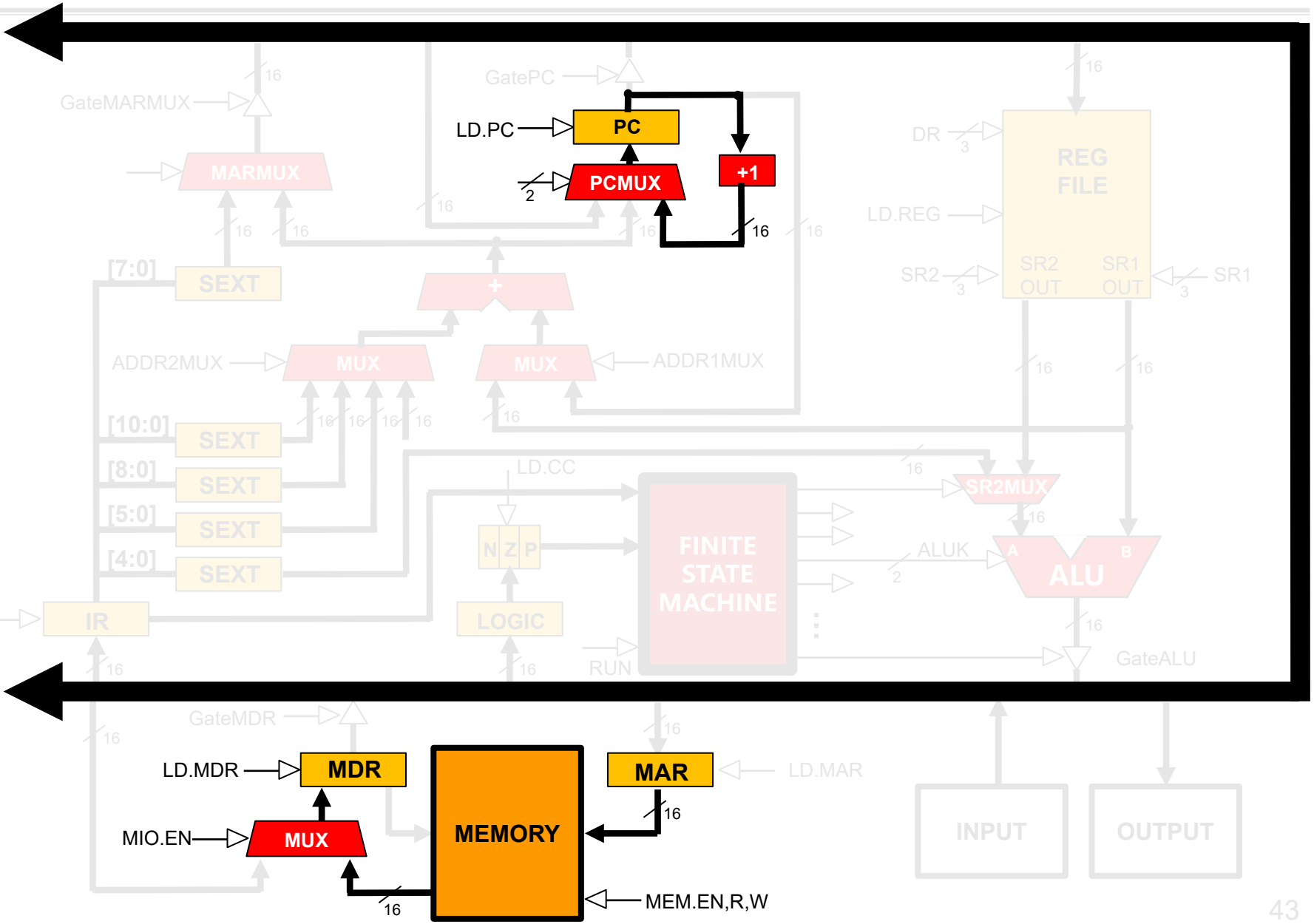

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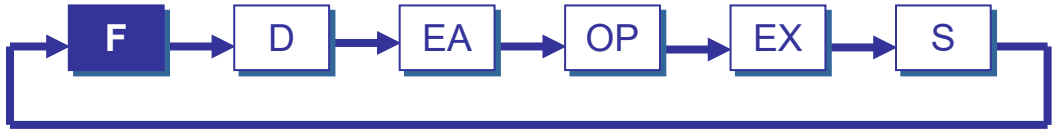

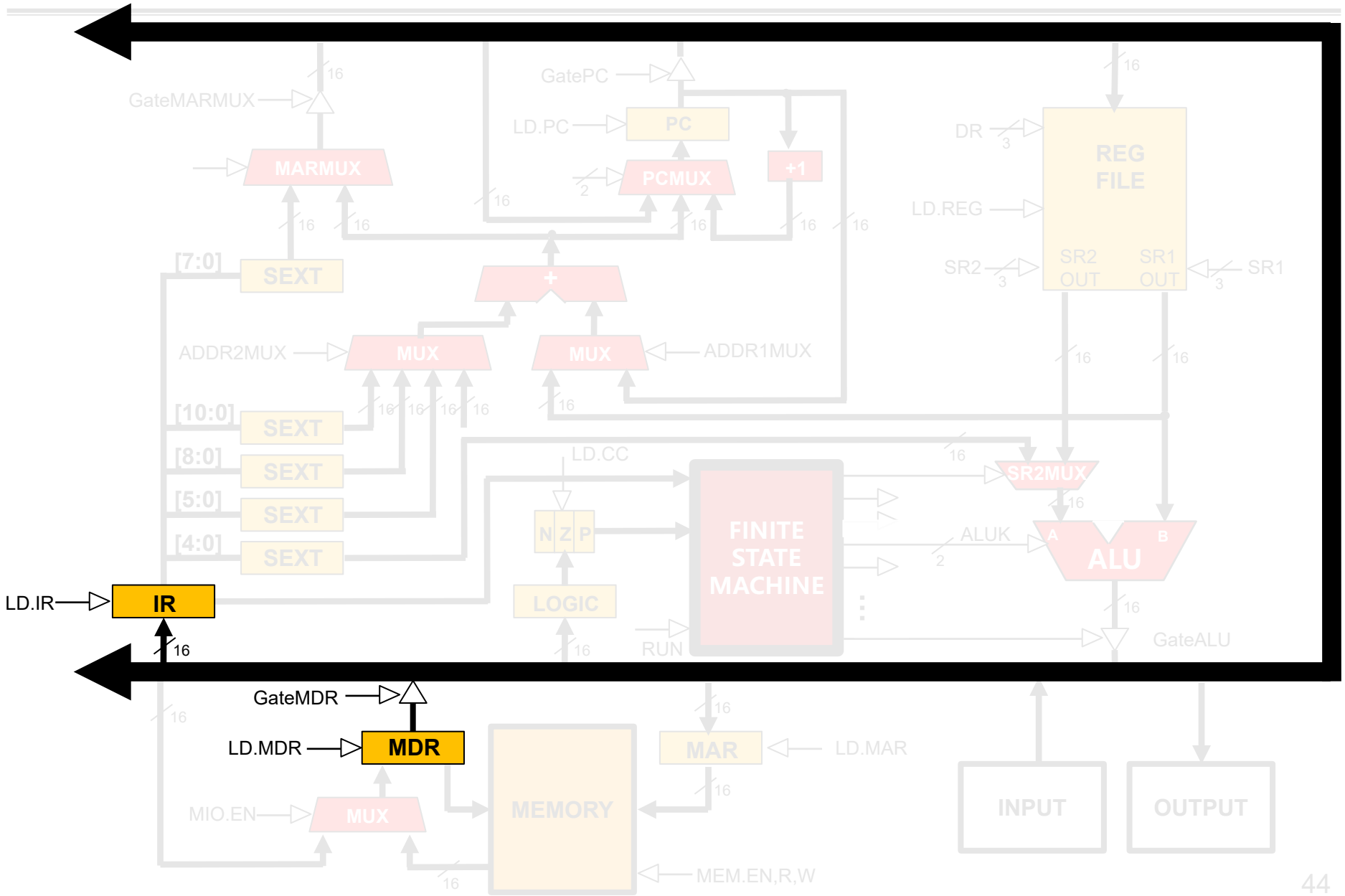

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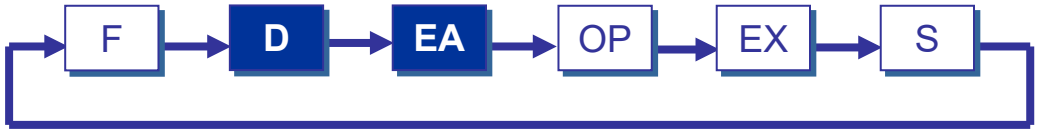

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MARMUX
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[4:0]
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LD.IR
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LD.CC
N Z P
LOGIC
FINITE STATE MACHINE
RUN
REG FILE
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3
LD.REG
SR2
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SR2 OUT
SR1 OUT
SR1
3
16
SR2MUX
ALUK
2
A
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ALU
GateALU
GatePC
LD.PC
PC
PCMUX
2
+1
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MIO.EN
MUX
MEMORY
MEM.EN,R,W
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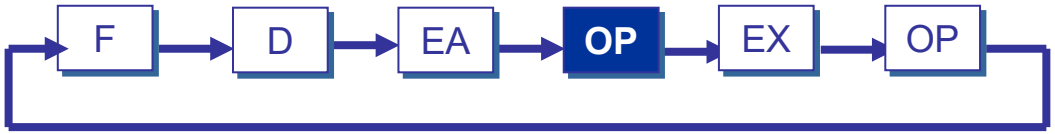
LD.MAR
INPUT
OUTPUT

STR (Base+Offset)



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MARMUX
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SEXT
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ADDR2MUX
MUX
MUX
ADDR1MUX
16
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[10:0]
SEXT
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SEXT
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IR
LD.CC
N Z P
LOGIC
FINITE STATE MACHINE
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PC
PCMUX
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LD.REG
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SR2 OUT
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SR2MUX
ALUK
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ALU
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MAR
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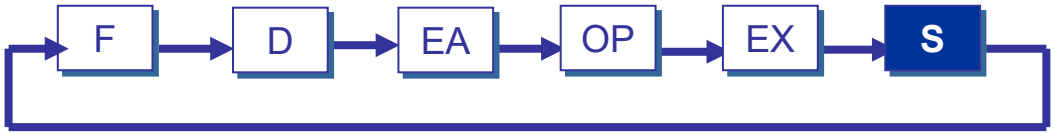
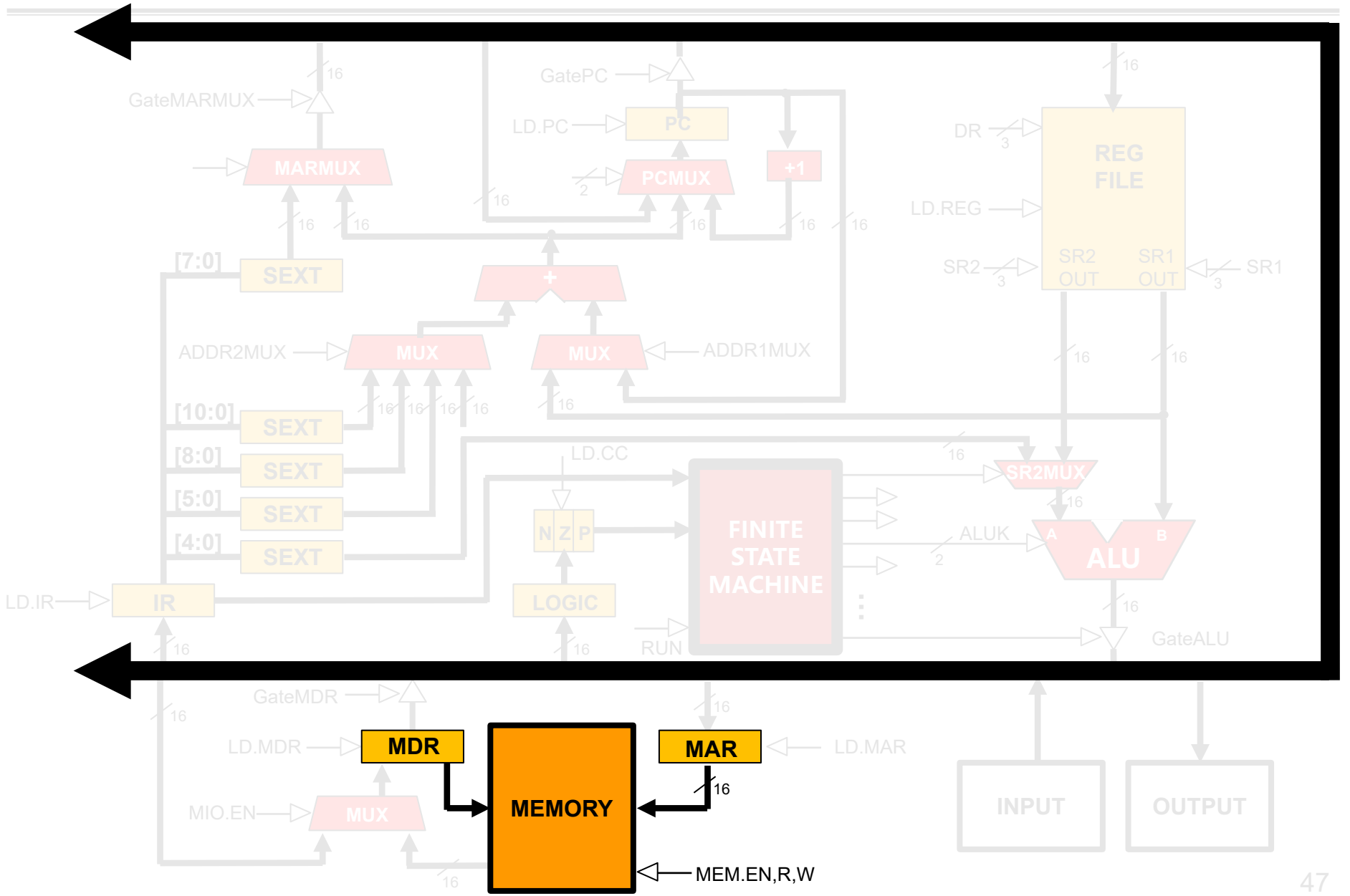
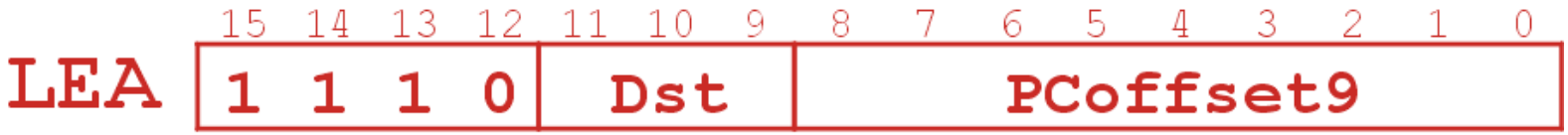
INPUT
OUTPUT
MEM.EN,R,W

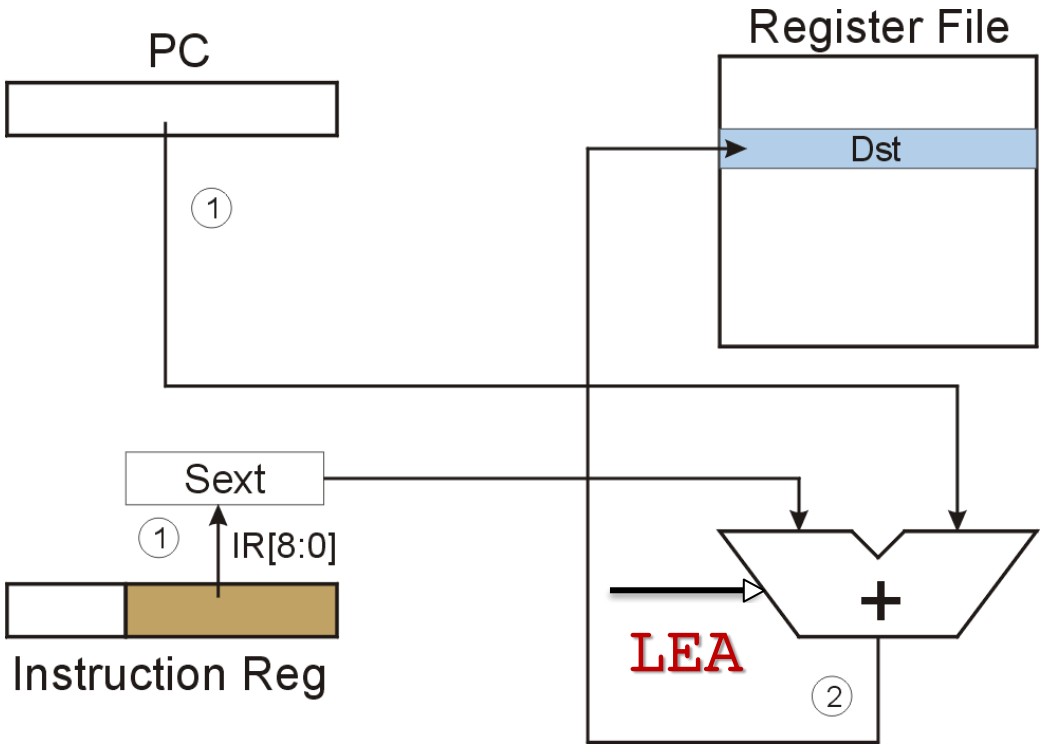
STR (Base+Offset)



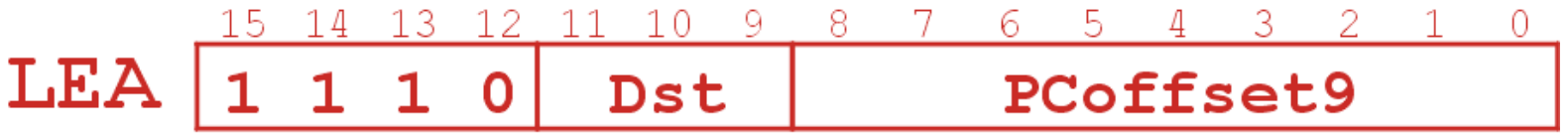


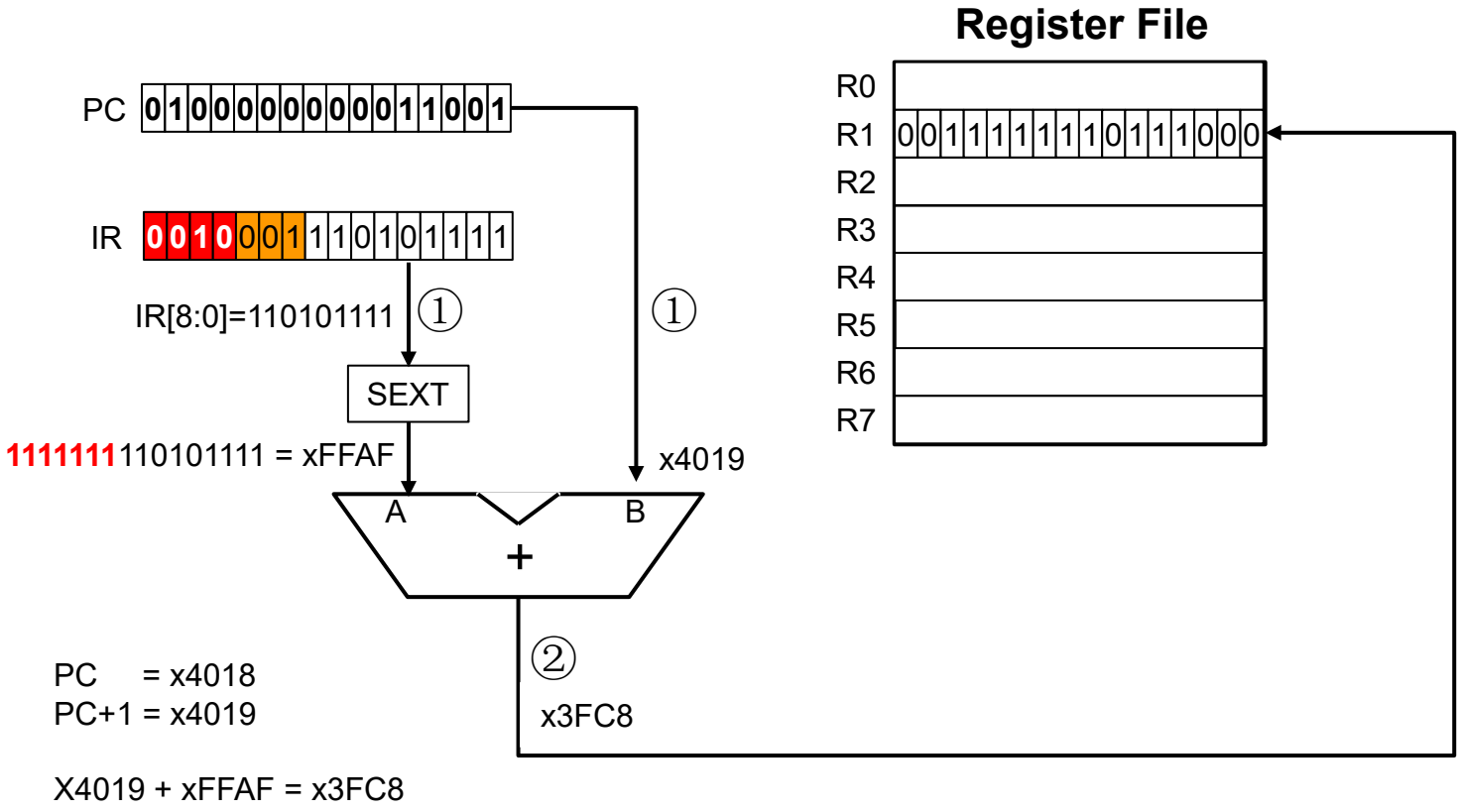
LEA (Immediate) LD DR, PCoffset9



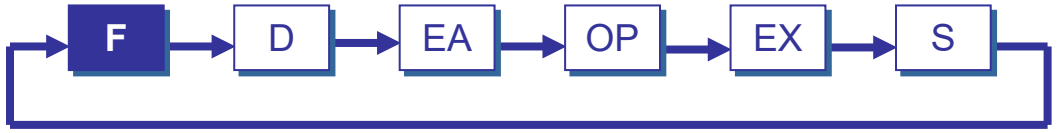


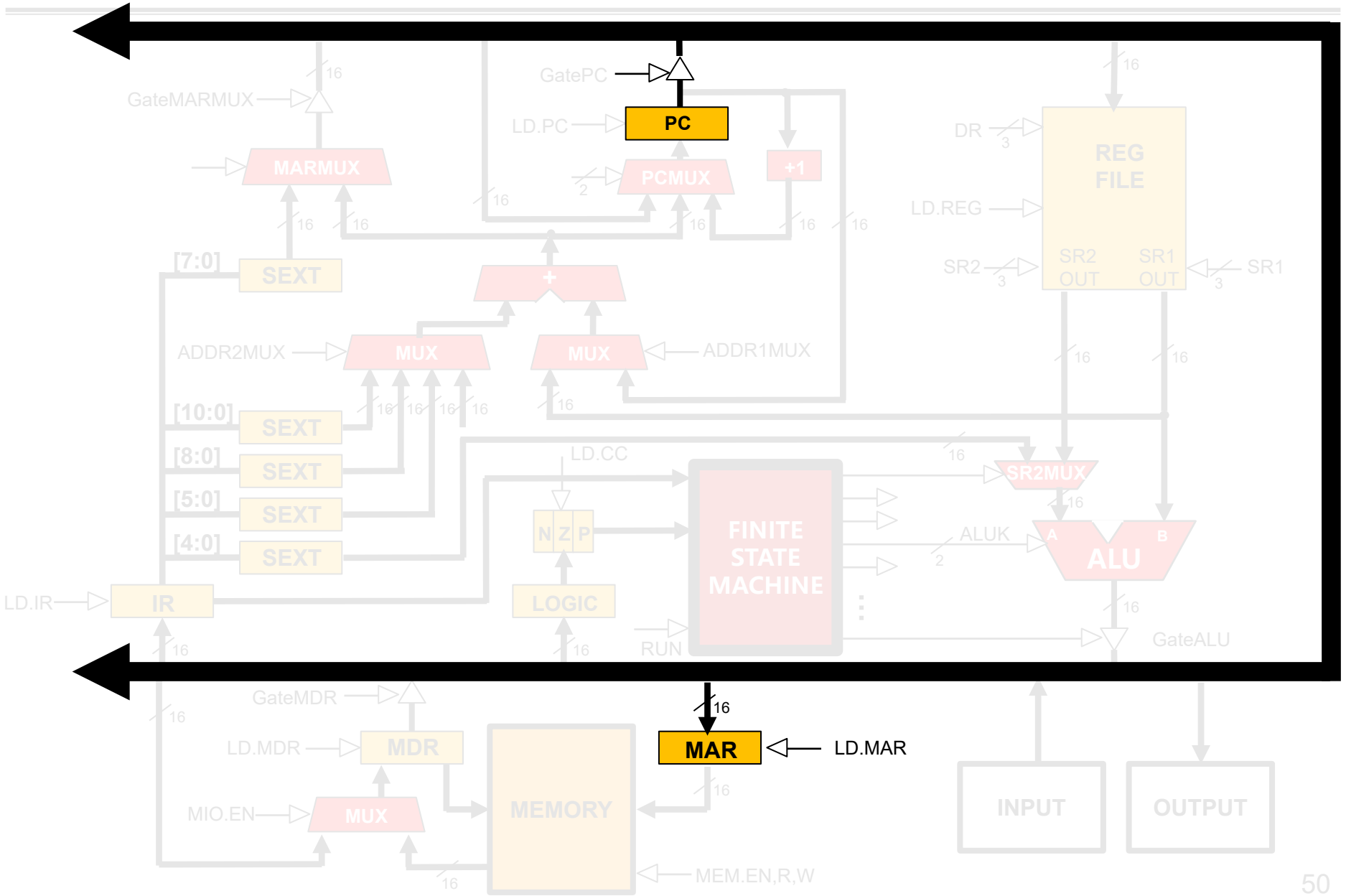
LEA (Immediate): LEA R1, x1AF



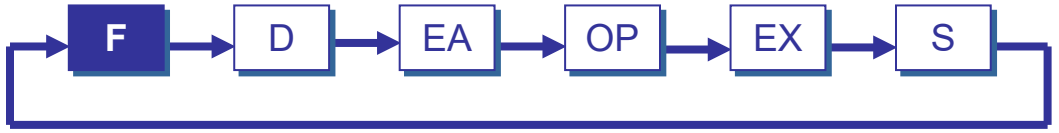


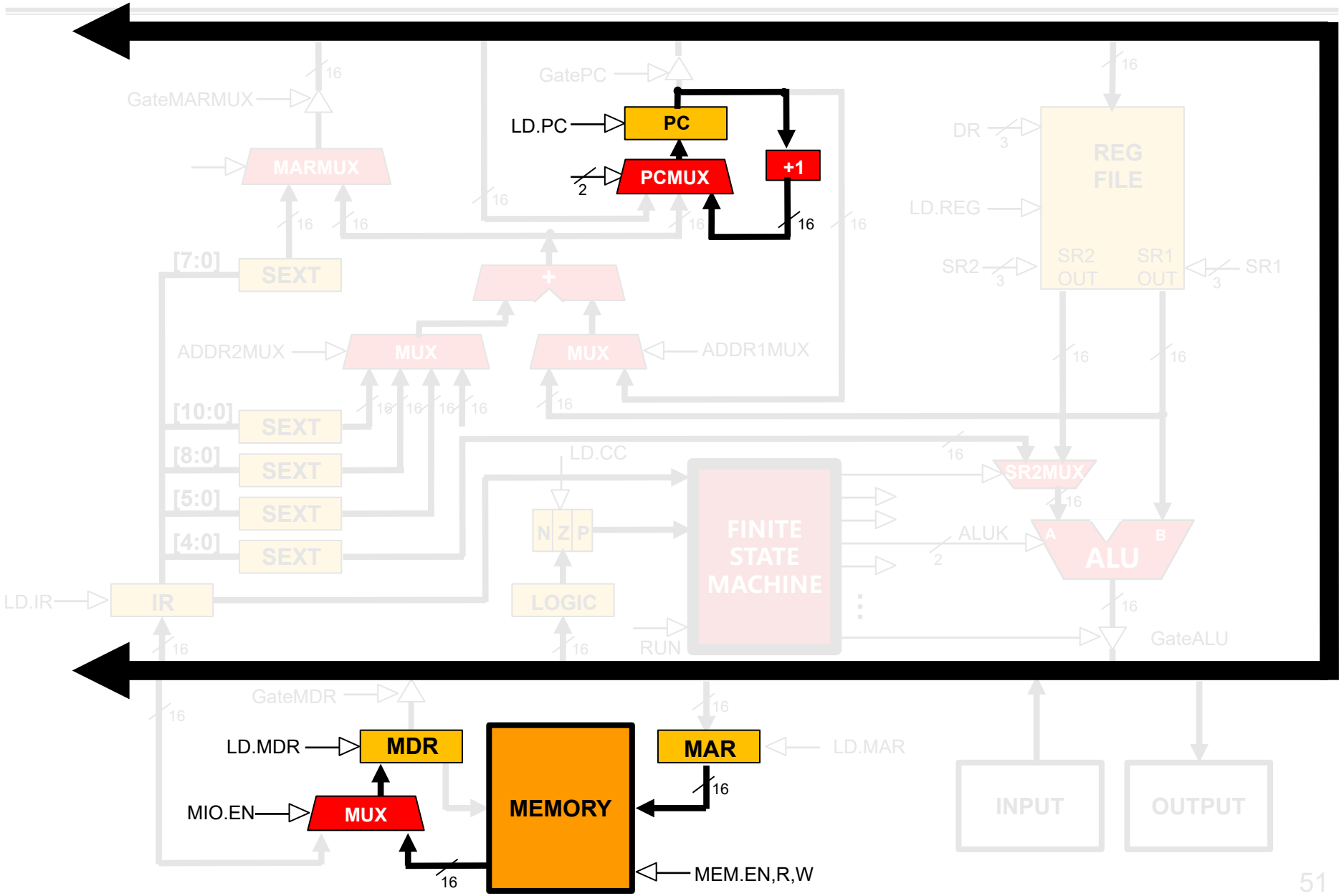
LEA (Immediate)





LEA (Immediate)





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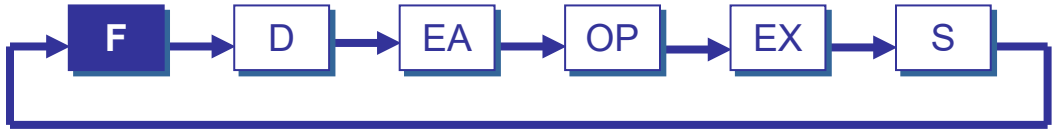

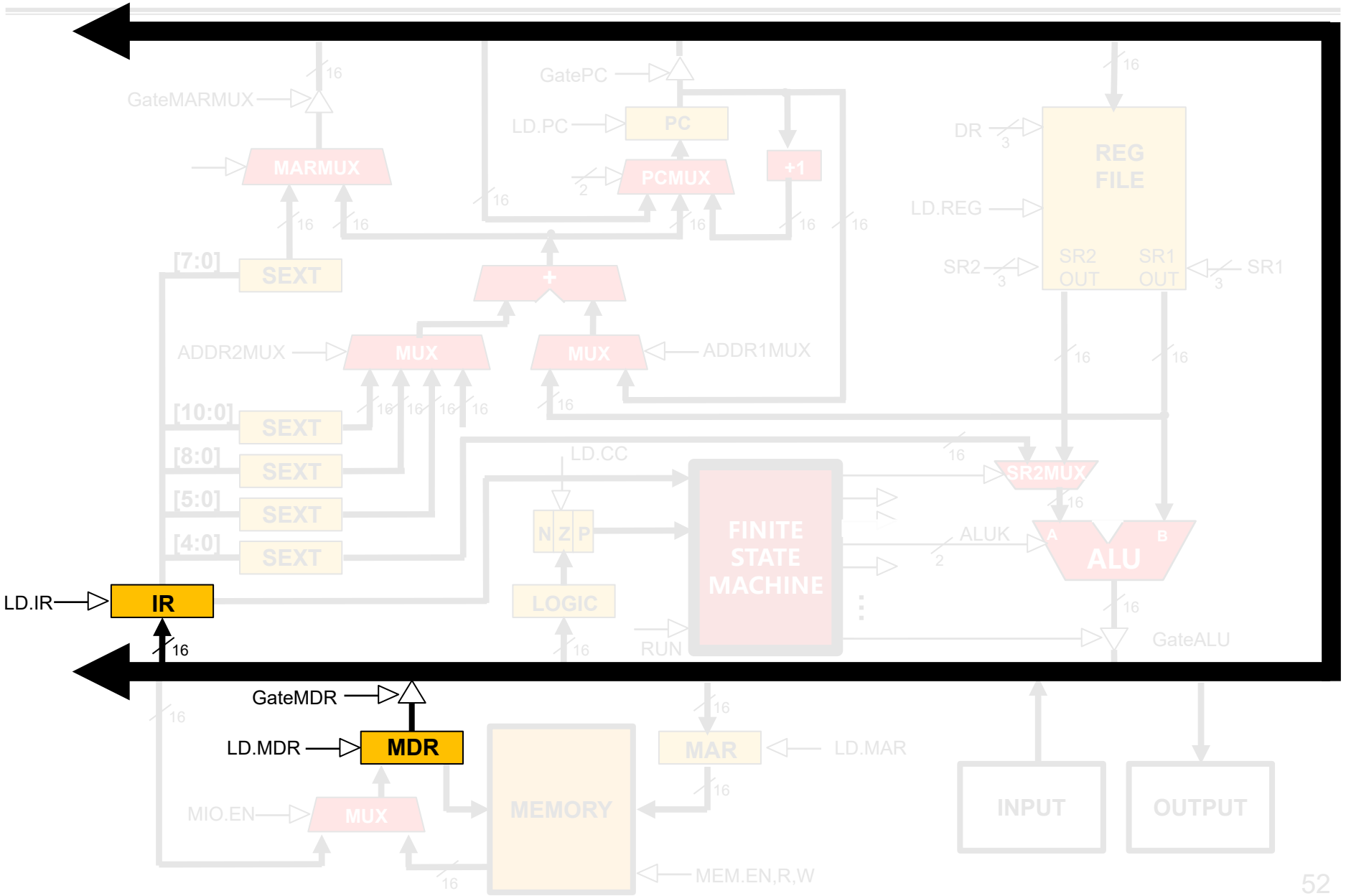

LEA (Immediate)