Ameba 1
SPI
Timing Specification

Version 1v0

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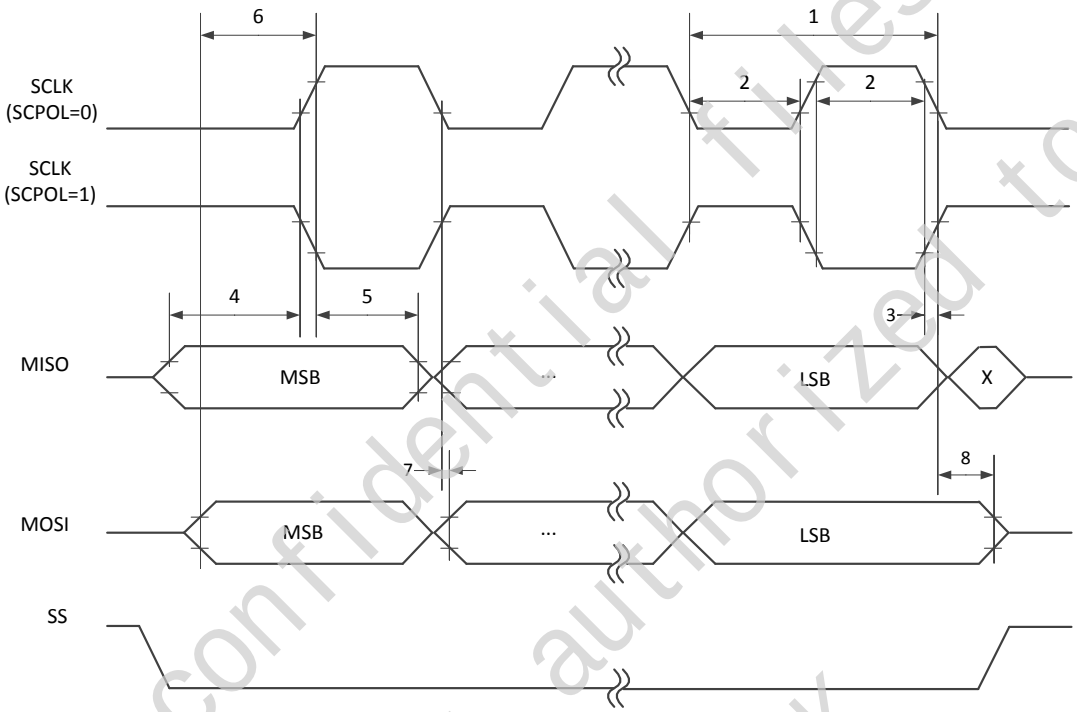
SPI Master Mode with CPU Clock 166 MHz

SCPH = 0 (Data Latch @ 1st Edge)

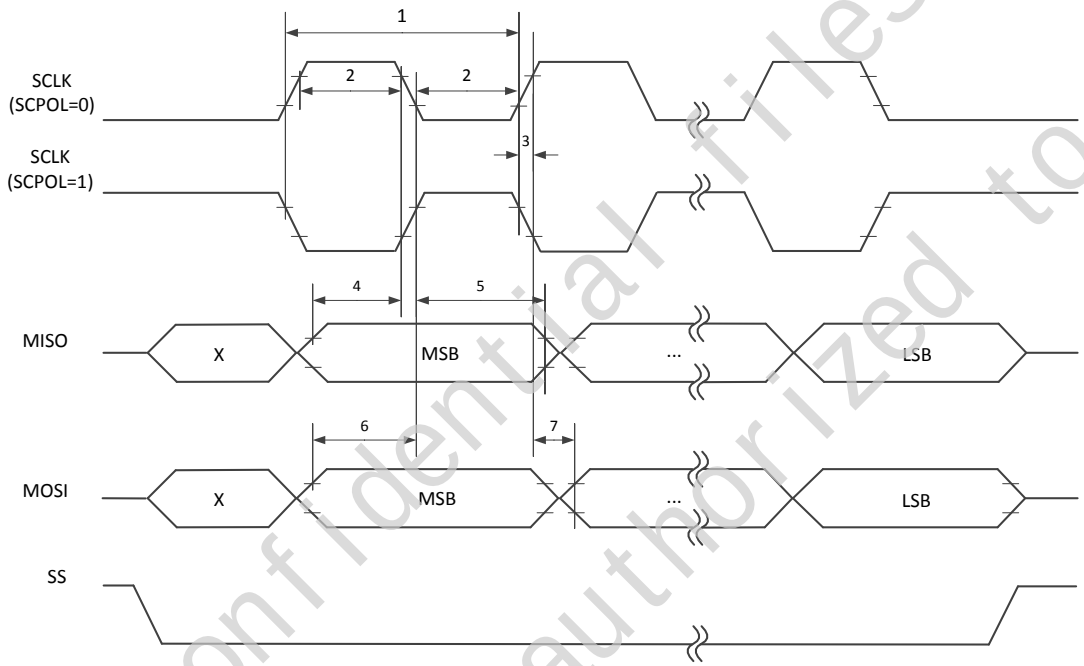


Number	Min	Typical	Max	Description
1	48 ns	--	--	SCLK Period
2	18 ns	--	--	SCLK High/Low Time
3	--	6 ns	--	SCLK Rise/Fall Time
4	10 ns	--	--	MISO Setup Time
5	5 ns	--	--	MISO Hold Time
6	3 ns	--	--	MOSI Ready before SCLK Edge
7	--	6 ns	9 ns	MOSI Valid after SCLK Edge
8	3 ns	6 ns	9 ns	MOSI Last Bit Valid Time after SCLK back to Idle State

*Timing Number 1, 2 are CPU Clock dependent. If the CPU Clock down to 83 MHz, these timing should times 2.

SPI Master Mode with CPU Clock 166 MHz

SCPH = 1 (Data Latch @ 2nd Edge)

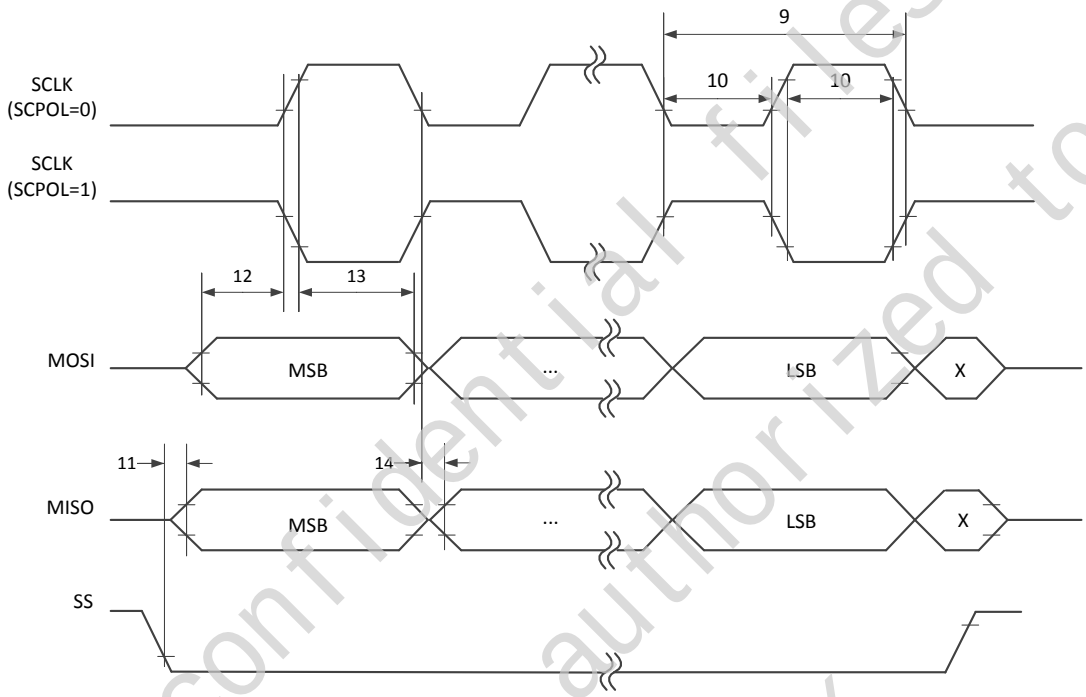


Number	Min	Typical	Max	Description
1	48 ns	--	--	SCLK Period
2	18 ns	--	--	SCLK High/Low Time
3	--	6 ns	--	SCLK Rise/Fall Time
4	10 ns	--	--	MISO Setup Time
5	5 ns	--	--	MISO Hold Time
6	3 ns	--	--	MOSI Setup Time
7	--	6 ns	9 ns	MOSI Valid after SCLK Edge

*****Timing Number 1, 2 are CPU Clock dependent. If the CPU Clock down to 83 MHz, these timing should times 2.

SPI Slave Mode with CPU Clock 166 MHz

SCPH = 0 (Data Latch @ 1st Edge)

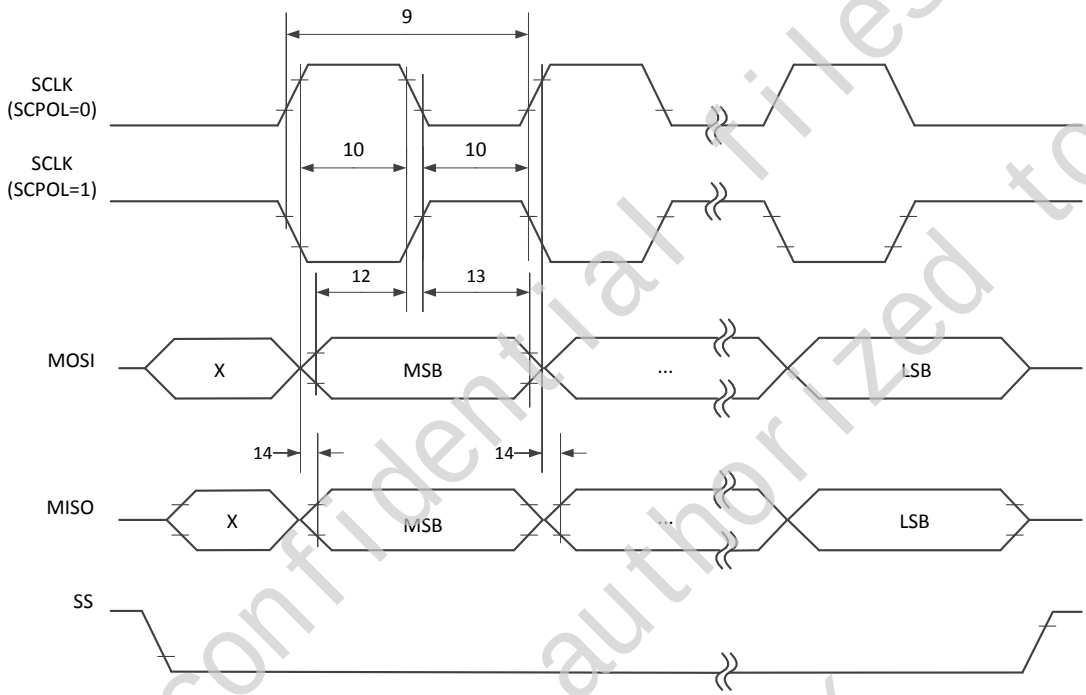


Number	Min	Typical	Max	Description
9	240 ns	--	--	SCLK Period
10	115 ns	--	--	SCLK High/Low Time
11	--	78 ns	88 ns	MISO Valid after SS Edge
12	5 ns	--	--	MOSI Setup Time
13	96 ns	--	--	MOSI Hold Time
14	--	78 ns	88 ns	MISO Valid after SCLK Edge

*Timing Number 9, 10, 11, 13, 14 are CPU Clock dependent. If the CPU Clock down to 83 MHz, these timing should times 2.

SPI Slave Mode with CPU Clock 166 MHz

SCPH = 1 (Data Latch @ 2nd Edge)



Number	Min	Typical	Max	Description
9	240 ns	--	--	SCLK Period
10	115 ns	--	--	SCLK High/Low Time
12	5 ns	--	--	MOSI Setup Time
13	96 ns	--	--	MOSI Hold Time
14	--	78 ns	88 ns	MISO Valid after SCLK Edge

*Timing Number 9, 10, 13, 14 are CPU Clock dependent. If the CPU Clock down to 83 MHz, these timing should times 2.