RTL8711AM

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RTL8711AM Data Sheet

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.1	2014/12/05	Preliminary release.

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1. General Description

Realtek RTL8711AM is a highly integrated single-chip low power 802.11n Wireless LAN (WLAN) network controller. It combines an ARM-CM3 MCU, WLAN MAC, a 1T1R capable WLAN baseband, and RF in a single chip. It also provides a bunch of configurable GPIOs which are configured as digital peripherals for different applications and control usage.

RTL8711AM integrates internal memories for complete WIFI protocol functions. The embedded memory configuration also provides simple application developments.

2. Features

General

- Package QFN56
- CMOS MAC, Baseband PHY, and RF in a single chip for 802.11b/g/n compatible WLAN
- Complete 802.11n solution for 2.4GHz band
- 72.2Mbps receive PHY rate and 72.2Mbps transmit PHY rate using 20MHz bandwidth
- 150Mbps receive PHY rate and 150Mbps transmit PHY rate using 40MHz bandwidth
- Compatible with 802.11n specification
- Backward compatible with 802.11b/g devices while operating in 802.11n mode

Standards Supported

- 802.11b/g/n compatible WLAN
- 802.11e QoS Enhancement (WMM)
- 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services
- WIFI WPS support
- WIFI Direct support
- Light Weight TCP/IP protocol

WLAN MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate High-Throughput Block Acknowledgement (HT-BA)
- Long NAV for media reservation with CF-End for NAV release
- PHY-level spoofing to enhance legacy compatibility
- Power saving mechanism

WLAN PHY Features

- 802.11n OFDM
- One Transmit and one Receive path (1T1R)
- 20MHz and 40MHz bandwidth transmission

- Short Guard Interval (400ns)
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM, and 640QAM modulation. Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6
- Maximum data rate 54Mbps in 802.11g and 150Mbps in 802.11n
- Fast receiver Automatic Gain Control (AGC)
- On-chip ADC and DAC

Peripheral Interfaces

- SDIO 2.0 SDR25 supported
- Maximum 2 high speed UART interface with baud rate up to 4MHz
- 1 log UART with standard baud rate support
- Maxumum 3 I^2C interface
- I^2S with 8/16/32/48/44.1 KHz sampling rate
- PCM with 8/16KHz sample rate
- Maximum 2 SPI supported. One supports baud rate up to 41.5MHz; the other one supports baud rate up to 15MHz.
- Support 4 PWM with configurable duration and duty cycle from 0 ~ 100%
- Support External Timer Trigger Event (ETE function) with configurable period in low power mode
- Maximum 21 GPIO pins

3. Block Diagram

3.1. Functional Block Diagram

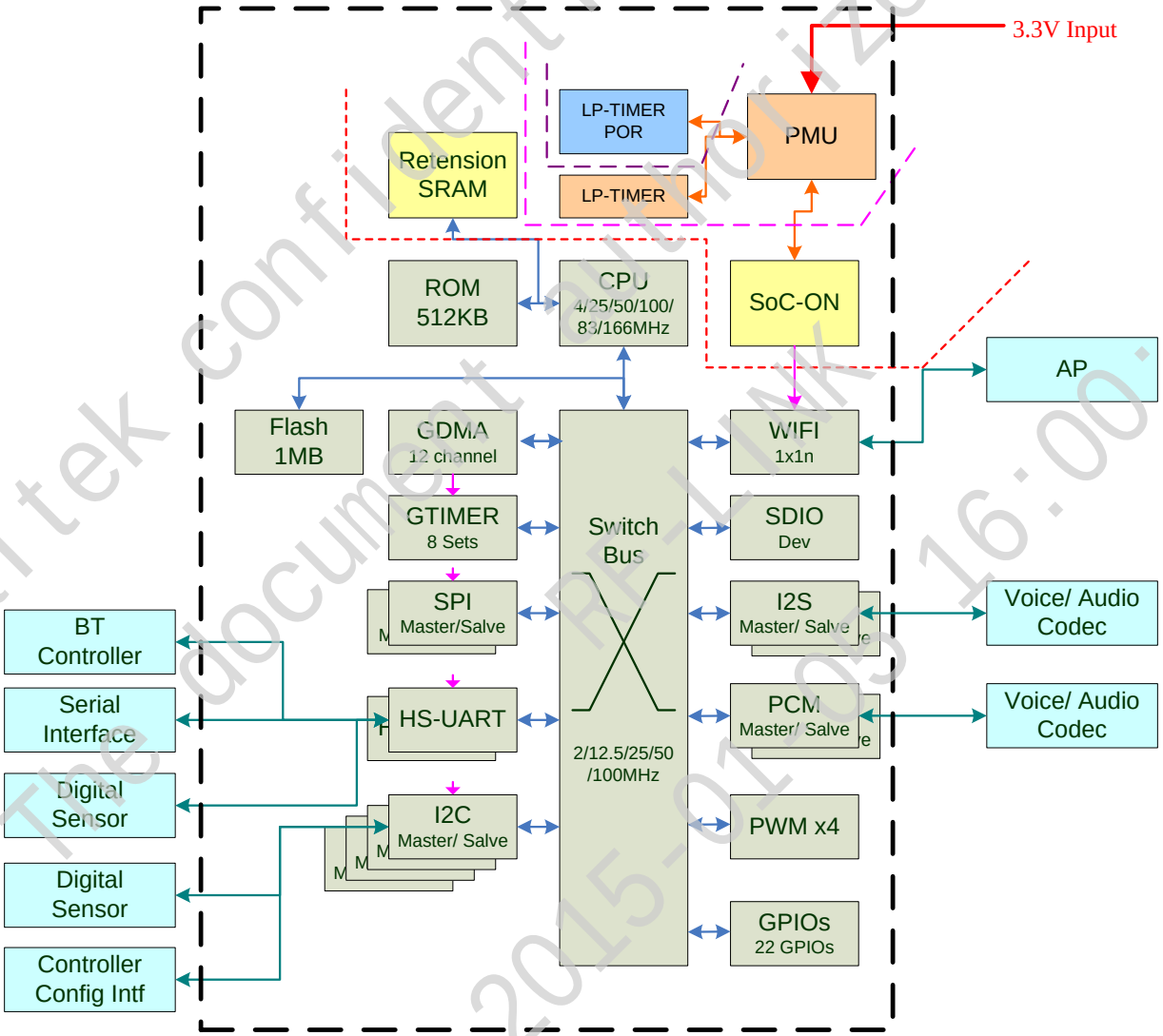


Figure 1. Block Diagram

3.2. WIFI and NFC Application Diagram

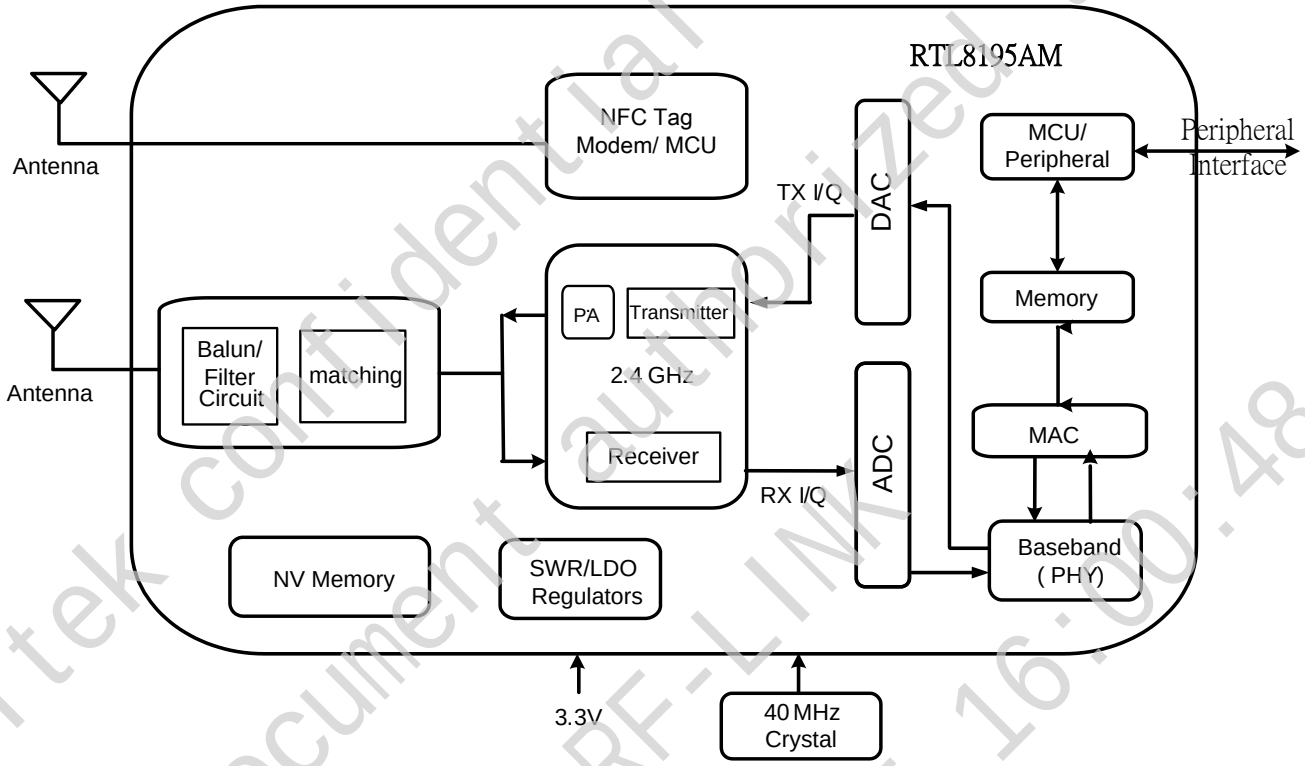


Figure 2. Single-Band 11n (1x1) and NFC Tag Solution

3.3. Power Supply Application Diagram

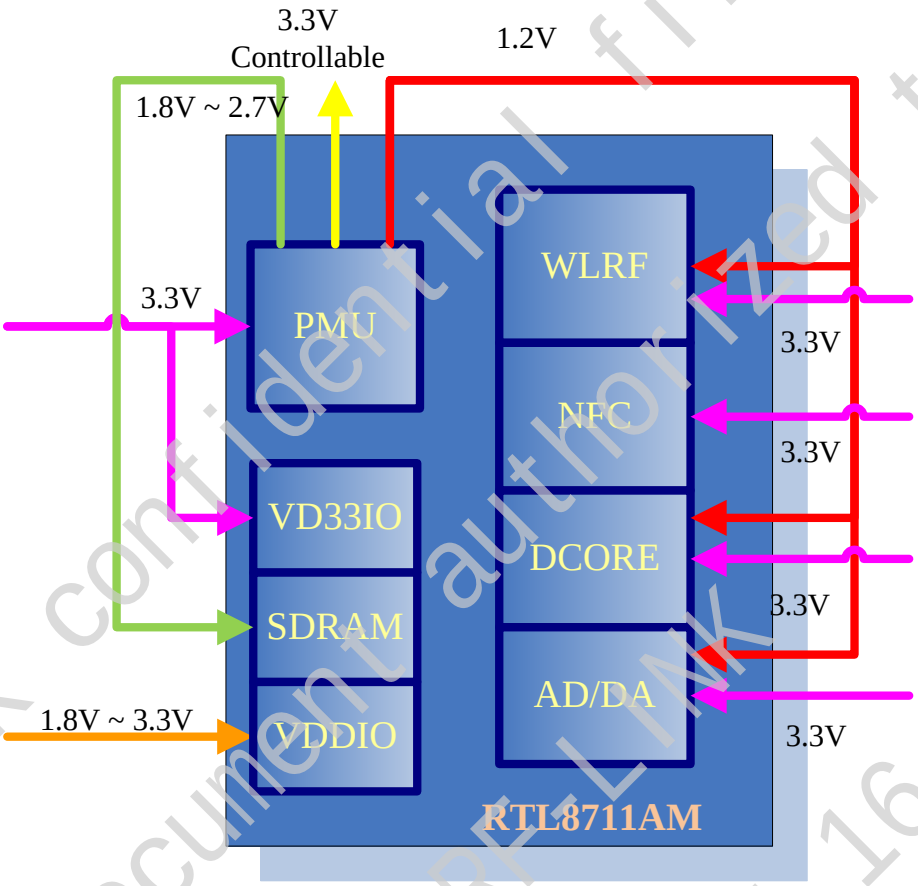


Figure 3. Power Supply Architecture

The integrated Power Management Unit (PMU) provides the following features:

- 1.2V power bulk or LDO selectable.
- 1.8~2.7V LDO
- 3.3V power source integrated power cut controlled by FW.

4. Memory Mapping

4.1. Programming Space

Name	Mode	Physical	Size	IP Function
Code		0x0000_0000 0x000F_FFFF	768KB	Instruction Memory (ROM)
		0x1000_0000 0x1006_FFFF	448KB	Inter SRAM: BD SRAM and Buffer SRAM share total 448KB physical sram
		0x1FFF_0000 0x1FFF_FFFF	64KB	TCM (Tightly-Coupled Memory) SRAM
SRAM		0x3000_0000 0x33FF_FFFF	64MB	SDR SDRAM memory

4.2. IO Space

Name	Mode	Physical Address	Size	IP Function
Peripheral		0x4000_0000	4KB	SYS Control (SYSON)
		0x4000_0FFF		
		0x4000_1000	2KB	GPIO Control
		0x4000_17FF		
		0x4000_1800		RSVD
		0x4000_1FFF		
		0x4000_2000	4KB	Timer Control
		0x4000_2FFF		
		0x4000_3000	1KB	UART for Log
		0x4000_33FF		
		0x4000_3400	1KB	I2C_2 Control
		0x4000_37FF		
		0x4000_3800	1KB	I2C_3 Control
		0x4000_3BFF		
		0x4000_3C00		RSVD
		0x4000_4FFF		
		0x4000_5000	4KB	SDR SDRAM controller
		0x4000_5FFF		
		0x4000_6000	4KB	SPI flash controller
		0x4000_6FFF		
		0x4000_7000		RSVD
		0x4000_FFFF		
		0x4001_0000	4KB	ADC
		0x4001_0FFF		
		0x4001_1000	4KB	DAC
		0x4001_1FFF		

Name	Mode	Physical Address	Size	IP Function
Peripheral		0x4004_0000	1KB	UART_0 Control
		0x4004_03FF		
		0x4004_0400	1KB	UART_1 Control
		0x4004_07FF		
		0x4004_0800	1KB	UART_2 Control
		0x4004_0BFF		
		0x4004_0C00		RSVD
		0x4004_1FFF		
		0x4004_2000	1KB	SPI_0 Control
		0x4004_23FF		
		0x4004_2400	1KB	SPI_1 Control
		0x4004_27FF		
		0x4004_2800	1KB	SPI_2 Control
		0x4004_2BFF		
		0x4004_2C00		RSVD
		0x4004_3FFF		
		0x4004_4000	1KB	I2C_0 Control
		0x4004_43FF		
		0x4004_4400	1KB	I2C_1 Control
		0x4004_47FF		
		0x4004_4800		RSVD
		0x4004_FFFF		

Name	Mode	Physical Address	Size	IP Function
Peripheral		0x4005_0000 0x4005_3FFF	16KB	SDIO Device / GMAC
		0x4005_4000 0x4005_7FFF		RSVD
		0x4005_8000 0x4005_BFFF	16KB	SDIO Host
		0x4005_C000 0x4005_FFFF		RSVD
		0x4006_0000 0x4006_07FF	2KB	GDMA0
		0x4006_0800 0x4006_0FFF	2KB	RSVD for other DMA
		0x4006_1000 0x4006_17FF	2KB	GDMA1
		0x4006_1800 0x4006_1FFF		RSVD for other DMA

Name	Mode	Physical Address	Size	IP Function
Peripheral		0x4006_2000	1KB	I2S_0 Control
		0x4006_23FF		
		0x4006_2400	3KB	RSVD
		0x4006_2FFF		
		0x4006_3000	1KB	I2S_1 Control
		0x4006_33FF		
		0x4006_3400	3KB	RSVD
		0x4006_3FFF		
		0x4006_4000	1KB	PCM_0 Control
		0x4006_43FF		
		0x4006_4400		RSVD
		0x4006_4FFF		
		0x4006_5000	1KB	PCM_1 Control
		0x4006_53FF		
		0x4007_0000	16KB	Security Engine
		0x4007_3FFF		
		0x4007_4000	48KB	RSVD
		0x4007_FFFF		
		0x4008_0000	256KB	WIFI REG & TX/RX FIFO direct map
		0x400B_FFFF		
		0x400C_0000	256KB	USB OTG REG & DATA FIFO direct map
		0x400F_FFFF		
		0x403F_FFFF	1MB	RSVD

4.3. Extension Memory Space

Name	Mode	Physical Address	Size	IP Function
Flash		0x9800_0000 0x9BFF_FFFF	64MB	External flash memory

5. Pin Assignments

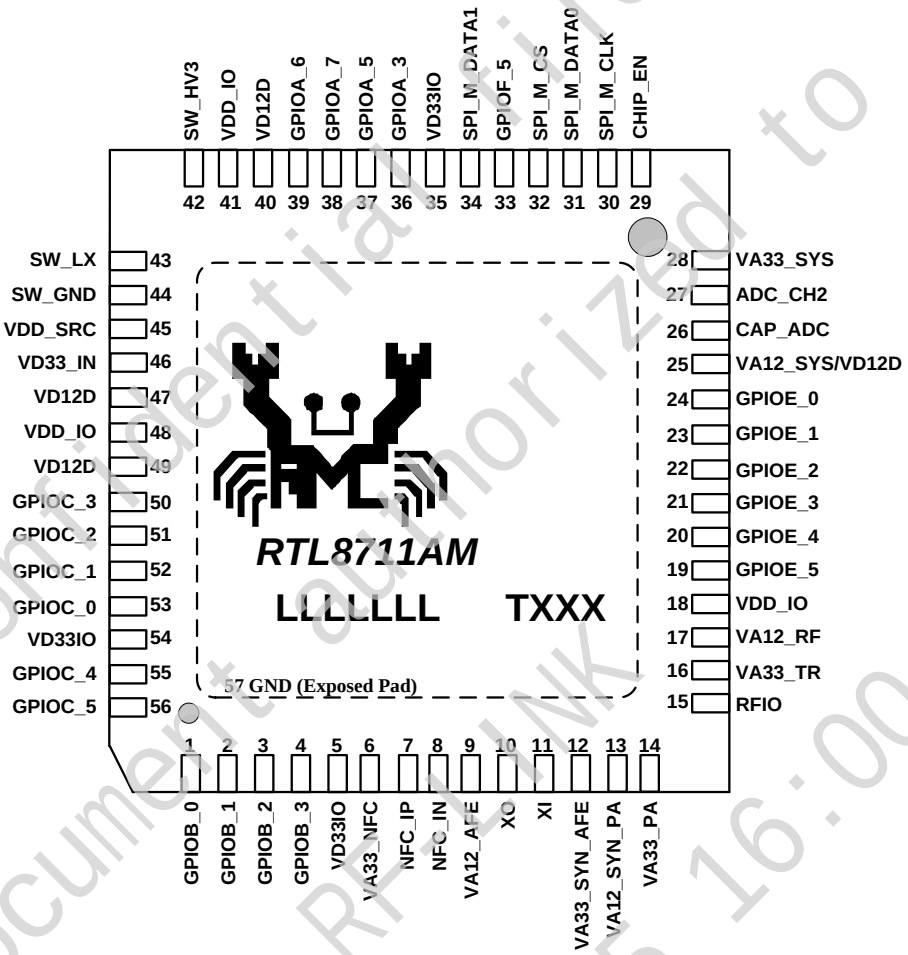


Figure 4. Pin Assignments

5.1. Package Identification

“Green” package is indicated by a ‘G’ in the location marked “T” in Figure 2.

6. Pin Descriptions

The following signal type codes are used in the tables:

I:	Input	O:	Output
T/S:	Tri-State bi-directional input/output pin	S/T/S:	Sustained Tri-State
O/D:	Open Drain	P:	Power pin

6.1. Power On Trap Pin

Table 1. Power On Trap Pins

Symbol	Type	Pin No	Description
CHIP_EN	I	29	1: enable chip 0: disable chip in shutdown mode
NORMAL_MODE_SEL	I	3	Shared with GPIOB_2 1: Normal operation mode 0: Enter into test/debug mode
SPS_LDO_SEL	I	NC	Shared with GPIOF_4 0: Internal switching regulator select 1: Internal LDO select
BOOT_SCENARIO	I	1	0: booting from internal memory 1: booting from flash
EEPROM_SEL	I	33	Shared with GPIOF_5 0: Internal NV memory select 1: External EEPROM select

Symbol	Type	Pin No	Description
SD_DEV_SEL	I	38	Shared with GPIOA_7 1: SDMMC Host mode 0: SDIO device mode
ICFG0	I	53	Shared with GPIOC_0 When NORMAL_MODE_SEL is “1”, then ICFG0 is test mode BIT0.
ICFG1	I	52	Shared with GPIOC_1 When NORMAL_MODE_SEL is “1”, then ICFG0 is test mode BIT1.
ICFG2	I	51	Shared with GPIOC_2 When NORMAL_MODE_SEL is “1”, then ICFG0 is test mode BIT2.
ICFG3	I	50	Shared with GPIOC_3 When NORMAL_MODE_SEL is “1”, then ICFG0 is test mode BIT3.

6.2. Analog to DC Converter

Table 2. ADC Pins

Symbol	Type	Pin No	Description
ADC_CH2	I	27	AD converter input
CAP_ADC	P	26	Capacitor for AD converter power.

6.3. RF and FC

Table 3. RF and NFC Pins

Symbol	Type	Pin No	Description
NFC_IP	I	7	NFC input differential signal
NFC_IN	I	8	NFC input differential signal
RF_IO	IO	15	WL RF signal

6.4. Power Pins

Table 4. Power Pins

Symbol	Type	Pin No	Description
SW_LX	P	43	Switching Regulator Output
SW_HV3	P	42	Switching Regulator Input Or Linear Regulator input from 3.3V to 1.5V
VA33	P	6, 12, 14, 16, 28,	3.3V for Analog Circuit
VD33IO	P	5, 35	VDD3.3V for Digital IO
VDD_IO	P	18, 36	GPIOE and GPIOC group IO power
VDD_IO	P	41, 48	Embedded SDR DRAM power
VD12D	P	24, 40, 47, 49	VDD 1.2V Digital Circuit
VA12	P	9, 13, 17, 25	1.2V for analog blocks
SW_GND	P	44	Switching Regulator Ground

6.5. Clock Pins

Table 5. Clock and Other Pins

Symbol	Type	Pin No	Description
XI	I	11	40MHz OSC Input Input of 40MHz Crystal Clock Reference
XO	O	10	Output of 40MHz Crystal Clock Reference

6.6. NOR Flash Interface

Table 6. NOR Flash Pins

Symbol	Type	Pin No	Description
SPI_MCLK	IO	30	NOR Flash CLK signal. Multiplexed with GPIOF_1 .
SPI_DATA0	IO	31	NOR Flash CLK signal. Multiplexed with GPIOF_2 .
SPI_CS	IO	32	NOR Flash CLK signal. Multiplexed with GPIOF_0 .
SPI_DATA1	IO	34	NOR Flash CLK signal. Multiplexed with GPIOF_3 .

6.7. Digital IO Pins

Please refer to section 6 Pin Function Table for more detailed information.

Table 7. GPIO Pins

Symbol	Type	Pin No	Description
GPIOB_0	IO	1	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOB_1	IO	2	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOB_2	IO	3	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOB_3	IO	4	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOE_0	IO	23	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOE_1	IO	22	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOE_2	IO	21	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOE_3	IO	20	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOE_4	IO	19	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOA_3	IO	36	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOA_5	IO	37	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOA_7	IO	38	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOA_6	IO	39	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOC_0	IO	53	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOC_1	IO	52	GPIO pin. The MUX function can be referred to Pin Function Table.

Symbol	Type	Pin No	Description
GPIOC_2	IO	51	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOC_3	IO	50	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOB_4	IO	55	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOB_5	IO	56	GPIO pin. The MUX function can be referred to Pin Function Table.

7. Pin Function Table

7.1. Pin Configurable Function Group Summary Table

Table 8. Pin Function Group Table

PIN name	JTAG	UART Funtion	I2C Group	SPI Group	I2S GROUP	PCM Group	WL_LED0	PWM0 GR	ETE Group
GPIOA_3									
GPIOA_5									
GPIOA_6		UART0_IN							
GPIOA_7		UART0_OUT/ UART2_OUT							
GPIOB_0		UART_LOG_OUT							ETE0
GPIOB_1		UART_LOG_IN					WL_LED0		ETE1
GPIOB_2									ETE2
GPIOB_3									
GPIOC_0		UART0_IN		SPI0_CS0	I2S1_WS			PWM0	ETE0
GPIOC_1		UART0_CTS		SPI0_CLK	I2S1_CLK			PWM1	ETE1
GPIOC_2		UART0_RTS		SPI0_MOSI	I2S1_SD_TX			PWM2	ETE2
GPIOC_3		UART0_OUT		SPI0_MISO	I2S1_MCK			PWM3	ETE3
GPIOC_4			I2C1_SDA	SPI0_CS1	I2S1_SD_RX				
GPIOC_5			I2C1_SCL	SPI0_CS2	I2S0_SD_RX				
GPIOE_0	JTAG_TRST	UART0_OUT	I2C2_SCL	SPI0_CS0	I2S0_WS	PCM0_SYNC		PWM0	
GPIOE_1	JTAG_TDI	UART0_RTS	I2C2_SDA	SPI0_CLK	I2S0_CLK	PCM0_CLK		PWM1	
GPIOE_2	JTAG_TDO	UART0_CTS	I2C3_SCL	SPI0_MOSI	I2S0_SD_TX	PCM0_OUT		PWM3	
GPIOE_3	JTAG_TMS	UART0_IN	I2C3_SDA	SPI0_MISO	I2S0_MCK	PCM0_IN			
GPIOE_4	JTAG_CLK		I2C3_SCL	SPI0_CS1	I2S1_WS				
GPIOE_5			I2C3_SDA	SPI0_CS2	I2S1_CLK				

8. Functional Description

8.1. Power Management Control Unit

8.1.1. Features

The PMU provides the following functions:

- Bulk/LDO to output 1.2V
- LDO to output 1.8V ~ 2.5V power source
- Integrated power cut to output Vref (input from VD33_IN) with SW controllable
- 2 very Low power clock source with less accuracy: 1K and 500K
- 1 low power 32.768KHz clock source with moderate accuracy
- Wakeup system detector to resume from low power state

8.1.2. Power Mode and Specification

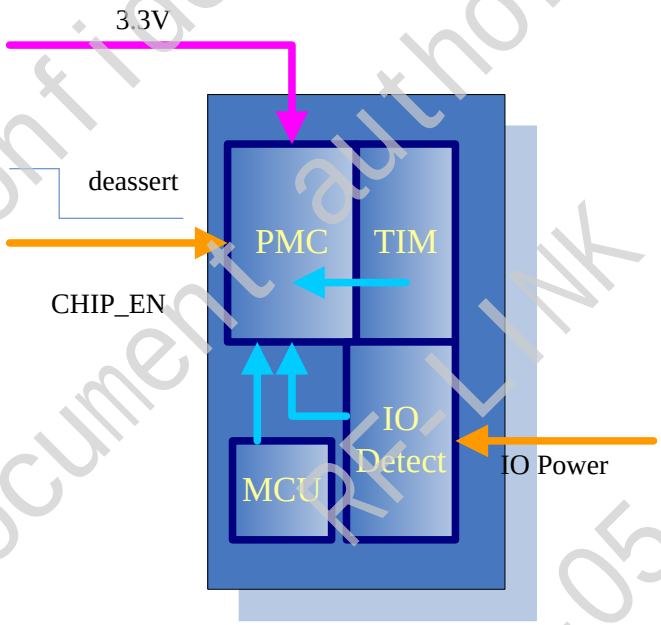
Table 9. Power Mode Brief Summary and Typical Power Consumption and Resume Time

Parameter	Power Consumption			Resume Time		
	Typical	Maximum	Units	Typical	Maximum	Units
Shutdown Mode	[TBD]	[TBD]	uA	[TBD]	[TBD]	ms
Deep Sleep Mode	[TBD]	[TBD]	uA	[TBD]	[TBD]	ms
Deep Standby Mode	[TBD]	[TBD]	uA	[TBD]	[TBD]	ms
Sleep Mode1	[TBD]	[TBD]	uA	[TBD]	[TBD]	ms
Sleep Mode2	[TBD]	[TBD]	uA	[TBD]	[TBD]	ms

8.1.3. Power Mode Description

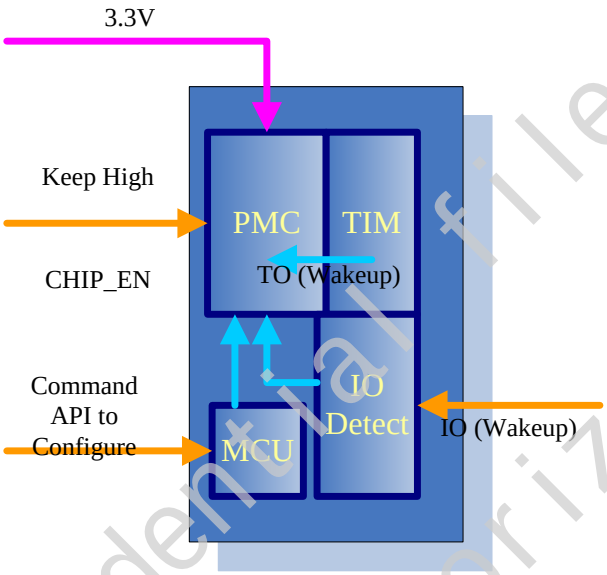
8.1.3.1 Shutdown Mode

CHIP_EN deasserts to shutdown whole chip without external power cut components required.



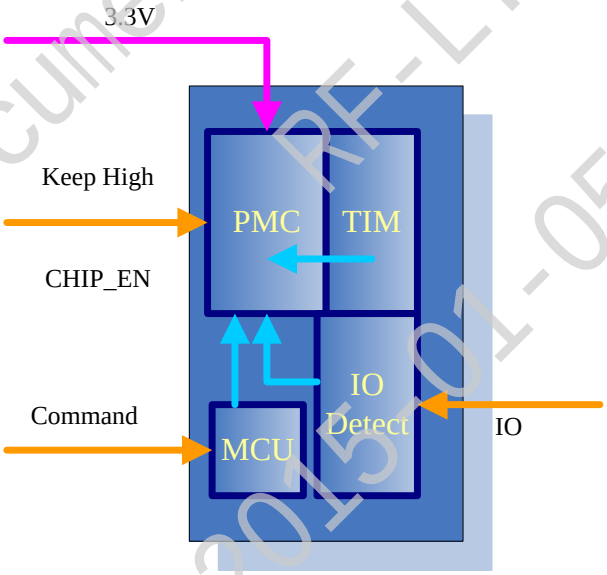
8.1.3.2 Deep Sleep Mode

CHIP_EN keeps high. Enter into Deep Sleep mode by API. The trigger timer period can be configured or GPIOB_0 can be used as external trigger event. The DLSP trigger timer can be configured with the range 1 ~ 3600 sec.



8.1.3.3 Deep Standby Mode

CHIP_EN keeps high. Entering into Deep Sleep mode by API. The trigger timer period can be configured or all GPIO group can be used as external trigger event.



8.1.3.4 Sleep Mode 1 and 2

[TBD]

8.1.4. Power On Sequence (Power On or Resume from Deep Sleep)

[TBD]

Figure 5. UART Power-On Sequence Without Hardware Flow Control

8.1.5. Power On Sequence (Power On or Resume from Deep Sleep)

[TBD]

Figure 6. UART Power-On Sequence Without Hardware Flow Control

8.1.6. Resume from Deep Standby

[TBD]

Figure 7. UART Power-On Sequence Without Hardware Flow Control

8.2. Memory System

8.2.1. Memory Architecture

RTL8711A integrates ROM, internal SRAM, extended SDR DRAM, extended NOR flash to provide applications with a variety of memory requirements.

8.2.2. Internal ROM

RTL8711A integrates 512KB ROM to provide high access speed, low leakage memory. The ROM memory clock speed is up to 166MHz. The ROM lib provides the following functions:

- Boot Code and MCU initialization
- Default UART driver
- Non-flash booting functions and drivers
- Peripheral libraries
- Security function libraries

8.2.3. Internal SRAM

448KB SRAM is integrated to provide instruction, data, and buffer usage. The maximum clock speed is up to 166MHz.

Additional 64KB fast access data memory (TCM) is provided for FW data section. The range is 0x1FFF-0000 ~ 0x1FFF-FFFF.

8.2.4. Extended SDR DRAM

8.2.4.1 Features

- Interface (Bus Width): 16-bit

- Targeted SDR Frequency: Up to 83MHz
- Supports one Chip Select (MCS0#) and 1 Band select (BA0)

8.2.4.2 SDR DRAM Input Timing

Table 10. SDR DRAM Input Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
T_{SETUP}	Input Setup Prior to Rising Edge of Clock Inputs included in this timing are MD[15:0] (during a read operation)	-	1.13	-	ns
T_{HOLD}	Input Hold Time after the Rising Edge of Clock Inputs included in this timing are MD[15:0] (during a read operation)	-	0	-	ns

Note: The RTL8196EU integrates some timing controls on the interface. Here the timing parameters listed in the table are extracted in the default situation (without specific controls).

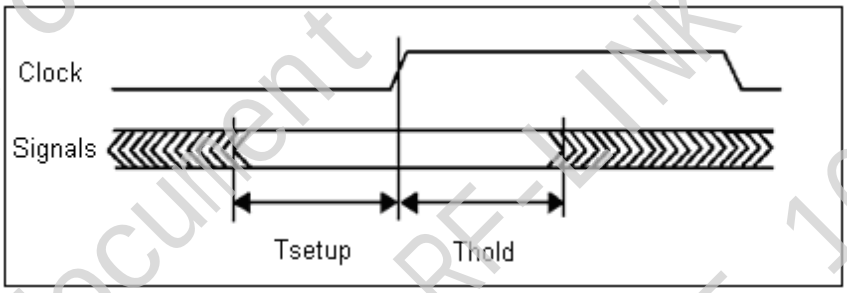


Figure 8. SDR DRAM Input Timing

8.2.4.3 SDR DRAM Output Timing

Table 11. SDR DRAM Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
$T_{CLK2OUT}$	Rising Edge of Clock-to-Signal Output Outputs include this timing are MD[15:0], MCS0#, MCS1#, RAS#, CAS#, LDQM, UDQM, WE# (during a write operation)	-	-	2.3	ns
$T_{HOLDOUT}$	Signal Output Hold Time after the Rising Edge of the Clock Outputs included in this timing are MD[15:0] (during a write operation)	0.8	-	-	ns

Note: Timing was tested with 75-pF capacitor to ground.

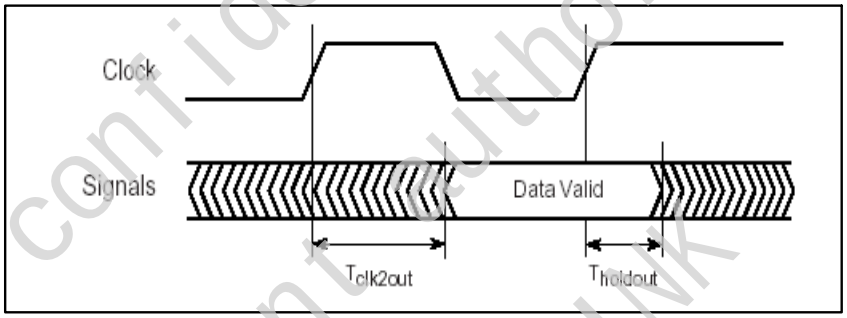


Figure 9. SDR DRAM Output Timing

8.2.4.4 SDR DRAM Access Control Timing

Table 12. SDR DRAM Access Control Timing

Symbol	Parameter	Units	Notes
$T_{REFRESH}$	Auto-Refresh Timing Controlled by Reg. 0xB8001008 (DTR)	µs	-
T_{RCD}	The Time Interval between RAS# Active and CAS# Active Controlled by Reg. 0xB8001008 (DTR)	ns	-

Symbol	Parameter	Units	Notes
T_{RP}	The Time Interval between Pre-Charge and the Next Active Controlled by Reg. 0xB8001008 (DTR)	ns	-
T_{RAS}	The Time Interval between Active and Pre-Charge Controlled by Reg. 0xB8001008 (DTR)	ns	-
T_{RC}	The Time Interval between Active and the Next Active Controlled by Reg. 0xB8001008 (DTR)	ns	1
T_{RFC}	The Time Interval between Auto-Refresh and Active Controlled by Reg. 0xB8001008 (DTR)	ns	-
$T_{CAS\_LATENCY}$	The Data Output Delay after CAS# Active Controlled by Reg. 0xB8001004 (DCR)	ns	-

Note 1: TRC=TRAS+TRP.

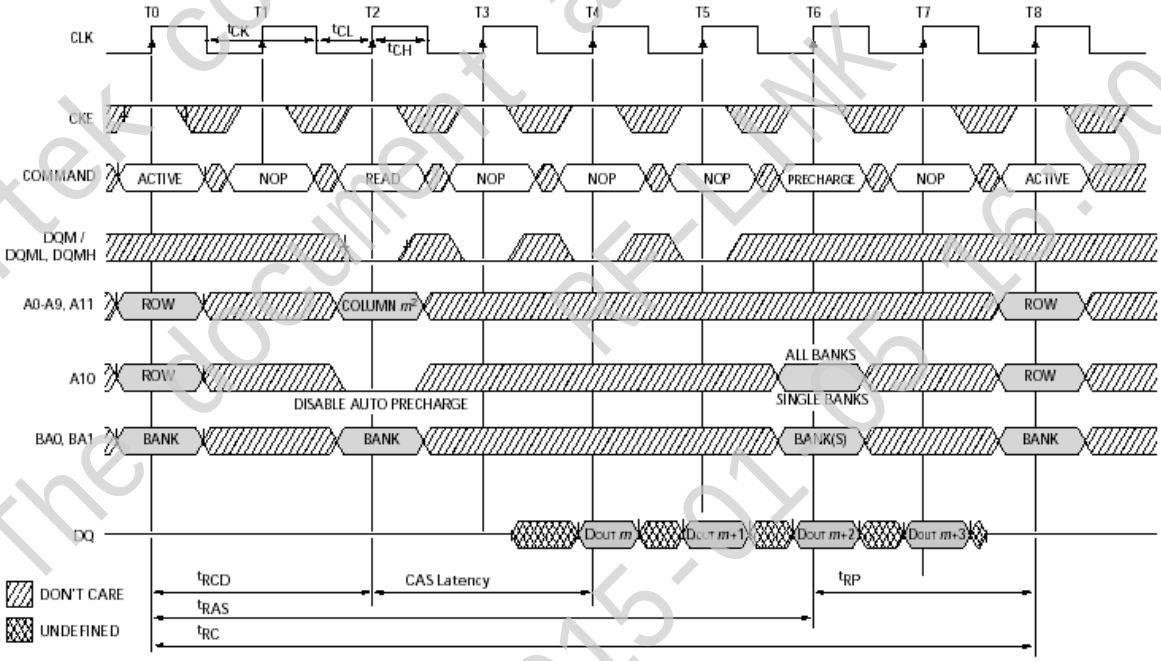


Figure 10. SDR DRAM Access Control Timing

8.2.5. SPI NOR Flash

8.2.5.1 Features

- Targeted SPI flash frequency: Up to 41.5MHz (when CPU clock is 166MHz)
- In addition to a programmed I/O interface, also supports a memory-mapped I/O interface for read operation
- Supports Read and Fast Read in memory-mapped I/O mode

8.2.5.2 Supported NOR Flash List

Table 13. Flash Bus DC Parameters

Vendor	Part Number	Density	Voltage	IO
MXIC	MXIC_MX25L4006E	4M Bits	3.3V	1I/2O
MXIC	MXIC_MX25L8073E	8M Bits	3.3V	1I/2O
MXIC	MXIC_MX25L8006E	8M Bits	3.3V	1I/2O

8.2.5.3 Electrical Specifications

Table 14. Flash Bus DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	1
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	2
V_{OH}	Output-High Voltage	-	2.4	-	-	V	3
V_{OL}	Output-Low Voltage	-	-	-	0.4	V	3
I_{IL}	Input-Leakage Current	V_{IN}=3.3V or 0	-10	±1	10	µA	-

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
I_{OZ}	Tri-State Output-Leakage Current	-	-10	±1	10	μA	-
R_{PU}	Input Pull-Up Resistance	-	-	75	-	KΩ	4
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	4

Note 1: V_{IH} overshoot: VIH (MAX)=VDDH + 2V for a pulse width ≤ 3ns.

Note 2: V_{IL} undershoot: $V_{IL\ (MIN)}$=-2V for a pulse width ≤ 3ns.

Note 3: The output current buffer is 8mA for the flash address and data bus; and is 8mA for Flash control signals.

Note 4: These values are typical values checked in the manufacturing process and are not tested.

8.3. General Purpose DMA Contrller

8.3.1. Features of GDMA

- Dual port DMA with totally 12 channels
- Configurable endian
- Support memory-memory, memory-peripheral, peripheral-memory, and peripheral-peripheral DMA transfer
- Support block level flow control
- Support address auto-reload, link-listed mode
- Support scatter-gather mode

8.3.2. GDMA Operations and Control

[TBD]

8.4. General Purpose Timer (GTimer)

8.4.1. Features of GTIMER

- 8 Gtimer supported
- Time unit is 32us
- Support Counter mode and timer mode

8.4.2. GTIMER Operations and Control

[TBD]

8.5. GPIO Functions

8.5.1. Features of GPIO

- GPO and GPI function
- Support interrupt detection with configurable polarity per GPIO
- Internal weak pull up and pull low per GPIO
- Multiplexed with other specific digital functions

8.5.2. GPIO Specifications

[TBD]

8.6. UART Interface Characteristics

8.6.1. Features of UART

- Support maximum 2 HS-UART (max baud rate 3.4MHz and DMA mode) and 2 low speed UART (IO mode)
- UART (RS232 Standard) Serial Data Format
- Transmit and Receive Data FIFO
- Programmable Asynchronous Clock Support
- Auto Flow Control
- Programmable Receive Data FIFO Trigger Level
- DMA data moving support to save CPU loading

8.6.2. High Speed UART Specification

The RTL8711AM UART interface is a standard 4-wire interface with RX, TX, CTS, and RTS. The default baud rate is 115.2k baud. In order to support high and low speed baud rate, the RTL8711AM provides multiple UART clocks.

Table 15. UART Baud Rate Specifications

Desired Baud Rate	Actual Baud Rate	Error (%)	Desired Baud Rate	Actual Baud Rate	Error (%)
300	300	0.00%	1200	1200	0.00%
600	600	0.00%	1800	1800	0.00%
900	900	0.00%	2400	2400	0.00%

Desired Baud Rate	Actual Baud Rate	Error (%)
3600	3601	0.03%
4800	4798	-0.04%
7200	7198	-0.03%
9600	9603	0.03%
14400	14395	-0.03%
19200	19182	-0.09%
28800	28846	0.16%
38400	38462	0.16%
56000	55970	-0.05%
57600	57692	0.16%
76800	76531	-0.35%
115200	115385	0.16%
128000	127119	-0.69%
153600	153061	-0.35%
230400	229167	-0.54%
460800	458333	-0.54%

Desired Baud Rate	Actual Baud Rate	Error (%)
500000	500000	0.00%
921600	916667	-0.54%
1000000	1000000	0.00%
1382400	1375000	-0.54%
1444444	1437500	-0.48%
1500000	1500000	0.00%
1843200	1833333	-0.54%
2000000	2000000	0.00%
2100000	2083333	-0.79%
2764800	2777778	0.47%
3000000	3000000	0.00%
3250000	3250000	0.00%
3692300	3703704	0.31%
3750000	3750000	0.00%
4000000	4000000	0.00%

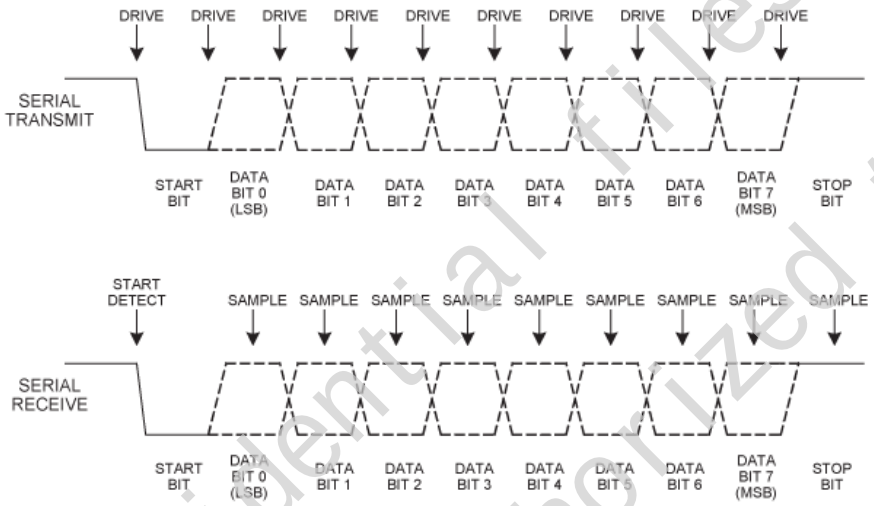


Figure 11. UART Interface Waveform

8.6.3. UART Interface Signal Levels

The UART signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the RTL8711AM UART interface via the IO power.

8.7. SPI Interface

8.7.1. Features of SPI

- Support 1 SPI port
- Support Master/Slave mode (SPI0 only), and Slave only (SPI1 and SPI2)
- Support DMA to offload CPU bandwidth
- 1 very high speed SPI with baud rate up to 41MHz
- 1 high speed SPI with baud rate up to 10MHz

- Programmable clock bit-rate
- Programmable clock polarity and phase
- Multiple Serial Interface Operations support
  - Motorola - SPI
  - Texas Instruments - SSI
  - National Semiconductor - Microwire

8.7.2. SPI-0 Specifications

[TBD]

8.8. I2C Interface

8.8.1. Features of I2C

- Support maximum 3 I2C port
- Three speeds:
  - Standard mode (0 to 100 Kb/s)
  - Fast mode (<400 Kb/s)
  - High-speed mode (<3.4 Mb/s) (with appropriate bus loading)
- Master or Slave I2C operation
- 7- or 10-bit addressing
- Transmit and receive buffers

- TX and RX DMA support (1 only)

8.8.2. I2C-1 Specifications

[TBD]

8.8.3. I2C-2 and I2C-3 Specifications

[TBD]

8.9. PWM Interface

8.9.1. Features of PWM

- Support maximum 4 PWM functions
- 0~100% duty can be configurable
- Minimum resolution is 32us
- The period can be configured up to 8 seconds

8.9.2. PWM Operations

[TBD]

8.10. External Trigger Event Interface

8.10.1. Features of External Trigger Event

- Support maximum 4 External Trigger Event functions without CPU active

- Triggered by GTIMER

8.10.2. External Trigger Event Operations

[TBD]

8.11. I2S Interface Characteristics

8.11.1. Features of I2S

- Support 8/16/24/32/48/96KHz, 44.1/88.2KHz
- Support 16 or 24 bits format
- Integrated DMA engine to minimize SW efforts
- Support TX and RX direction
- Master or Slave mode support

8.11.2. I2S Specifications

[TBD]

8.12. PCM Interface Characteristics

8.12.1. Features of PCM

The RTL8711AM supports a PCM digital audio interface that is used for transmitting digital audio/voice data to/from the Audio Codec. Features are supported as below:

- Supports Master and Slave mode
- Programmable long/short Frame Sync
- Supports 8-bit A-law/μ-law, and 13/16-bit linear PCM formats
- Supports sign-extension and zero-padding for 8-bit and 13-bit samples
- Supports padding of Audio Gain to 13-bit samples
- PCM Master Clock Output: 64, 128, 256, or 512kHz
- Supports SCO/ESCO link

8.12.2. PCM Specifications

8.12.2.1 PCM Format

FrameSync is the synchronizing function used to control the transfer of DAC_Data and ADC_Data. A Long FrameSync indicates the start of ADC_Data at the rising edge of FrameSync (Figure 12), and a Short FrameSync indicates the start of ADC_Data at the falling edge of FrameSync (Figure 13).

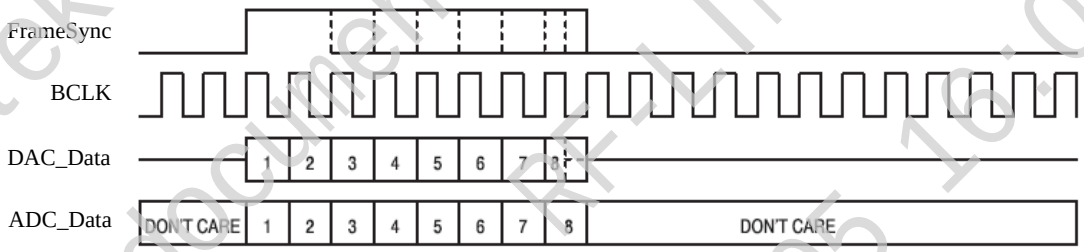


Figure 12. Long FrameSync

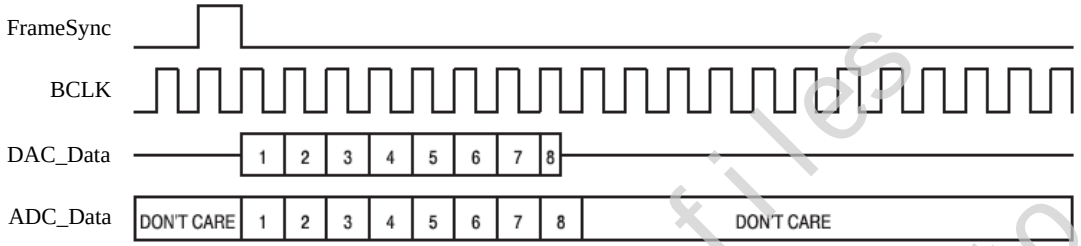


Figure 13. Short FrameSync

8.12.2.2 Sign Extension and Zero Padding for 8-Bit and 13-Bit Samples

For 16-bit linear PCM output, 3 or 8 unused bits may be sign extended/zero padded.

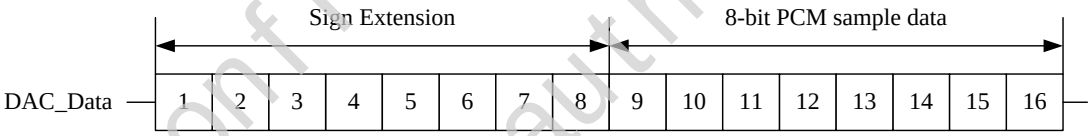


Figure 14. 16-Bit Output Data with 8-Bit PCM Sample Data and Sign Extension

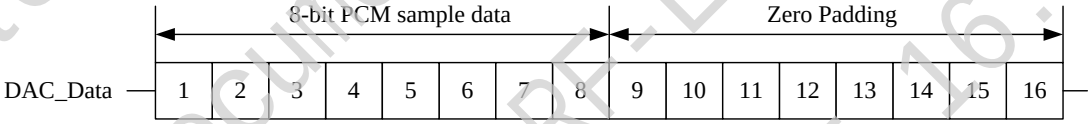


Figure 15. 16-Bit Output Data with 8-Bit PCM Sample Data and Zero Padding

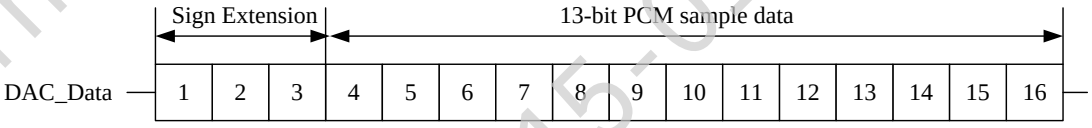


Figure 16. 16-Bit Output Data with 13-Bit PCM Sample Data and Sign Extension

For 16-bit linear PCM output, 3-bit programmable audio gain value can be padded to 13-bit sample data.

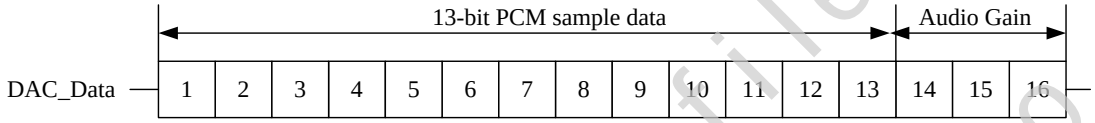


Figure 17. 16-Bit Output Data with 13-Bit PCM Sample Data and Audio Gain

8.12.2.3 PCM Interface Timing

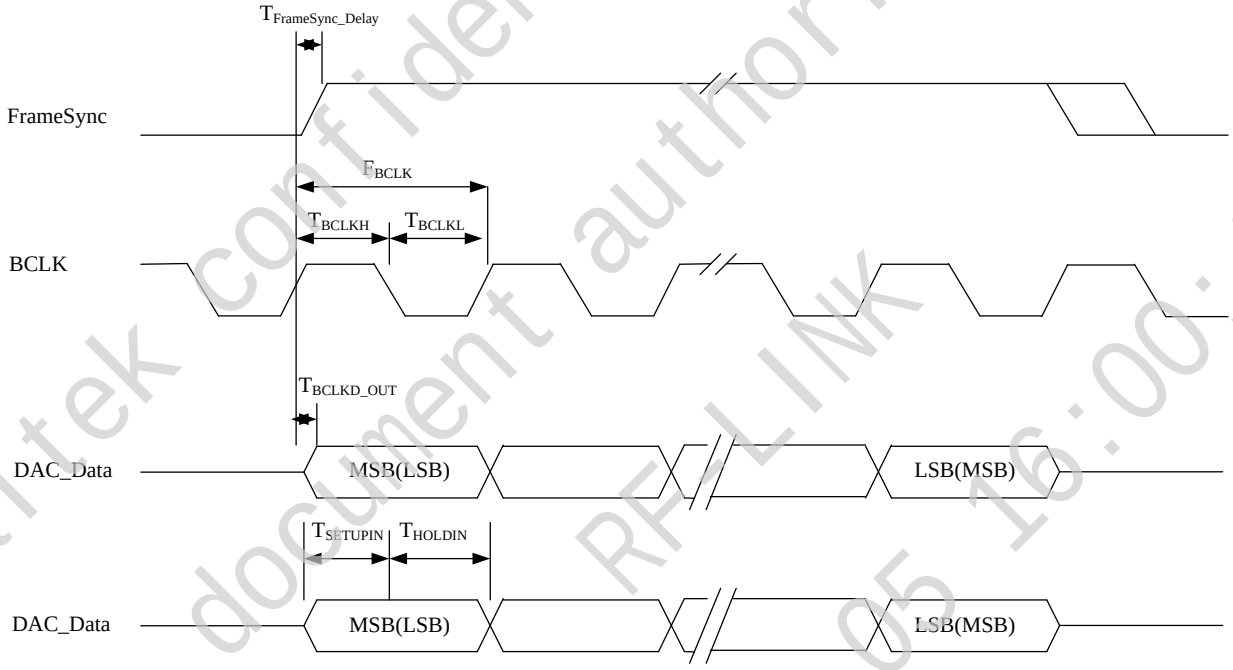


Figure 18. PCM Interface (Long FrameSync)

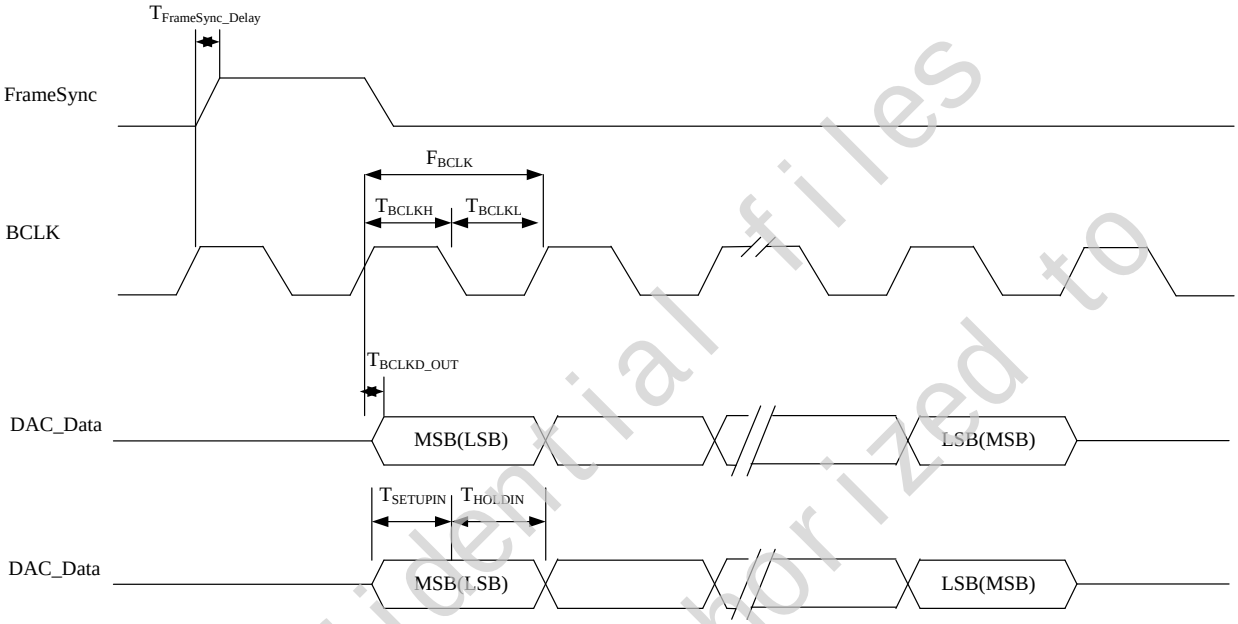


Figure 19. PCM Interface (Short FrameSync)

Table 16. PCM Interface Clock Specifications

Symbol	Description	Min.	Typ.	Max.	Unit
F_{BCLK}	Frequency of BCLK (Master)	64	-	512	kHz
$F_{FrameSync}$	Frequency of Frame Sync (Master)	-	8	-	kHz
F_{BCLK}	Frequency of BCLK (Slave)	64	-	512	kHz
$F_{FrameSync}$	Frequency of Frame Sync (Slave)	-	8	-	kHz
D	Data Size	8	8	16	bits
N	Number of Slots Per Frame	1	1	1	Slots

Table 17. PCM Interface Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{BCLKH}	High Period of BCLK	980	-	-	ns

Symbol	Description	Min.	Typ.	Max.	Unit
T_{BCLKL}	Low Period of BCLK	970	-	-	ns
$T_{FrameSync\_Delay}$	Delay Time from BCLK High to Frame Sync High	-	-	75	ns
T_{BCLKD_OUT}	Delay Time from BCLK High to Valid DAC_Data	-	-	125	ns
$T_{SETUPIN}$	Set-up Time for ADC_Data Valid to BCLK Low	10	-	-	ns
T_{HOLDIN}	Hold Time for BCLK Low to ADC_Data Invalid	125	-	-	ns

8.12.2.4 PCM Interface Signal Levels

The PCM signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the RTL8711AM PCM interface via the VDD_IO pin.

8.13. AD Converter

8.13.1. Features

- Up to 3 sets of 12-bit resolution A/D converter channel configurable
  - Bandwidth 16KHz
  - Input signal range: 0.01V ~ V_{REF} - 0.2V
- 1 16-bit high resolution A/D converter (ADC_CH2 only)
  - Bandwidth 64KHz
  - Input signal range: 0.01V ~ V_{REF} - 0.2V
- Support DMA mode

- Support One-Shot sampling mode without CPU active to save power
  - Pre-configured period to auto-sampling
  - Support two wakeup method: buffer threshold interrupt and event trigger

8.13.2. ADC Specifications and Operations

[TBD]

8.14. Security Engine

8.14.1. Features

- Provide low SW computing and high performance encryption
- Supported authentication algorithms:
  - MD5
  - SHA-1
  - SHA-2 (SHA-224 / SHA-256)
  - HMAC-MD5
  - HMAC-SHA1
  - HMAC-SHA2
-
- Supported Encryption / Decryption mechanisms:
  - DES (CBC / ECB)

- 3DES (CBC / ECB)
- AES-128 (CBC / ECB / CTR)
- AES-192 (CBC / ECB / CTR)
- AES-256 (CBC / ECB / CTR)

8.14.2. The DMA Engine Operation and the Descriptor Structure

[TBD]

9. Electrical Characteristics

9.1. Temperature Limit Ratings

Table 18. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C
Junction Temperature	0	125	°C

9.2. Power Supply DC Characteristics

Table 19. Power Supply DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
VA33, VD33IO, SW_HV3	3.3V Supply Voltage	3.0	3.3	3.6	V
VDD_IO	Digital IO Supply Voltage	1.62	1.8~3.3	3.6	V
VA12_AFE, VA12_SYN, VA12_RF	1.2V Core Supply Voltage	1.08	1.2	1.32	V
IDD33	3.3V Rating Current (with internal regulator and integrated CMOS PA)	-	-	450	mA

Symbol	Parameter	Minimum	Typical	Maximum	Units
IDD_IO	IO Rating Current (including VDD_IO)			200	mA
IDD_IO_33	3.3V IO Rating Current			50	mA

9.3. Power State and Power Consumptions

9.3.1. Sleep Mode Power Consumption

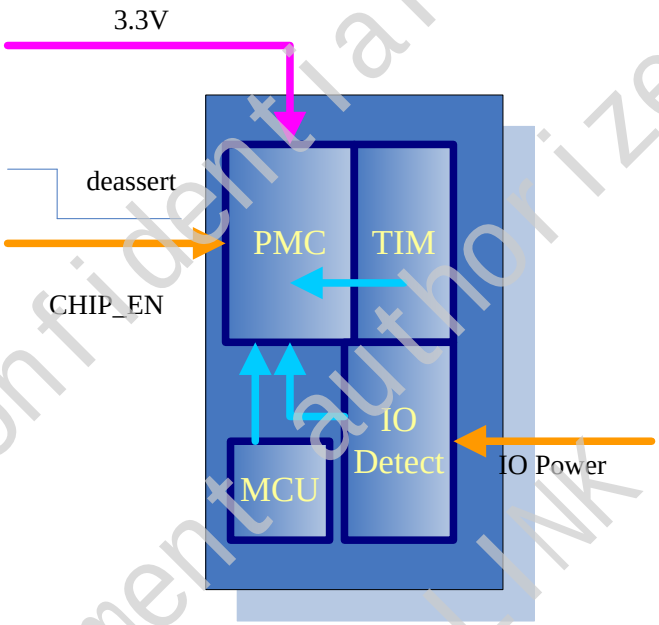
Table 20. Power Mode Brief Summary and Typical Power Consumption and Resume Time

Parameter	Power Consumption			Resume Time		
	Typical	Maximum	Units	Typical	Maximum	Units
Shutdown Mode	[TBD]	[TBD]	uA	[TBD]	[TBD]	ms
Deep Sleep Mode	[TBD]	[TBD]	uA	[TBD]	[TBD]	ms
Deep Standby Mode	[TBD]	[TBD]	uA	[TBD]	[TBD]	ms
Sleep Mode1	[TBD]	[TBD]	uA	[TBD]	[TBD]	ms
Sleep Mode2	[TBD]	[TBD]	uA	[TBD]	[TBD]	ms

9.3.2. Power Mode Description

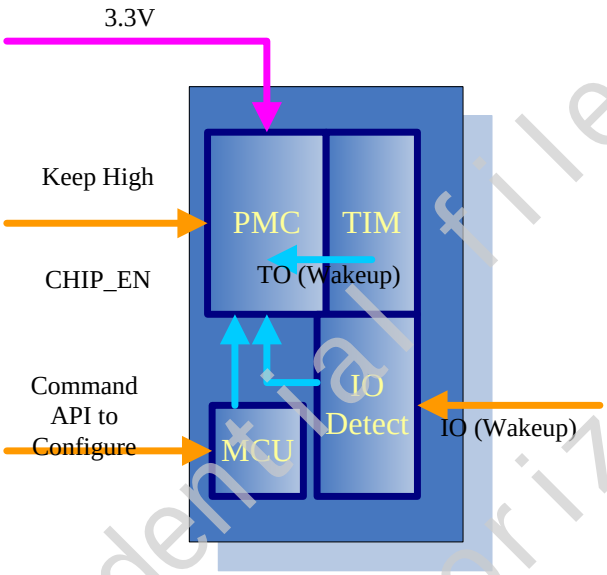
■ Shutdown Mode

CHIP_EN deasserts to shutdown whole chip without external power cut components required.



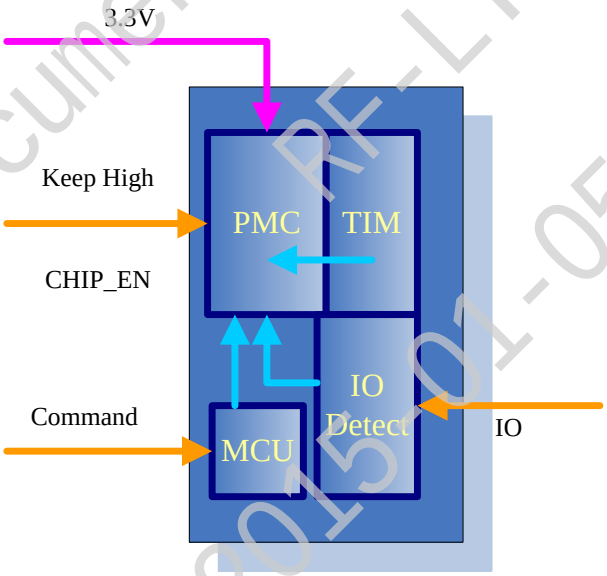
■ Deep Sleep Mode

CHIP_EN keeps high. Enter into Deep Sleep mode by API. The trigger timer period can be configured or GPIOB_0 can be used as external trigger event. The DLSP trigger timer can be configured with the range 1 ~ 3600 sec.



■ Deep Standby Mode

CHIP_EN keeps high. Entering into Deep Sleep mode by API. The trigger timer period can be configured or all GPIO group can be used as external trigger event.



■ Sleep Mode 1 and 2

[TBD]

9.3.3. Power On Sequence (Power On or Resume from Deep Sleep)

[TBD]

Figure 20. UART Power-On Sequence Without Hardware Flow Control

9.3.4. Power On Sequence (Power On or Resume from Deep Sleep)

[TBD]

Figure 21. UART Power-On Sequence Without Hardware Flow Control

9.3.5. Resume from Deep Standby

[TBD]

Figure 22. UART Power-On Sequence Without Hardware Flow Control

9.4. Digital IO Pin DC Characteristics

9.4.1. Electrical Specifications

Table 21. Typical Digital IO DC Parameters (3.3V Case)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	[TBD]	[TBD]	[TBD]	[TBD]	V	-
V_{IL}	Input-Low Voltage	[TBD]	[TBD]	[TBD]	[TBD]	V	-
V_{OH}	Output-High Voltage	[TBD]	[TBD]	[TBD]	[TBD]	V	-
V_{OL}	Output-Low Voltage	[TBD]	[TBD]	[TBD]	[TBD]	V	-

Note

Table 22. Typical Digital IO DC Parameters (1.8V Case)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	[TBD]	[TBD]	[TBD]	[TBD]	V	-
V_{IL}	Input-Low Voltage	[TBD]	[TBD]	[TBD]	[TBD]	V	-
V_{OH}	Output-High Voltage	[TBD]	[TBD]	[TBD]	[TBD]	V	-
V_{OL}	Output-Low Voltage	[TBD]	[TBD]	[TBD]	[TBD]	V	-

Note

9.5. USB Electrical Specifications

Table 23. USB v2.0 DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	-	200	-	-	mV	2
V_{IL}	Input-Low Voltage	-	-	-	10	mV	2
V_{OH}	Output-High Voltage	-	300	-	500	mV	2
V_{OL}	Output-Low Voltage	-	-10	-	10	mV	2
I_{IL}	Input-Leakage Current	-	-	-	-	µA	1

Note 1: These values are typical values checked in the manufacturing process and are not tested.

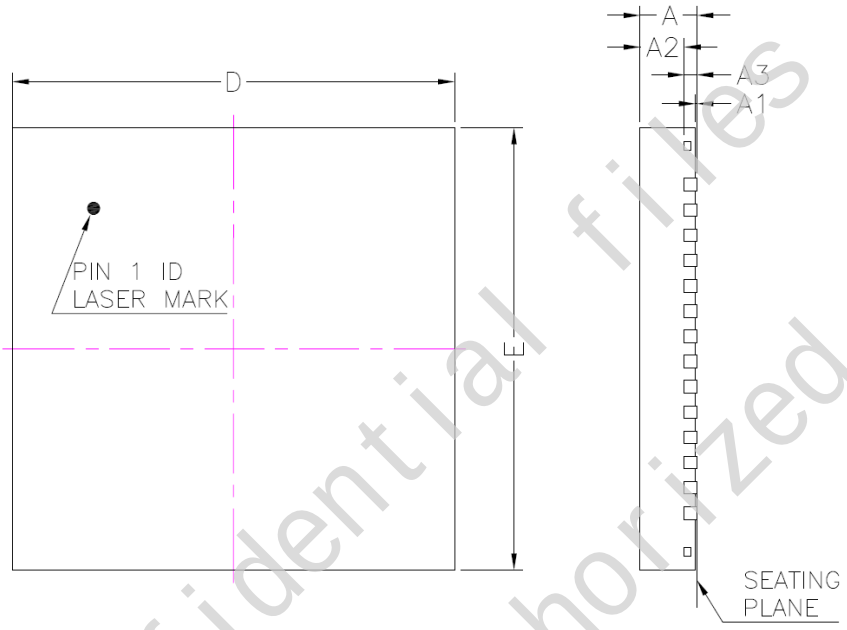
Note 2: For additional information, see the USB v2.0 Specification.

9.6. AD Converter Electrical Specifications

9.7. DA Converter Electrical Specifications

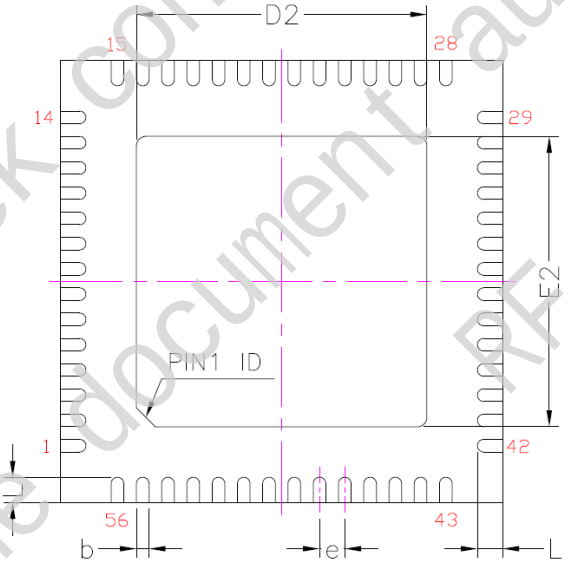
10. Mechanical Dimensions

10.1. Package Specification

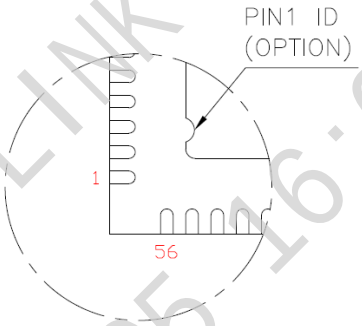


TOP VIEW

SIDE VIEW



BOTTOM VIEW



PIN1 ID OPTION

10.2. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_2	---	0.65	0.70	---	0.026	0.028
A_3	0.2 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	7.00 BSC			0.276 BSC		
D_2/E_2	4.35	4.60	4.85	0.171	0.181	0.191
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes：

1. CONTROLLING DIMENSION：MILLIMETER(mm).
2. REFERENCE DOCUMENTL：JEDEC MO-220.

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.05	1.12	1.19	0.041	0.044	0.047
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.86	0.91	0.96	0.034	0.036	0.038
c	0.22	0.26	0.30	0.009	0.010	0.012
D	5.90	6.00	6.10	0.232	0.236	0.240
E	5.90	6.00	6.10	0.232	0.236	0.240
D1	---	5.00	---	---	0.197	---
E1	---	5.00	---	---	0.197	---
e	---	0.50	---	---	0.020	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa	0.10			0.004		
bbb	0.10			0.004		
ddd	0.08			0.003		
eee	0.15			0.006		
fff	0.05			0.002		
MD/ME	11/11					

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: bbb,ddd
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
6. REFERANCE DOCUMENT : JEDEC PUBLICATION 95 DESIGN GUIDE 4.5

11. Ordering Information

Table 24. Ordering Information

Part Number	Package	Status
RTL8711AM-VA0-CG	QFN-56, 'Green' Package	Engineering Samples

Note: See page 14 for package identification.