Transmitter Programming Interface (TPI) Programmer's Reference

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Revision History

Revision	Date	Comment
0.77	04-09-10	Update wakeup support in D3 Cold and Hot for SiI 9022A/ SiI 9024A. Clarify RESET value. Removed comment about 3D modes and DE generator.
0.76	03-08-10	Revised Programmer's Reference release. Updates for SiI9136/9334: - Added workaround for HBR audio (added V bit programming) - Revised Ri Read section - Fixed Video Black Mode Register access - Added video output programming section - Fixes for KSV Forward - Fixes for range control

0.75	02-04-10	Revised Programmer's Reference release. Updates for SiI9136/9334: - Update SiI9136/9334 Revision ID - Add Hot Plug Delay De-bounce - Update explicit Sync DE Generator values for H_RES, DE_CNT, DE_LIN - Indicate Bit swap and YC Channel swap features function without enable - Add Ri Read, Bcaps and Bstatus - Add VSYNC and HSYNC polarity to Embedded Sync Extraction Registers - Indicate re-write of TPI 0x60 after setting AVI InfoFrame not necessary - Remove 2x clocking setting from 16bit deep color setting - Video Black Mode Levels provided for Black Mode of Video Input Mode - When TPI 0x1A transitions from DVI to HDMI, then TPI 0x08[1:0] is no longer cleared - Remove manual configuration for 192kHz S/PDIF with 480i video - Muting works in DVI mode - Deep Color modes require GCP to send deep color information, this must be enabled by software - Add TPI Soft Reset Register - Removed incorrect restrictions on H_Res for 3D modes - Updated HEAC information with latest recommendations
0.74	09-21-09	Revised Programmer's Reference release. Changes: - Removed incorrect restriction on H_RES for 3D modes - Updated HEAC information with latest recommendations - Removed SiI9230/9234 Tx references (moved to separate document) - Added notes of interest to describe details of HDCP operation.
0.73	08-18-09	Revised Programmer's Reference release. Changes: - Corrected description of TPI 0x1F (I^2S register) - Clarified description of authentication success/fail status - Added supported 3D mode descriptions - Clarified Access requirements in register descriptions - Added clarification notes for SiI9136/9334 Tx operation - Modified DE_ADJ# setting recommendation
0.72	06-15-09	Revised Programmer's Reference release. Changes: - Added ARC and HEAC sections. - Added significant information and corrections to most sections.
0.71	02-27-09	Revised Programmer's Reference release. Changes: - Removed "Advance" from title, because this document is mature for most products represented. - Added additional information for new and upcoming products
0.70	11-18-08	Initial Advance Programmer's Reference release.

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Overview

Silicon Image HDMI transmitter solutions merge independent video and audio streams for transmission over HDMI. To do this, the transmitter employs a unique mechanism that allows host graphics and audio software to interact with the HDMI transmitter.

All new devices implement a simplified interface and special logic that automates most HDMI functions. This Transmitter Programming Interface (TPI) maps a concise set of registers into I^2C address space that the host can readily access.

TPI offers a significantly simplified operating scheme, using built-in hardware to handle tasks such as the following.

- Secure operation is fully automatic on devices equipped with HDCP. With only a single-bit write, the device establishes and maintains link security, interrupting the host only if the secure link is lost.
- DDC arbitration is handled cleanly, allowing the host to simply request the bus and then fetch EDID information directly – no need to program transfers into or out of a FIFO. Arbitration is handled even when link security is enabled.
- Complex audio setup is nearly eliminated. Hardware calculates N/CTS values and automatically sends out the appropriate packet information with no setup needed.
- All frequency-dependent internal settings, such as for PLLs, are derived automatically in hardware from the video mode information that has been programmed.

In addition:

- Devices still implement the standard Silicon Image register set used by legacy transmitters, for backwards compatibility with special functions in existing code.
- All devices implement an automated CEC controller, using the Silicon Image standard CEC Programming Interface (CPI).
- Many versions additionally support HDCP, implemented as part of the automated solution and requiring no host intervention for normal operation.

This document describes the TPI programming solution for the following devices.

HDCP-enabled Version	Non HDCP-enabled Version	Upgrade to this existing product	Application
SiI9024 Tx	SiI9022 Tx	SiI9020 Tx	HDMI Mobile
SiI9024A Tx	SiI9022A Tx	SiI9022/24 Tx	HDMI Mobile
SiI9136 Tx SiI9334 Tx	—	SiI9034 Tx	STB, PVR, AVR
SiI9222 Tx	SiI9226 Tx	—	Mobile HD Link*
SiI9232 Tx	SiI9236 Tx	—	Mobile HD Link*

* Mobile HD Link solutions have additional programming requirements covered in Appendix B.

Figure 1 illustrates the major functional blocks for a typical TPI-based transmitter solution.

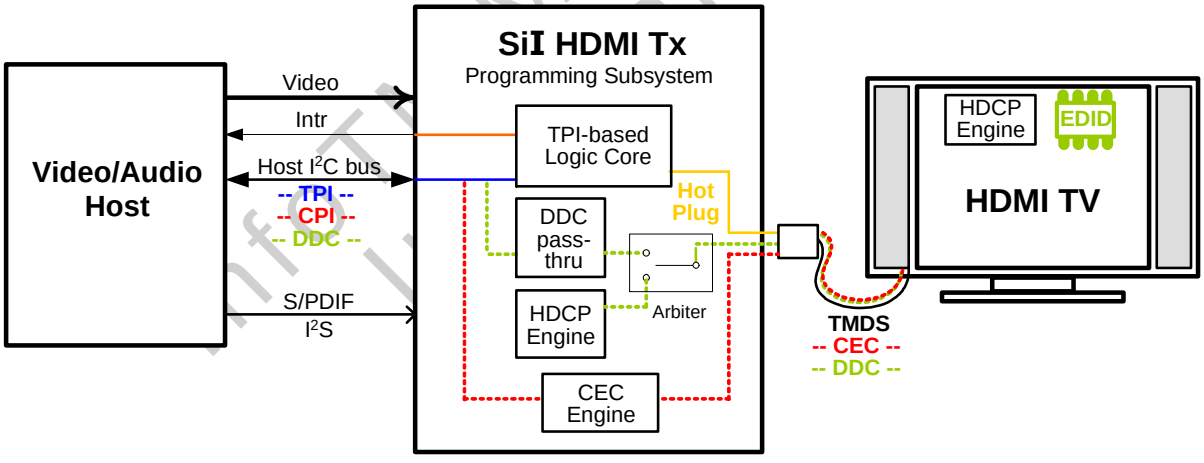


Figure 1. Transmitter Data Flow Paths

Register Group Summary

Transmitter Programming Interface (TPI)

TPI provides a programming interface that operates at a higher hardware level than traditional register file interfaces. The TPI register groups below handle all normal chip operations in a concise format.

Table 1. Register Group Summary

Group Function	Register Addresses	Page	Register Name	What Firmware Does with these Registers
Identification	0x1B-1D	11	Identification	Identifies the chip and version of TPI implemented.
Input Configuration – one-time configuration of the input bus for its application environment.	0x08	13	Input Bus and Pixel Repetition	Selects input bus characteristics like pixel size, clock edge
	0x0B	19	YC Input Mode Select	Selects YC Mux modes, signal timing features, and chooses sync method registers to access
	0x60-61	18	Sync Configuration and Monitoring	
	0x62-6D with 0x60[7]=0	21	Explicit Sync DE Generation	Defines parameters for explicit sync method
	0x62-6D with 0x60[7]=1	23	Embedded Sync Extraction	Defines parameters for embedded sync method
Audio Configuration	0x1F-0x28	29	Audio Configuration	Configures audio input channels and rates
Video Mode Select – resolution, color space, InfoFrame headers	0x00-0x07	12	Video Mode	Defines the incoming resolution
	0x09-0A	15	Input and Output Format	Defines color space, color depth
	0x0C-0x19	24	AVI InfoFrame	Programs header information as defined by HDMI specification
	0xBF-0xDE	25	Other InfoFrame	
	0x60	19	YC Mux Mode	
System Control – single-byte control for most-used functions	0x1A	26	System Control	Requests DDC bus access, selects between DVI/HDMI, controls TMDS output and AV Mute
Interrupt – single-byte status for monitoring significant events	0x3C-3D	36	Interrupt	Polls for and clears events, selects the interrupt events that should cause hardware INT activation
Power Control	1E	40	Power Control	Selects full-power operational mode or low-power standby mode
HDCP – automatic security	0x29-0x3A	45	HDCP	Sets up and monitors HDCP link security

Internal (Indexed) Registers

Underlying the TPI register set is a broader and more complex internal register set that is normally hidden from direct access. This register set includes the "legacy" registers that were available in older programming methodologies, but also some additional registers that are used primarily during chip development and testing.

From time to time, situations arise that require customer software to manually access these internal registers. Therefore, a mechanism is provided for accessing single bytes. Where defined, Internal Registers are accessed as noted below.

1. Set Page	2. Select Indexed Offset within Page	3. Obtain Read/Write Register Access
0xBC	0xBD	0xBE

Device-Specific Information

Several documents are required for a full understanding of the system level operation of the chip. Information in the Data Sheet and starter kit User's Guide is specific to the device in question; references are provided in the appropriate section below. CEC information is common to all devices and is provided in the following document.

- SiI-PR-0041: *CEC Programming Interface (CPI) Programmer's Reference*

SiI9022 and SiI9024 Tx

The SiI9022 and SiI9024 transmitters are improved replacements for the SiI9020 Tx. The following additional documents are required for a full understanding of the system level operation of these chips.

- SiI-DS-1009: *SiI9022/9024 HDMI Transmitter Data Sheet*
- SiI-UG-1010: *CP9022HDMI/9024HDMI Starter Kit User's Guide*

Differences between SiI9022 and SiI9020 Transmitters

The default SiI9022 transmitter register set has been maintained identically from the SiI9020 transmitter, but with the following improvement.

- The SiI9020 transmitter implemented a hardware state machine to drive the DDC I^2C bus. The host set up a transfer by programming a series of bytes, and then waited for the chip to complete the transfer and generate an interrupt.
- The SiI9022 transmitter implements an I^2C pass-through mechanism, which is driven directly by the host as if the DDC device were on the local I^2C bus. No transfer setup or interrupt service is required.

Differences between SiI9024 and SiI9022 Transmitters

From a programming point of view, the SiI9024 transmitter has all the same features as the SiI9022 transmitter. Additionally, the SiI9024 transmitter contains an HDCP encryption engine and pre-programmed HDCP keys.

An extra register group is implemented in the SiI9024 transmitter to operate the HDCP function in a completely automatic way. Note that SiI9020 Compatible Mode operation (refer to Appendix A) cannot be chosen for the SiI9024 transmitter if HDCP is required, since the SiI9020 transmitter did not support HDCP.

SiI9022A and SiI9024A Tx

The SiI9022A Tx and SiI9024A Tx are pin- and feature-compatible replacements for the SiI9022 Tx and SiI9024 Tx, respectively. Refer to SiI-DS-1053 – *SiI9022A/9024A HDMI Transmitter Data Sheet* – for additional information.

Differences between SiI9022/SiI9024 and SiI9022A/SiI9024A Transmitters

Several new features have been added to the "A" version TPI register set, improving the ease of use.

- x.v.Color is supported by sending gamut descriptor packets (described in Other InfoFrame Data section).
- Top level TPI support is provided for TClkSel (TPI 0x08) and Audio Packet Layout Control (TPI 0x26).
- I^2S Audio Input Word Length selection is now written automatically (TPI 0x25).
- CEC no longer requires calibration (refer to the *CEC Programming Interface (CPI) Programmer's Reference* (SiI-PR-0041).

Firmware that runs on the SiI9022 or SiI9024 transmitter will run unchanged on the "A" version of these parts. However, certain changes should be considered for most efficient operation.

- The D3 state now has an additional requirement to program the "Cold" mode to take advantage of the new lower-power TMDS core.
- Wakeup from Receiver Sense (RSEN) is not available in D3 Cold mode but, is available in D3 Hot mode..
- The devices come up in operational state after a hardware reset, with the TMDS output enabled. To enter an intermediate power mode similar to the reset state of a non "A" device, it is necessary to enter TPI mode (writing 00 to 0xC7).

Detection of HDCP capability on the "A" devices works slightly differently than on previous devices.

- On non "A" devices, software could read the HDCP revision ID register TPI 0x30 to distinguish SiI9024 Tx (HDCP-equipped) from SiI9022 Tx (not HDCP-equipped). A zero value indicated no HDCP support. This method is no longer supported on "A" devices.
- New method: To distinguish SiI9024A Tx (HDCP-equipped) from SiI9022 Tx or SiI9022A Tx (not HDCP-equipped), software must read the Aksv value from registers starting at TPI 0x36, and check for a valid value (20 1s and 20 0s). This method is a more secure means of verifying host HDCP capability.

SiI9136 Tx and SiI9334 Tx

Differences between SiI9034/9134 Tx and SiI9136/9334 Transmitters

The SiI9034 Tx and SiI9134 Tx used an older register scheme that required significant software intervention and overhead to manage all aspects of operation. This "legacy" register set is replaced on the SiI9136/9334 Tx by TPI. The TPI logic scheme automates many tasks that previously required software support. As a result, the register set is greatly reduced, simplifying support code and reducing software overhead.

The need for specific legacy register support has been superseded by the TPI register set as shown in Table 2.

Table 2. Comparison of Legacy Registers to TPI Registers

SiI9034/9134 Tx Register Group			SiI9136/9334 Tx TPI Correspondent	Notes
I^2C Device	Group Name	Reg Address		
0x72	ID	0x00-04	0x1B-1D	ID Registers
	System Control and Status	0x08-0D	0x08 (edge, bsel) 0x1E (power ctrl) 0x3D (hpd, rsen)	Clock stability monitoring is fully automated under TPI, as are plug/unplug handling and power cycling.
	HDCP	0x0F-2B	0x29-46	All parts of the HDCP authentication protocol are fully automated under TPI. Register group is reduced from 35 bytes to 18.
	Video	0x32-3D, 0x3E-47	0x60-0x6D	DE Generator and Embedded Sync register groups are overlaid in TPI.
		0x48-0x4E	0x09-0B	
	Interrupt	0x70-79	0x3C,3D	Interrupt handling is consolidated, and most critical events are handled automatically under TPI. Reading one byte returns all event information. Register group is reduced from 16 bytes to 2.
	TMDS PLL	0x0C 0x80-85	0x00-01	Filter PLL control settings are loaded automatically under TPI, according to the frequency programmed. Register group is reduced to 2 bytes.
	Reset	0x05	—	Reset control is fully automated under TPI. No manual reset sequencing is required on frequency changes.
	DDC, ROM	0xEC-F5, 0xF9, 0xFA	0x1A	Direct DDC bus access is granted, with no need for programmed transfers, under TPI. A single register write gains access to the bus. Register group is reduced to 1 byte.
0x7A	Audio	0x00-3D	0x1F-28	Audio handling, including loading of N/CTS values, is fully automated under TPI. Audio-related resets are no longer required. Register group is reduced to 10 bytes.
	Packet	0x3E-FE	0x0C-19 0xBF-DE	Most packet groups are overlaid in TPI. Register group is reduced from 192 bytes to 46.

Additional differences are as follows.

- The SiI9334 Tx supports certain HDMI 1.4 features; these are described in Appendix D.

- Some legacy registers from the SiI9034/9134 Tx are available through an indirect (indexed) access mechanism on the SiI9136/9334 Tx. When the register page is written to TPI 0xBC, and the register index to TPI 0xBD, the legacy register becomes read/write accessible at TPI 0xBE. Software engineers who have needs not met by TPI can therefore revert to the legacy registers for special cases. Note that HDCP operation is not supported through legacy registers.

Refer to SiI-DS-1064 – *SiI9334 HDMI Transmitter Data Sheet* – for additional information.

Differences between SiI9024A Tx and SiI9136/9334 Transmitters

Firmware that runs on the SiI9024A Tx will run unchanged on the SiI9136/9334 Tx. However, some additional features listed below have been added to the SiI9136/9334 Tx.

- Supports 48 bit Deep Color at up to 1080p, 30 frames per second, as controlled by new register bits at TPI 0x09.
- Supports certain HDMI 1.4 features, described in Appendix D.
- Supports HBR Audio and DSD Audio, enabled through TPI 0x26.

Refer to SiI-DS-1064 – *SiI9334 HDMI Transmitter Data Sheet* – for additional information.

I²C Requirements

The host must have hardware reset control over the transmitter, typically through a GPIO pin. The transmitter notifies the host of service needs through an interrupt line. All other communication occurs by way of the local I²C interface.

I²C Access Speeds. The internal hardware I²C interface of the transmitter runs at speeds up to 400kHz. This throughput can also be achieved on the DDC interface, if the connected device supports it, when using the pass-through I²C feature of the TPI register set.

The host software is responsible for ensuring its DDC access speed does not exceed the limitations of any device present on the bus – all devices must be determined capable of supporting 400kHz operation before the host attempts to do any accesses at that speed. Speeds in excess of 100kHz may not be allowed by the interface specification in use.

> → **Important Note:** There is lower speed limit of 40kHz on DDC pass-through operation, except for the SiI9136 Tx and SiI9334 Tx which have a lower limit of 1kHz.

I²C Access Addresses. The I²C address used to access the TPI registers is 0x72. The transmitter can optionally respond at address 0x76 depending on the CI2CA hardware strap setting described in the transmitter Data Sheet. Certain legacy registers, not supported on all devices, respond at 0x7A (or 0x7E depending on CI2CA pin strapping).

The I²C address used to access the CPI registers is noted in the *CEC Programming Interface (CPI) Programmer's Reference* (SiI-PR-0041). The I²C address used to access the CTRL bus registers is noted in the "CTRL Bus Configuration" section.

In a TPI transmitter environment, the host masters one I²C interface, and the transmitter masters another, as illustrated for a typical transmitter in Figure 1. For transmitters without HDCP capability, the I²C paths are the same, but the DDC bus is not used for HDCP in this case.

- **Host TPI/CPI/DDC I²C Interface.** The transmitter implements this slave interface, mastered by the host. The host serially transmits and receives data over this bus, which implements a register interface structure where the host writes video mode and HDCP control data and reads back connection status information.
- **DDC I²C Interface.** When using the native TPI operating interface, the transmitter implements this interface as a pass-through connection from the host to the DDC bus of the HDMI TV. The transmitter has the ability to block the graphics host from accessing this bus when using it for HDCP, and also monitors the bus for activity to prevent breaking an active connection.

Summary of Host Software Tasks

Managing TPI operations is straightforward, starting from when the host resets the subsystem after power-up.

Initialization. After reset, the subsystem comes up in a pre-determined state:

- Standby (D2) state for SiI9022 Tx, SiI9022A Tx, SiI9024 Tx, SiI9024A Tx
- Active (D0) state for SiI9136/9334 Tx.

Host software initializes it by:

- Configuring the registers according to known video/audio input format information
- Enabling any interrupt events to be signaled on the INT pin.

From this point, there are various service conditions that will be called for.

Hot Plug Service. Until a device is attached, the host just monitors the connection status either through interrupts or by polling. The host software waits for an attached Sink hot plug event, and then:

- Reads the downstream Sink EDID information
- Powers up the transmitter (D0 state)
- Sends active video corresponding to the Sink capabilities, and selects DVI or HDMI mode, depending on the EDID information found.

Operational State. The subsystem manages most routine HDMI activities in Operational state. The host software usually only needs to:

- Change video modes
- Enable HDCP operation and check the ksv list against known bad keys in the SRM
- Monitor ongoing HDCP operation, through interrupt service or by polling.

Unplug Service. Once the subsystem detects a hot unplug event, it:

- Notifies the host through INT (if the interrupt is enabled)
- Disables HDCP and restores certain other logic states
- On the next plug-in event, drives the INT pin active (if the interrupt was previously enabled)**.**

Within the host software, Unplug Service events are typically handled by the Hot Plug Service routine.

Reserved Bits. Bits marked *Rsvd* or *Reserved* should be written as 0 when other bits in the register are accessed, unless otherwise noted.

Detailed Sequences

In the following descriptions:

- 'host' refers to activities of the software for the graphics host processor.
- 'TPI' refers to use of the I^2C interface to access the TPI registers implemented in the transmitter itself.
- 'Tx' refers to the respective transmitter chip variant. 'Rx' refers to the HDCP registers on the remote HDMI receiver.

Initialization

The following steps are required to prepare for operation.

Step	Function	Registers Involved	See page	Details
1	Reset and Initialize	0xC7	--	host → TPI: Hardware Reset to Tx subsystem The host must reset the chip, then write **0x00** to **0x72:0xC7** to enable TPI mode.
2	Detect Revision	0x1B-0x1D	11	host ← TPI: Detect Tx type and TPI revision. When TPI 0x1B can be read correctly, the TPI subsystem is ready.
3	Power up transmitter	0x1E	40	host → TPI: Enable active mode. Write TPI 0x1E[1:0] = 00
4	Configure Input Bus and Pixel Repetition	0x08	13	host → TPI: Select input bus characteristics like pixel size, clock edge
5	Select YC Input Mode	0x0B	19	host → TPI: Select YC input mode and signal timing features
6	Configure Sync Methods	0x60-61	18	host → TPI: Choose the sync method register group to access, enable YC Mux mode
7	Configure Explicit Sync DE Generation	0x62-6D w/ 0x60[7]=0	21	host → TPI: Define parameters for explicit sync method
8	Configure Embedded Sync Extraction	0x62-6D w/ 0x60[7]=1	23	host → TPI: Define parameters for embedded sync method Note that the TPI 0x63 values must be rewritten after 0x19 is written.
9	Set up Interrupt Service	0x3C	36	host → TPI: Enable hardware interrupts to be serviced (TPI 0x3C).

→ **Important Note:** For TPI operation, **always** write device address 0x72, register offset 0xC7 = 0x00 as the first step after hardware reset. (This step is not required on the SiI9222/9226 device.)

Step 1 above is mandatory to allow operation of the TPI register set on HDMI transmitters. If the write is not done as the first register write, the transmitter will revert to SiI9020 Tx Compatible Mode register set operation; the TPI registers will not be accessible. Refer to Appendix A for details.

SiI9022A/9024A/9136/9334 Tx only. These devices require transmitter source termination to be enabled manually during initialization. After powering up the transmitter, the host should write the following sequence to enable source termination.

```
a) Write 0xBC=0x01              // Internal page 1
b) Write 0xBD=0x82              // Indexed register 82
c) Read 0xBE                    // Read current value
d) Modify bit[0] = 1            // Enable source termination
e) Write 0xBE                   // Write back modified value
```

Servicing a Hot Plug Event

The host must recognize and handle Plug and Unplug events either by polling or interrupts as described in the Hot Plug Management section. Once a Plug event has been confirmed, the host follows the sequence below.

Step	Function	Registers Involved	See page	Details
1	Host reads EDID and sets interface type	0x1A	26	host → Tx → Monitor: Use DDC to access EDID. Host uses TPI 0x1A to request access to the DDC bus; scans EDID and reads video information, audio descriptors, and HDMI signature; then writes to TPI 0x1A to set interface type detected (HDMI or DVI) and to release the DDC bus.
2	Host enables bridge CEC operation	CTRL	60	For Mobile HD Link devices only. Refer to Appendix B.
3	Host sends video and audio	--	--	host → Tx: Begin transmitting video and audio streams.
4	Host sets video format and resolution	0x00-0x0A	12	host → TPI: Set the VMode and Format registers. Writing VMode optimizes the operation of the internal logic for the particular speed selected. Expansion and compression are set in the Input and Output Format registers.
5	Host sets AVI InfoFrame	0x0C-0x19	24	host → TPI: Set AVI InfoFrame. For an HDMI sink, write the AVI InfoFrame registers (0x0C-0x19). For a DVI sink, these registers must be cleared.
6	Host optionally selects YC Mux mode	0x60	19	host → TPI: Set YC Mux Mode if needed. Except for SiI9334 and SiI9136, any time TPI 0x19 is written, TPI 0x60[5] will be reset to its default state and must be explicitly restored to enable YC Mux (one- to two-data-channel de-mux) mode.
7	Host optionally configures Embedded Sync Extraction	0x63 w/ 0x60[7]=1	23	host → TPI: Define parameters for embedded sync method Any time TPI 0x19 is written, TPI 0x63 will be reset to its default state and must be explicitly restored.
8	Host sets audio mode	0x1F-0x28	29	host → TPI: Host parses audio descriptors from EDID, then sets audio configuration using capabilities information found.
9	Host enables video output	0x1A	26	host → TPI: Enable TMDS Output. Write TPI 0x1A[4] = 0.
10	Host chooses pixel repetition rate	0x08		host → TPI: Select pixel repetition rate. Except for SiI9334 and SiI9136, this setting must always be made *after* changing 0x1A[4] from 1 to 0.
11	TPI looks for sink HDCP capability	--	--	TPI → Monitor: HDCP read of Bksv, Bcaps from Rx. This process happens without host intervention, triggered by the enabling of the TMDS output. This step occurs for HDCP-capable transmitters only, and can take up to 2 seconds to complete depending on sink readiness.

After configuration, the chip must be explicitly commanded to enter active (D0) mode as noted above. Video, audio, and interrupt settings can also be changed after entering D0 state, but changing the audio input selection may cause disturbances in output video and audio streams. Refer to the Transmitter Power State Register section for information on entering various power states.

Changing Video Modes

Switching input video or audio modes requires a resolution change sequence. Note that if not using AV Mute, the host must **disable** HDCP before changing video modes. Otherwise, the disruption in video could break authentication at the receiver.

Step	Details
1	host → TPI: Blank the Display (optional). Write 0x1A[3] = 1 to send an AV Mute control packet to blank the sink device. Wait at least 128ms to allow control InfoFrames to pass through to the sink device.
2	host → TPI: Prepare for Resolution Change. Write 0x1A[4] = 1 to start the resolution change process.
3-10	Same as steps 3-10 in "Servicing a Hot Plug Event".
11	host → TPI: Enable Display (optional). Write 0x1A[3] = 0 to un-blank the sink device.

HDCP Authentication and Encryption

The hardware takes control of the DDC bus during HDCP operation. Refer to the section on p. 26 for limitations on using the DDC bus while HDCP is enabled.

Step	HDCP-Capable Transmitter Details
1	host ← TPI: HDCP available? (TPI 0x30 for chip availability, TPI 0x29[1] for Sink availability)
2	host ← TPI: Read Aksv (TPI 0x36 group) and Bksv (TPI 0x2B group) for verification purposes (check each for 20 '1's and 20 '0's)
3	host → TPI: Request link security (TPI 0x2A)
4	Tx → Rx: Authenticate local link, authenticate repeater link, start link integrity check
5	host ← TPI: Await "link secure" status (TPI 0x29)
6	host → Tx: Send secure content.
7	host ← TPI: Periodically verify "link secure" status (TPI 0x29)

HDCP Revocation Check

Step	HDCP-Capable Transmitter Details
1	host ← TPI: Repeater attached? (TPI 0x29)
2	host ← TPI: Extended link (through repeater) secure? (TPI 0x29)
3	host ← TPI: assert "Interrupt Control Received 1st Byte of KSV" (TPI 0x3E[1])
4	host ← TPI: read "Number of bytes in KSV FIFO" (TPI 0x41[4:0])
5	host → TPI: Prepare to read KSV list (use Req/Gnt, TPI 0x1A)
6	host ← Monitor: Read bytes of KSV list in FIFO (TPI 0x42)
7	host → TPI: Select V* value to read (TPI 0x31) host ← TPI: Read V* value (TPI group 0x32–35) Repeat until finished.
8	host: Calculate V value from repeater information and KSV lists read, and compare with V* for a match.
9	host: Check for revoked keys.

General Programming Registers

The TPI register set in transmitter applications provides access to data structures through the following register groups.

- Identification
- Video Mode
- Audio Configuration
- Power State Management
- HDCP
- Interrupt Service
- CTRL Bus (Mobile HD Link devices only – described in Appendix B)

Figure 2 illustrates how the TPI subsystem presents a register interface of several local configuration and operational register groups to the host. The example shows an HDCP-capable transmitter; the logic for a non HDCP-capable transmitter is similar, but omits the HDCP blocks.

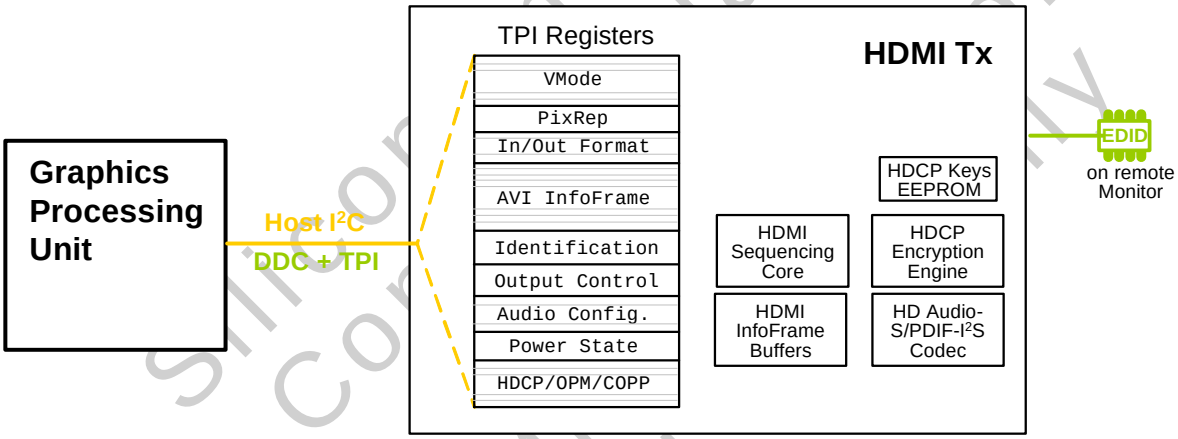


Figure 2. Transmitter TPI Register Interface to Host

The sections below describe the interaction required by the host to set up and operate the HDMI platform.

Important Notes

These notes are mentioned elsewhere but are repeated here for clarity.

1. After a hardware reset, it is necessary to enter TPI mode. **Write** device address **0x72,** register offset **0xC7 = 0x00** to enter TPI mode.
2. Once in TPI mode, all TPI registers referenced are accessed at I^2C device address **0x72**.

Identification

The ID registers return the device ID and TPI revision ID. The ID registers are listed in Table 4. HDCP-capable and non HDCP-capable transmitters are distinguishable only by reading the HDCP revision register (TPI 0x30).

Access. These registers are accessed as single bytes.

Table 3. TPI Identification Registers (RO)

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1B	Device ID Refer to Table 4							
0x1C	Device Production Revision ID revision level (major.minor) Refer to Table 4							
0x1D	TPI Scheme 0=Hardware (always) 1=Software	TPI revision level (major.minor) Refer to Table 4						

Table 4. Device ID Information

Device	Device ID TPI 0x1B	Device Production Revision ID TPI 0x1C	TPI Revision ID TPI 0x1D	HDCP Revision TPI 0x30
SiI9022 Tx	0xB0	0x00	0x00	0x00
SiI9022A Tx	0xB0	0x02	0x03	0x00
SiI9024 Tx	0xB0	0x00	0x00	0x12
SiI9024A Tx	0xB0	0x02	0x03	0x12
SiI9136/9334 Tx	0xB4	0x20	0x30	0x12
Mobile HD Link Tx	Refer to Appendix B			

Video Configuration

Setup for the incoming video resolution at minimum requires video mode and AVI InfoFrame data. The registers below describe the interface; refer also to the source code provided with the Starter Kit.

Video Mode

The host notifies TPI of its intended resolution through the following read/write registers.

Note: This information must be written for both HDMI mode and DVI mode operation.

Basic Video Mode Data

The video host provides the video mode data listed below. TPI requires that these values be set for proper operation.

Access. These registers can be read or written individually or by bursts as desired. The actual write to the HDMI transmitter registers takes place only once the final byte of the burst is written.

Table 5. TPI Video Mode Data (R/W)

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00 [00]	PixelClock Pixel Clock / 10000 – LSB							
0x01 [00]	MSB							
0x02 [00]	VFreq Vertical Frequency in Hz – LSB							
0x03 [00]	MSB							
0x04 [00]	Pixels Total Pixels per line – LSB							
0x05 [00]	MSB							
0x06 [00]	Lines Total Lines – LSB							
0x07 [00]	MSB							

PixelClock. The logic uses this value to configure the internal PLL circuitry for optimal operation at the incoming frequency.

VFreq. For the SiI9136, SiI9334, and SiI9232 transmitters with HDCP, the logic uses this value to correctly time HDCP authentication operations that are based on frame rates.

The input bus clocking format, along with clocking rate and edge, are specified in this register. The video host also indicates the pixel repetition factor here. Refer to the Format Matching section below for an example.

Access. This register is accessed as a single byte. Except for the SiI9136/9334 Tx, it must be written **after** TPI 0x1A[4] is set to 0, also any time TPI 0x1A[4] goes from 1 to 0, TPI 0x08[3:0] will be reset to their default state.

Table 6. TPI Input Bus and Pixel Repetition Data (R/W)

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x08 [60]	InputBusFmt							
	TClkSel[1] Ratio of output TMDS clock to input video clock 00 – x0.5 01 – x1 (default) 10 – x2 11 – x4		Input Bus Select 0 – half-pixel wide 1 – full pixel wide (default)	Edge Select 0 – Falling edge 1 – Rising edge	PR3:0 Pixel Repetition Factor[2] 0000 – Pixel data is not replicated 0001 – Pixels are sent two times each 0011 – Pixels are sent four times each All others – Rsvd			

Note

1. TClkSel is not available here on the SiI9022 or SiI9024 Tx (non "A" versions). The bits default to 00 in those parts.
2. PR3:0 are cleared whenever TPI 0x1A[4] goes from 1 to 0.

Input Bus Select. The input data bus can be either one pixel wide or ½ pixel wide. The bit defaults to 1 to select full pixel mode. In ½ pixel mode, the full pixel is brought in on two successive clock edges (one rising, one falling). All parts support 24-bit full-pixel and 12-bit half-pixel input modes.

The SiI9136/9334 Tx additionally supports 30- and 36-bit full-pixel and 15-, 18-, and 24-bit half-pixel input modes. The corresponding color depth is selected at TPI 0x09[7:6].

Edge Select. Input data is latched on the selected rising or falling clock edge. For ½ pixel mode, this bit indicates when = 0 that data present at the falling edge is latched first, and when = 1, data present at the rising edge is latched first. The high-order bits are latched first.

TClkSel. If the video host drives in data using anything other than a 1:1 ratio of input clock speed to TMDS clock speed, the host must program the clock multiplier logic. Refer to the Format Matching section below for an example.

→ **Exception.** Most devices can access these bits directly as shown in Table 6. For SiI9022/SiI9024 (non "A" version) devices, set the clock management subsystem to the correct ratio using the following sequence.

```
a) Write 0xBC=0x01                  // Internal page 1
b) Write 0xBD=0x82                  // Indexed register 82
c) Read 0xBE                        // Read current value
d) Modify bits[6:5] = TClkSel       // Change only the identified bits
e) Write 0xBE                       // Write back modified value
```

Table 7. TPI Frequency Multiplication Ratio (R/W)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Internal Register available at 0xBE when: 0xBC=01 0xBD=82	Rsvd – write as read.	TClkSel Ratio of output TMDS clock to input video clock 00 – x0.5 01 – x1 (default) 10 – x2 11 – x4		Rsvd – write as read.				

Format Matching

For certain combinations of video input clock frequency and audio sampling rate, the HDMI transmitter must use a higher multiple of the input pixel clock when sampling the S/PDIF input.

Set PR3:0 to reflect the pixel replication factor of the input data stream so that it is properly decoded. `TClkSel` indicates the factor by which the input clock (IDCK) must be multiplied to yield the output clock frequency. These settings ensure that the output clock can provide sufficient bandwidth for multi-channel audio data on an HDMI link. The pixel replication count bits in the AVI InfoFrame Packet must be accurate. Refer to Table 8 for an example based on the 480p instance cited in section 7.3 of the *HDMI Specification version 1.3a*.

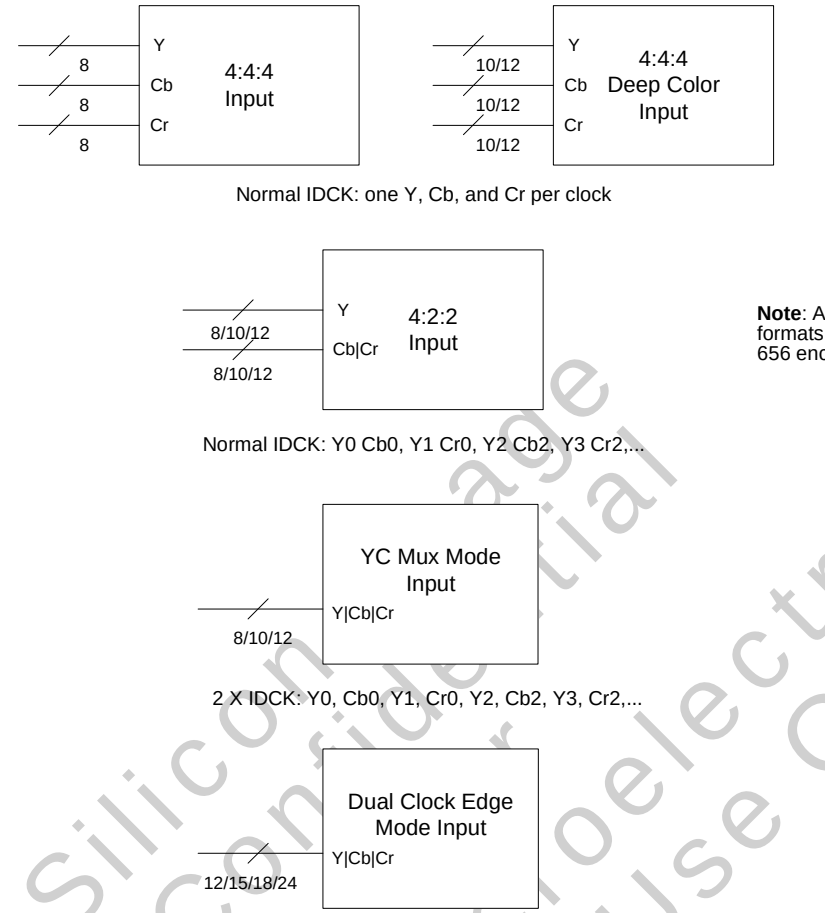
Table 8. 480p Mode Format Matching Example

Input Clock	Write to TPI 0x01:00 (decimal)	Audio Mode & max f_s	TPI 0x08 PR3:0 Pixel rep.	YC Mux Mode (TPI 0x60[5])	`TClkSel` (refer to previous page)	Output Pixel Rep.	Resulting TMDS Link Clock	AVI InfoFrame Packet Byte 5 bits PR3:PR0
54MHz	5400	8 ch, 96kHz	0b01 (2x)	0	01 (1.0)	2x[7]	54MHz[6]	0b0001
54MHz	5400	2 ch, 192kHz	0b01 (2x)	0	00 (0.5)	1x	27MHz	0b0000
54MHz	5400	8 ch, 96kHz	0b00 (1x)	1[5]	01	2x[7]	54MHz[6]	0b0001
54MHz	5400	2 ch, 192kHz	0b00 (1x)	1[5]	00	1x	27MHz	0b0000
27MHz	2700	8 ch, 96kHz	0b00 (1x)	0	0b10 (2.0)	2x[7]	54MHz[6]	0b0001
27MHz	2700	2 ch, 192kHz	0b00 (1x)	0	0b11 (4.0)	4x[8]	108MHz	0b0011
27MHz	2700	8 ch, 48kHz	0b00 (1x)	0	0b01 (1.0)	1x[9]	27MHz	0b0000

Notes

1. Input Clock (IDCK) and the TMDS Link Clock must be within the min/max range for the HDMI transmitter.
2. For proper decoding, set PR3:0 to reflect the pixel replication factor of the input data stream.
3. `TClkSel` selects the factor by which the input clock must be multiplied to give output clock frequency.
4. There is only one pixel per 27 MHz clock cycle, so each must be replicated.
5. When YCbCr 4:2:2 data is multiplexed onto a single channel, the input clock must be doubled.
6. 54 MHz is necessary so that the blanking intervals have sufficient bandwidth to carry the 8-channel audio data sampled at frequencies up to 96 kHz.
7. Because the output clock has been doubled, pixels must be replicated.
8. Illustrates 4x pixel replication on output.
9. 27 MHz input clock provides sufficient bandwidth for 8-channel audio data sampled at frequencies 48 kHz and below. Refer to the *HDMI Specification*.
10. Bits PR0:PR3 of Byte 5 of the AVI InfoFrame packet indicate to the HDMI sink how many repetitions of each unique pixel are transmitted. Refer to the *CEA-861-E Specification*.

These settings ensure that the output clock provides sufficient bandwidth for multi-channel audio data on an HDMI link (25 MHz minimum).



Note: All input bus formats shown can use 656 encoded syncs.

Figure 3. Input Bus Diagram for Different Formats

Input and Output Format

`InputFormat` and `OutputFormat` are used by the host to specify the data format and range. At a reset event, the chip defaults set input and output to be full-range RGB.

To set these registers, the host should read the EDID to determine whether the sink is DVI or HDMI, and what its preferred output format is. Once written, the selection remains until overwritten or until the next reset event.

Input Color Space / Output Format. These bits should be set as needed. Note that the settings made to these bits do not take effect until the AVI InfoFrame registers are programmed, so that any color space change can be synchronized to the color settings specified in the InfoFrame (avoiding temporarily green or pink images).

Range Compression. Range compression is enabled when RGB input and YCbCr output conversion is selected.

Range Expansion. Range expansion is enabled when YCbCr input and RGB output conversion is selected

Range Override. Range Expansion is associated with the Input Format; the Range bits either force expansion (01) or block it (10). Range Compression is associated with the Output Format; the Range bits either block compression (01) or force it (10).

Input Color Depth. This setting selects the incoming bus width to allow for proper handling on output. Note that only two YCbCr input bus widths, 8-bit and 12-bit, are possible. For 4:2:2 inputs 9, 10, or 11 bits wide, the host should set 0x09[7:6]=11 (12 bits), and drive unused bits of the video stream to 0.

Black Mode. This setting disables the video data input bus, forcing the video output to black (as long as valid video clock and control inputs are still available). This setting should not be used when HDCP is enabled, as the screen will show snow.

Access. These registers can be accessed individually or by bursts as desired. For writes, the actual write to the HDMI transmitter logic takes place only once the final byte of the burst write to TPI 0x0C-19 occurs (refer to Input Color Space / Output Format note above).

Table 9. TPI AVI Input and Output Format Data (R/W)

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x09 [00]	InputFormat							
	Input Color Depth[1] 00 – 8-bit 01 – 16-bit[2] 10 – 10-bit (10/12-bit un-dithered for 4:2:2 mode) 11 – 12-bit (10/12-bit dithered to 8, for 4:2:2 mode)		Rsvd		Video Range Expansion 00 – Auto-selected by [1:0] 01 – On 10 – Off 11 – Rsvd		Input Color Space 00 – RGB 01 – YCbCr 4:4:4 10 – YCbCr 4:2:2 11 – Black Mode [3]	
0x0A [00]	OutputFormat							
	Output Color Depth [2] 00 – 8-bit (also used for 4:2:2 mode) 01 – 16-bit 10 – 10-bit 11 – 12-bit		Dither from Input Depth to Output Depth[2] 0 – Disable 1 – Enable	Color Space Standard 0 – BT.601 conversion 1 – BT.709 conversion	Video Range Compression 00 – Auto-selected by [1:0] 01 – Off 10 – On 11 – Rsvd		Output Format 00 – RGB 01 – YCbCr 4:4:4 10 – YCbCr 4:2:2 11 – RGB (same as 00)	

Notes

1. These bits were formerly described as Extended and Dither.
2. Applies only to devices capable of Deep Color output (SiI9136/9334 Tx). See notes below.
3. For the SiI9136/9334, the blanking levels for Black Mode vary based on color space and video range. Before setting TPI 0x09[1:0] = 3, set the TPI Video Mute Registers, TPI 0x4A through TPI 0x4F.

Deep Color Operation (SiI9136/9334 Tx only). Deep color settings can be used where supported by the HDMI sink device. The following additional configuration is required.

General Control Packet – Deep color settings require the General Control Packet to be sent once per video field with the correct PP and CD information. This must be enabled by software via TPI Deep Color Packet Enable Register 0x40[2] = 1, enable transmission of the GCP packet.

Output Color Depth – This setting selects the color depth for the HDMI output stream, and also selects the corresponding HDMI protocol handling. It should be left at 8-bit for YCbCr 4:2:2 modes, as well as for any non deep-color mode of operation. Unlike the other bits in this register, any output color depth setting change takes place immediately and is not dependent on a write to the AVI InfoFrame registers.

Note 1: Selecting any deep color output mode is done directly through TPI 0x0A[7:6]. However, if it is later necessary to switch back to 8-bit color depth, switch to 16-bit deep color first, and then to 8-bit color depth.

Dither from Input Depth to Output Depth – When the incoming data contains greater color depth than the attached HDMI source is capable of handling, this bit can be set to dither the HDMI output based on the least significant bits of the input, and thereby achieve greater color accuracy. For example, if TPI 0x09[7:6]=01, 16-bit input depth, and TPI 0x0A[7:6]=10, 10-bit output depth, setting 0x0A[5]=1 will dither from 16-bit input to 10-bit output depth.

Video Mute Operation (SiI9136/9334 Tx only). The Black Level data is related to the Video Input Mode (RGB / YCbCr 444, YCbCr422) and Input width (8, 10, 12, 16) and programmable.

Table 10. TPI Video Mute Registers (R/W)

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Cb component / Blue component							
0x4A	Cb [7:0] / B [7:0]							
0x4B	Cb [15:8] / B [15:8]							
	Y component / Green component							
0x4C	Y [7:0] / G [7:0]							
0x4D	Y [15:8] / G [15:8]							
	Cr component / Red component							
0x4E	Cr [7:0] / R [7:0]							
0x4F	Cr [15:8] / R [15:8]							

For Black Level Settings:

Input 720p RGB and Output YCbCr (8 bit) a Black Level can be achieved via the following settings:

```
1. TPI 0x4B, 0x4A = 0x0000      // B [15:0]
2. TPI 0x4D, 0x4C = 0x0000      // G [15:0]
3. TPI 0x4F, 0x4E = 0x0000      // R [15:0]
```

Input 720p YCbCr and Output YCbCr (8 bit) a Black Level can be achieved via the following settings:

```
1. TPI 0x4B, 0x4A = 0x8000      // Cb [15:0]
2. TPI 0x4D, 0x4C = 0x1000      // Y [15:0]
3. TPI 0x4F, 0x4E = 0x8000      // Cr [15:0]
```

Output color space control (SiI9334 and SiI9136)

Since it is optional for a sink to support AV Mute packets, HDMI transmitters need to output correct blanking levels during AV Mute packets. This can be accomplished using the following sequence:

```
1) Write 0xBC=0x01                  // Internal page 1
2) Write 0xBD=0x4B                  // Indexed register 0x4B
3) Write 0xBE=Blank1                // Blue/Cb channel value (MSB)
4) Write 0xBD=0x4C                  // Indexed register 0x4B
5) Write 0xBE=Blank2                // Y/G channel value (MSB)
6) Write 0xBD=0x4D                  // Indexed register 0x4B
7) Write 0xBE=Blank1                // Red/Cr channel value (MSB)
Blank1 value is 0x00 for full range RGB, 0x10 for limited range RGB, 0x80 for YCbCr.
Blank2 value is 0x00 for full range RGB, 0x10 for limited range RGB and YCbCr.
```

Input Setup Operations

Programming setup for the device is straightforward. A typical startup configuration sequence is shown below.

Write:

```
1. 0x00=0x00   // Set pixel rate for 74.24MHz (7424 = 0x1D00)
2. 0x01=0x1D   //
3. 0x1A=0x11   // Disable TMDS output
4. 0x1E=0x00   // Enter full-operation D0 state
5. 0x26=0x50   // Set to S/PDIF, Mute
6. 0x25=0x03   //
7. 0x27=0x00   //
8. 0x26=0x40   // Unmute S/PDIF
9. 0x1A=0x01   // Enable TMDS output
```

Sync Generation Options

For input video modes that do not provide explicit HSYNC, VSYNC, and/or DE signals, the transmitter logic offers two methods for sync signal generation:

- DE Generation (when explicit HSYNC and VSYNC signals are provided)
- Sync Extraction (when incoming video uses the ITU 656 method for embedding sync information).

The register sets for both modes overlap, so only one can be accessed at a time. However, by toggling between the two groups, features from both can be intermixed.

The dual data paths are shown in Figure 4, with the path for embedded sync extraction highlighted. When decoding syncs from the embedded sync stream, the DE Generator block should be disabled through TPI 0x63[6].

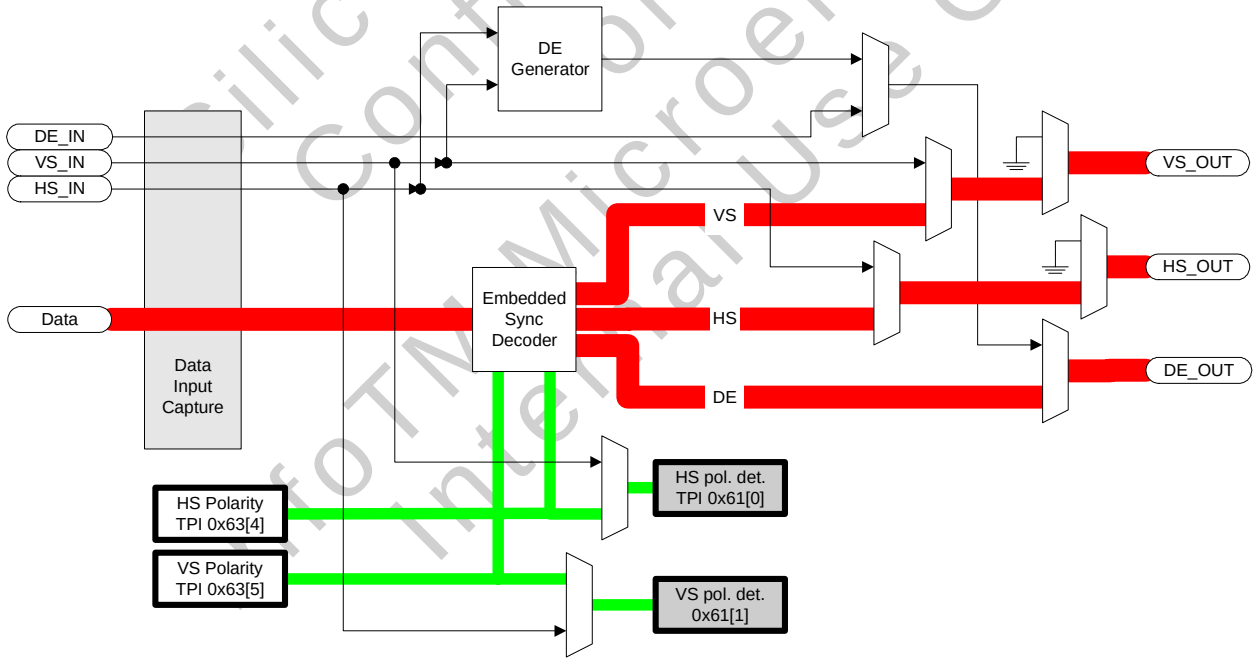


Figure 4. Transmitter Video Data with Sync Decoding

The registers available at 0x62–0x6F depend on the setting of TPI 0x60[7].

- Setting TPI 0x60[7] = 0 selects external sync and access to the DE Generator registers. The DE signal can be generated internally and sent over TMDS if TPI 0x62–6D are set and then TPI 0x63[6] is set to 1.
- Setting TPI 0x60[7] = 1 allows access to the Embedded Sync Extraction registers. The DE, HSYNC, and VSYNC signals can then be extracted and sent over TMDS if TPI 0x62–69 are set and then TPI 0x63[6] is set to 1.

Features from both groups can be enabled together, by enabling the features of each group with TPI 0x60[7] set appropriately.

Access. These registers are accessed as single bytes or as part of a burst.

→ **Important Note:** TPI 0x60 must be written **after** the AVI InfoFrame is set. Any time TPI 0x19 is written, TPI 0x60[5] will be reset to its default state. The SiI9136/9334 does not require TPI 0x60 to be written after the AVI InfoFrame.

Table 11. Sync Register Configuration and Sync Monitoring Registers

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x60 [04]	Sync Generation Control Register							
	Sync Method 0 – External 1 – Embedded	Rsvd	YC Mux Mode One- to two-data-channel de-mux 0 – Disable 1 – Enable	Invert Field Polarity 0 – Leave bit as is 1 – Invert field bit	Rsvd	DE_ADJ# 0 – Enable (recom-mended) 1 – Disable (default)	F2VADJ Adjust VBIT to VSYNC per bit [0] 0 – Disable (default) 1 – Enable	F2VOFST Adjust VBIT to VSYNC if bit [1] = 1 0 – Decrement by 1 1 – Increment by 1
0x61 [00]	Video Sync Polarity Detection Register (RO)							
	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Interlace Mode detected 0 – non interlaced 1 – interlaced	Input VSYNC polarity detected 0 – active high (leading edge rises) 1 – active low (leading edge falls)	Input HSYNC polarity detected 0 – active high (leading edge rises) 1 – active low (leading edge falls)

DE_ADJ# enables detection circuits to locate the position of VSYNC relative to HSYNC and only include HSYNC edges that are greater than ¾ lines from VSYNC in the line count for DE_TOP. Clearing this bit enables the function and is recommended for normal operation. Setting it high disables VSYNC adjustments and is not a recommended setting.

F2VADJ adjusts the VBIT_TO_VSYNC value during field 2 of an interlace frame; **F2VOFST** sets the direction of adjustment (increment or decrement by 1).

Invert Field Polarity. The Invert Field Polarity bit is used when the 656 Flag Bit is opposite the standard polarity for Field1 and Field2. Inverting polarity causes the sync extraction to format HSYNC and VSYNC properly based on the 'F' bit. In embedded sync mode, the transmitter does not detect 'even' from 'odd' field, except based on the setting of the 'F' bit. With explicit syncs, the transmitter simply encodes HSYNC and VSYNC across the HDMI/TMDS link without regard for field sequence.

YC Mux Mode

When YCbCr 4:2:2 data is multiplexed onto a single channel (YC Mux mode), the input clock rate from the host must be doubled. The one- to two-data-channel de-mux feature is used to decode the incoming data accordingly. When using YC Mux mode (TPI 0x60[5]=1), the input data can be additionally manipulated using the register controls provided below.

Table 12. TPI YC Input Mode Select [1] (R/W)

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0B [00]	Swap MSB and LSB within each data channel. [4] ("A" only) 0 – Disable 1 – Enable	Video Input DDR Select[2] 0 – Lower 12 bits 1 – Upper 12 bits	Rsvd	Rsvd	Non Gap Mode 0 – Disable 1 – Enable	YC Input Mode Select[3]. 000 – YC normal 001 – YC channel data swap 010 – YC 8-bit DDR input 011 – YC 8-bit DDR input, channel data swap 100 – YC 24-bit input in consecutive order All other values = Rsvd		

Notes

1. This register is not available in the SiI9022 and SiI9024 Tx (non "A" revisions).
2. The SiI9136/9334 Tx does not support this option.
3. The SiI9136/9334 Tx supports only the 000 and 001 options. The SiI9136/9334 Tx YC channel data swap (YC Input Mode Select, bits[2:0]) control does not require YC Mux Mode Channel swapping to be enabled (TPI 0x60[5]=1).
4. The SiI9136/9334 Tx bit swapping (Swap MSB and LSB within each data channel, bit [7]) control does not require YC Mux Mode Channel swapping to be enabled (TPI 0x60[5])=1).

Swap MSB and LSB swaps the most significant and least significant bytes of the incoming data. This feature is not supported in YC Mux Mode.

Video Input DDR Select chooses the pins on which 12-bit DDR video will arrive.

- Lower 12 bits D11:0 are the default input path.
- Upper 12 bits D23:12 are available as an optional input path, for the SiI9022A and SiI9024A devices only.

YC Input Mode Select adds new input bus formats when using YC Input modes. Refer to SiI9022A/SiI9024A HDMI Transmitter Data Sheet (SiI-DS-1053) for details.

- "YC channel data swap" reverses the order of data on the 1st and 2nd clocks, normally C-then-Y, to Y-then-C.
- "YC 8-bit DDR input" enables double-data-rate clocking, so that the C data comes on the rising (or falling) clock edge, and Y data on the falling (or rising) clock edge.
- "YC 8-bit DDR input, channel data swap" enables both DDR and swap, so that the Y data comes on the rising (or falling) clock edge, and C data on the falling (or rising) clock edge.
- "YC 24-bit input in consecutive order" enables full data input of all 24 bits on a single clock edge.

DE Generator Register Set

The DE Generator registers are accessible only when TPI 0x60[7] = 0.

The transmitter provides an explicit sync DE generator that allows the Data Enable (DE) signal, required to be encoded in the TMDS output, to be derived from the incoming HSYNC and VSYNC signals. When programmed through TPI registers 0x62–6D, the output DE is generated based on the values in the DE generator registers and the arrival times of the HSYNC and VSYNC pulses from the video source. These registers are used only for DE generation and do not affect HSYNC or VSYNC.

The registers are shown diagrammatically in Figure 5. The vertical sync pulse (VSYNC) occurs in the top area of the frame, before the active video area. The active (leading) edge is shown with an arrow. The horizontal sync pulse (HSYNC) occurs every line before the active video area during the DE_DLY time. The active (leading) edge of HSYNC is shown with an arrow. (Note that VSYNC and HSYNC widths are not shown to scale.)

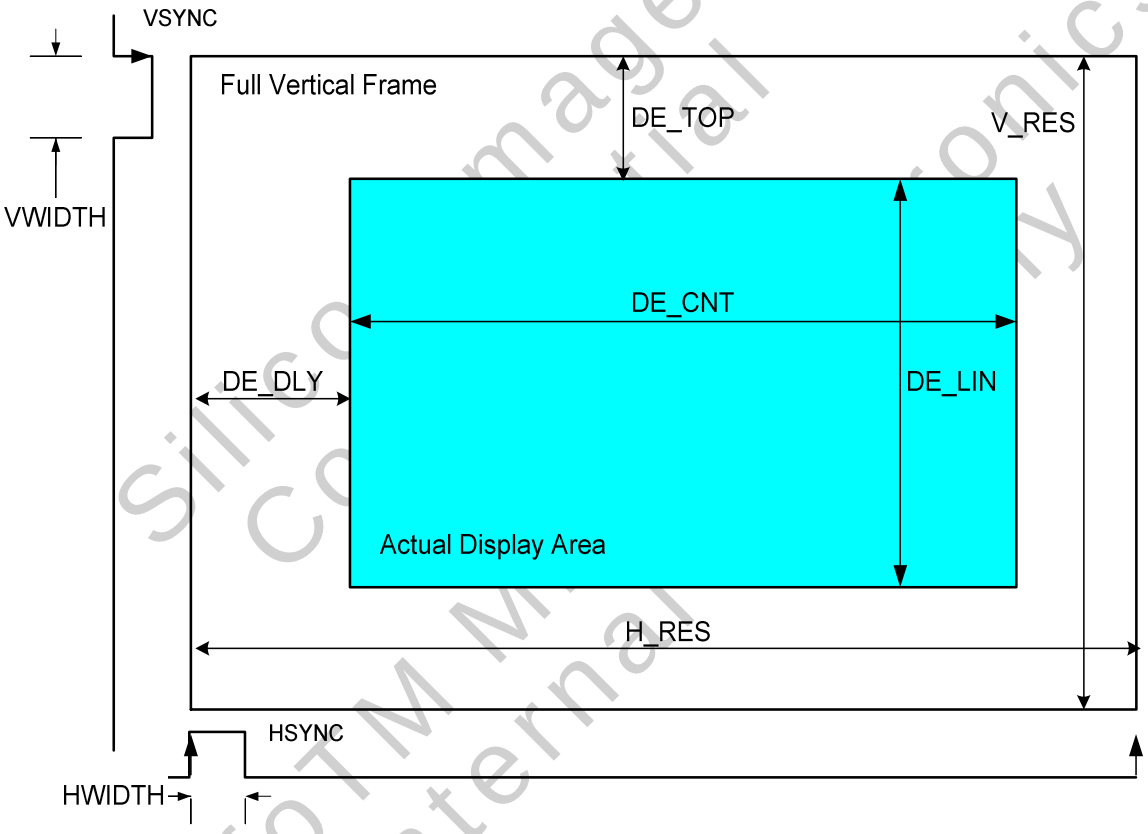


Figure 5. DE Generator Measurements

In the following definitions, 'pixels' is used to mean 'unique pixels'. The counts in the DE Generator registers, if expressed in 'pixels,' are counted according to the original clock, even if that original input clock is multiplied internal to the chip. For example, a 480i field will contain 720 unique pixels per line in the active video area, even when the clock is multiplied to 1440 clock cycles per active video time.

Default. The DE Generator defaults to 'disabled' after reset.

Access. These registers can be read or written individually or by bursts as desired. All are read/write except as noted.

Table 13. Explicit Sync DE Generator Registers (TPI 0x60[7] = 0)

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x62 [00]	DE_DLY[7:0]							
0x63 [00]	Rsvd	DE Generator 0 – Disable 1 – Enable	VSYNC Polarity: 0 – Positive (leading edge rises) 1 – Negative (leading edge falls)	HSYNC Polarity: 0 – Positive (leading edge rises) 1 – Negative (leading edge falls)	Rsvd	Rsvd	DE_DLY[9:8]	
0x64 [00]	Rsvd	DE_TOP[6:0]						
0x65 [00]	Rsvd							
0x66 [00]	DE_CNT[7:0]							
0x67 [00]	Rsvd			DE_CNT[12:8]				
0x68 [00]	DE_LIN[7:0]							
0x69 [00]	Rsvd				DE_LIN[11:8]			
0x6A [00]	H_RES[7:0] (RO) – Measures the time between two HSYNC active edges. Unit of measure is pixels.							
0x6B [00]	Rsvd			H_RES[13:8] (RO)				
0x6C [00]	V_RES[7:0] (RO) – Measures the time between two VSYNC active edges. Unit of measure is lines.							
0x6D [00]	Rsvd				V_RES[11:8] (RO)			

DE_DLY[9:0] set the width of the area to the left of the active display. Unit of measure is pixels. This register should be set to the sum of (HSYNC width) + (horizontal back porch) + (horizontal left border), and is used only for DE generation. Valid range is 1–1023. 0 is invalid.

HSYNC and VSYNC Polarity bits 0x63[5:4] should be set to the polarity of the source providing the sync signals. Setting these bits does not change the polarity of HSYNC or VSYNC in the encoded TMDS output stream.

DE_TOP[6:0] define the height of the area above the active display. The unit of measure is lines (HSYNC pulses). This register should be set to the sum of (VSYNC width) + (vertical back porch) + (vertical top border). Valid 1–127. 0 is invalid.

DE_CNT[12:0] define the width of the active display. Unit of measure is pixels. This register should be set to the desired horizontal resolution. The DE_CNT is 12 bits (valid values are 1 through 2047, 0 is invalid) for parts that support HDMI 1.3. The DE_CNT is 13 bits (valid values are 1 through 8191, 0 is invalid) for parts that support HDMI 1.4, see Appendix D.

DE_LIN[11:0] define the height of the active display. The unit of measure is lines (HSYNC pulses). This register should be set to the desired vertical resolution. The DE_LIN is 11 bits (valid values are 1 through 2047, 0 is invalid) for parts that support HDMI 1.3. The DE_LIN is 12 bits (valid values are 1 through 4095, 0 is invalid) for parts that support HDMI 1.4, see Appendix D.

H_RES [13:0] and V_RES [11:0] measure the time between two sync active edges and may vary slightly from one reading to the next. The values in these registers are accurate only when there are active HSYNC and VSYNC controls arriving on the video input. The H_RES is 12 bits (valid values are 1 through 4095, 0 is invalid) for parts that support HDMI 1.3. The H_RES is 14 bits (valid values are 1 through 16383, 0 is invalid) for parts that support HDMI 1.4, see Appendix D.

Embedded Sync Register Set

The Embedded Sync Extraction registers are available only when TPI 0x60[7] = 1.

The transmitter provides logic to extract ITU 656 encoding from the video stream.

Table 14. Embedded Sync Extraction Registers (TPI 0x60[7] = 1)

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x62 [00]	HBIT_TO_HSYNC[7:0]							
0x63 [00]	Rsvd	Embedded Sync Extraction[1] 0 – Disable 1 – Enable	VSYNC Polarity:[2] 0 – Positive (leading edge rises) 1 – Negative (leading edge falls)	HSYNC Polarity:[2] 0 – Positive (leading edge rises) 1 – Negative (leading edge falls)	Rsvd		HBIT_TO_HSYNC[9:8] [1]	
0x64 [00]	FIELD2_OFST[7:0]							
0x65 [00]	Rsvd			FIELD2_OFST[12:8]				
0x66 [00]	HWIDTH[7:0]							
0x67 [00]	Rsvd						HWIDTH[9:8]	
0x68 [00]	Rsvd		VBIT_TO_VSYNC					
0x69 [00]	Rsvd		VWIDTH					

Note

1. The Embedded Sync Mode information at TPI 0x63 is always reset to its default disabled state whenever AVI InfoFrame register TPI 0x19 is written. Therefore, if embedded sync video input is being used, TPI 0x63 must be re-written after any write to TPI 0x19.
2. Vsync and Hsync Polarity settings are only available in the Embedded Sync Extraction Registers for the SiI9136/9334. To change Vsync and Hsync Polarity settings on parts other than the SiI9136/9334 use the following sequence:
   a. Switch to Explicit Sync DE Generator configuration (TPI 0x60[7]=0).
   b. Modify Vsync and Hsync polarity (TPI 0x63[5:4]).
   c. Switch back to Embedded Sync Extraction configuration (TPI 0x60[7]=1).

The settings described below are useful only when the input video uses 656 encoded syncs. 0 is an invalid setting for all these parameters.

HBIT_TO_HSYNC[9:0] create HSYNC pulses. Set register to the delay from the detection of an EAV sequence (H bit change from 1 to 0) to the active edge of HSYNC. Unit of measure is pixels. Valid 1–1023.

FIELD2_OFST[11:0] determine VSYNC pixel offset for the odd field of an interlaced source. Set this to half the number of pixels/line. Valid 1–4095.

HWIDTH[9:0] set the width of the HSYNC pulses. Set the register to the desired HSYNC pulse width. Unit of measure is pixels. Valid 1–1023.

VBIT_TO_VSYNC sets the delay from the detection of V bit changing from 1 to 0 in an EAV sequence, to the asserting edge of VSYNC. Unit of measure is lines. Valid 1–63.

VWIDTH sets the width of the VSYNC pulse. Unit of measure is lines. Valid 1–63.

HSYNC and VSYNC Polarity bits 0x63[5:4] should be set to the polarity of the source providing the sync signals. Setting these bits does not change the polarity of HSYNC or VSYNC in the encoded TMDS output stream.

InfoFrame Data

The transmitter register map provides simplified direct access to the commonly used AVI InfoFrame registers, and a separate overlay register space for all the other InfoFrame registers.

AVI InfoFrame Data

A dedicated AVI InfoFrame buffer is provided to meet HDMI requirements for transmission every 2 frames. The host fills in the AVI InfoFrame according to the HDMI 1.x specification. This data is used only for transmission, and is not used for any internal register control purposes.

Access. These registers can be read or written individually or by bursts as desired. The data sent out on the link gets updated only when TPI 0x19 is written, either by itself or as the last byte of a burst. Writing TPI 0x19 also causes the values last written to TPI 0x09-0A to be loaded into the chip logic.

> → **Important Note:** After switching to a DVI mode by using TPI 0x0A[1:0], at least the one byte at TPI 0x19 **must** be written in order for the mode switch to take place.

Certain devices support HDMI 1.4 modes as noted in Appendix D, and require AVI InfoFrame bits to be set appropriately.

Table 15. TPI AVI InfoFrame Data (R/W)

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0C [00]	AVI_DBYTE0 AVI InfoFrame Checksum							
0x0D [00]	AVI_DBYTE1							
	Rsvd (0)	Y1:0 RGB/YCbCr Indicator		A0 Active info	B1:0 Bar Info Data Valid		S1:0 Scan Information	
0x0E [00]	AVI_DBYTE2							
	C1:0 Colorimetry Info		M1:0 Picture Aspect Ratio		R3:0 Active Format Aspect Ratio			
0x0F [00]	AVI_DBYTE3							
	ITC IT Content	EC2:0 Extended Colorimetry			Q1:0 RGB Quantization Range		SC1:0 Non Uniform Scaling	
0x10 [00]	AVI_DBYTE4							
	Rsvd (0)	VIC6:0 Video Format Identification Code						
0x11 [00]	AVI_DBYTE5							
	YQ1:0 YCC Quantization Range		CN1:0 Content Type		PR3:0 Pixel Repetition Factor			
0x12 [00]	EndTopBar Line Number of End of Top Bar – LSB							
0x13 [00]	MSB							
0x14 [00]	StartBottomBar Line Number of start of Bottom Bar – LSB							
0x15 [00]	MSB							
0x16 [00]	EndLeftBar Pixel Number of End of Left Bar – LSB							
0x17 [00]	MSB							
0x18 [00]	EndRightBar Pixel Number of End of Right Bar – LSB							
0x19 [00]	MSB							

Calculating the Checksum. The host must calculate the checksum to include the InfoFrame identifier headers and the expected length byte, per the HDMI specification. The routine for generating the checksum is provided below.

```
byte CRC = 0x82 + 0x02 + 13; // Identifier code for AVI InfoFrame, length
byte TXAddr = AVI_IF_ADDR + 4;
byte i;
for(i = 1; i < 14; i++ )
      CRC += ReadByteHDMITXP1( TXAddr++ );
CRC = 0x100 - CRC;
regAVIInfoFrm[0]=CRC;
return CRC;
```

Other InfoFrame Data

The host writes miscellaneous InfoFrame information as needed to the packet buffers, according to the HDMI 1.x specification. Seven buffers are provided, selected according to TPI 0xBF[2:0]. This data is used only for transmission, and not for any internal control purposes.

Access. These registers can be read individually or by bursts as desired. For writes, they should be accessed as a complete group in a burst. The actual data is transferred to the HDMI transmitter logic only once the final byte of the InfoFrame is written, as determined by the length of the InfoFrame set in 0xBF[2:0]. Alternatively, individual bytes can be modified and then the updated data can be transferred by writing just to the final byte.

Table 16. TPI Miscellanous InfoFrame Data (R/W)

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xBF [00]	I-F_SELECT							
	Enable selected InfoFrame transmission 0 – not enabled (default) 1 – enable	Repeat selected InfoFrame transmission 0 – don't repeat (default) 1 – repeat each frame	Rsvd		Rsvd	Selects the InfoFrame to load (n=31 bytes except where noted) 000 - Reserved 001 – SPD or ACP 010 – Audio (n = 14 bytes) 011 – MPEG or GBD 100 – Generic 1 / ISRC1 101 – Generic 2 / ISRC2 110 – HDMI VSIF 111 – GBD (SiI9334/SiI9136 only)		
0xC0 [00]	I-F_TYPE							
	Type 0 – Packet 1 – InfoFrame	InfoFrame Type per CEA-861-E spec						
0xC1 [00]	I-F_VER							
	InfoFrame version per CEA-861-E spec							
0xC2 [00]	I-F_LENGTH							
	Rsvd = 0	Rsvd = 0	Rsvd = 0	InfoFrame length per CEA-861-E spec				
0xC3 [00]	DBYTE0							
	InfoFrame Checksum							
0xC4 [00]	DBYTE1							
	InfoFrame data byte 1							
0xC5 [00] . . **0xDD** [00]	DBYTE2.. DBYTEn-1							
	InfoFrame data bytes (0xCD is the last location for Audio InfoFrame)							
0xDE [00]	DBYTEn							
	Last InfoFrame data byte (for all except Audio InfoFrames)							

Select. The host chooses the InfoFrame to which the data corresponds, and sets the Enable and Repeat bits, in the `I-F_SELECT` byte. When the last byte (n) of that selected InfoFrame group is written, the Enable and Repeat bit settings originally written will take effect. This sequence allows the command, checksum, and data to be written as a continuous burst over the TPI I^2C interface, preventing a partially written InfoFrame from being sent.

Because there is a limited number of packet buffers, it may be necessary to alternate the buffers where appropriate. For example, ACP packets can be sent every 300ms normally, but interrupted on occasion to use the same buffer to send an SPD packet for identification of the source device.

Enable bit. Enables selected InfoFrame for transmission over HDMI. To enable transmission, write "1" into this bit. Once transmission is done, the hardware will reset it back to 0 unless the Repeat bit was also set.

Repeat bit. The Repeat bit causes the logic to repeatedly send the selected InfoFrame data each frame. When this bit is set along with Enable (bit [7]), hardware will try to send the InfoFrame once every vertical blanking period. Software has to disable this bit first to force clear of the Enable bit by the hardware.

Length. The length is calculated without including the type, version, length, or checksum bytes.

Calculating the Checksum. Refer to the previous section for an example of calculating the checksum, noting that the Identifier Code and Length values will change according to the specific InfoFrame being sent.

Using x.v.Color

All transmitters support sending video data in x.v.Color (xvYCC) format across HDMI. Refer to Appendix D for special color space conversion and GBD handling features of the SiI9136 and SiI9334 transmitters. For all other transmitters, color space conversion is not available; input video data must be provided in the correct x.v.Color format. The programming is the same as the YCbCr 4:4:4 mode of operation.

The Gamut Boundary Descriptor packet is written to the Miscellaneous InfoFrame buffer selected by TPI 0xBF [2:0]=011. This buffer is also designated for use with MPEG packets, but these are rarely required. Contact Silicon Image technical support for recommendations on sending both GBD and MPEG packets in the same system.

Extended Colorimetry Standards

All transmitters support sending video data in $sYCC_{601}$, $Adobe_{RGB}$, and $AdobeYCC_{601}$ formats across HDMI. These modes are passed through directly and are not processed by the transmitter. TPI 0x09 and 0x0A must both be set to the same mode (matching input color space and output format) to ensure that these modes are handled properly.

The EC, CN, and YQ bits of the AVI InfoFrame must be set according to the HDMI 1.4 specification when transmitting any of these formats.

System Control

TPI has the ability to determine certain system functional needs and act automatically to control operation. The System Control register configures these functions and also allows the host to override them when needed.

Table 17. TPI System Control (R/W)

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1A [10]	SystemControl							
	Rsvd – write as 0 always.	Link Integrity Mode 0 – Static 1 – Dynamic	Rsvd – write as 0 always.	TMDS Output Control 0 – Active 1 – Power down (default)	AV Mute 0 – Normal audio/video 1 – Mute HDMI audio/video at receiver	DDC Bus Request by host 0 – Host does not need to use DDC 1 – Host requests to use DDC	DDC Bus Grant by TPI Read: Status 0 – Bus not available 1 – Bus can be used by host Write: Force bus ownership 0 – TPI 1 – Host	Output Mode Select Write in Hot Plug Service Loop 0 – Set DVI 1 – Set HDMI

DDC Bus Request/Grant. TPI logic automatically utilizes the DDC bus as needed. If the host needs to use the DDC bus, it must notify TPI logic and then wait until it is safe to take the bus over. The host graphics software should use the DDC bus Request control and Grant status bits as follows.

1. Before performing a DDC bus access, the host writes 0x1A[2] = 1 to request the bus.
2. It then loops on a read of 0x1A[1] until it returns 1, indicating that it is safe to read the bus. In SiI9334 and SiI9136 this step has to be skipped if HDCP is enabled but video is muted while HDCP is enabled as the bus grant logic waits for Ri reading but the reading does not occur while video is mute. In mentioned above chips this step also can be skipped if HDCP is off.
3. Once it has been granted the bus, the host **must** write TPI 0x1A=0x06. This action closes the switch to allow subsequent I^2C accesses to flow out onto the DDC bus.
4. Once the host has finished reading EDID, it must write TPI 0x1A=00 to clear the request. Note that the device will **not** ACK this write.
5. Finally, the host must read 0x1A[2:1] and verify that they are 00 (repeat step 4 if not). Reading back from this register opens the switch to direct subsequent I^2C accesses back to the TPI bus.

If link security has been requested any time since the last hardware reset or hot plug event, HDCP link integrity checking will be taking place every 128 frames. Therefore, in order to receive full access, the host must **disable** link security before requesting use of the DDC bus.

Output Mode. During the Hot Plug Service Loop, before register 0x1E is written to 00 to select full-power operational mode, the DVI/HDMI control bit at 0x1A[0] must be written to force the mode of operation.

0 = DVI

1 = HDMI

Register 0x1A can be written and read multiple times while in the Hot Plug Service Loop, but for bit 0, only the last write made is important. After writing 0x1E = 00, the most recent setting of 0x1A[0] is used to establish the operating mode.

The transmitter subsystem will operate in the selected mode (DVI or HDMI) until the next hardware reset, or until the next time 0x1E is written to 0.

AV Mute. HDMI allows the display and audio output of the sink device to be muted by remote command. The host can send this command by using the AV Mute bit. This feature is useful when switching video resolutions, for example, to prevent the screen from flickering.

Important Notes

→ **1:** Once the system has been set to DVI output mode, the AV mute and un-mute packets can no longer be sent. Therefore, sending an AV Mute packet and then switching from HDMI to DVI output mode could result in a permanently muted screen until the next hardware reset.

→ **2:** Setting TPI 0x1A[3] sends an AV Mute command and temporarily disables HDCP encryption, as required for HDMI. However, as there is no concept of an AV Mute command for DVI, setting this bit when in DVI mode results only in disabling HDCP encryption. Therefore, in general, this bit should not be used in DVI mode. Setting this bit on the SiI9136/9334 does not disable HDCP.

TMDS Output Control. The transmitter TMDS outputs can be powered down, leaving them floating. TMDS output must be explicitly enabled with this bit after entering operational (D0) mode.

Link Integrity Mode. Not used for devices without HDCP. For details, refer to the HDCP section for devices with HDCP capability.

Resolution Change. Setting 0x1A[4] = 1 is a signal from the host that a resolution change is about to happen. The host should disable HDCP security using 0x2A[0], wait for at least 64ms or poll 0x29[7:4] to verify that it is disabled, then follow this procedure.

1. Disable TMDS Output (0x1A[4] = 1).
2. Wait at least 128ms to allow control InfoFrames to pass through to the sink device.
3. Change video resolution, and wait for the new resolution to stabilize.
4. Set the VMode registers.
5. Write the AVI InfoFrame registers (0x0C).
6. Enable TMDS Output (0x1A[4] = 0).

Upon completion, re-enable HDCP security if needed using 0x2A[0].

Audio Configuration

The audio subsystem can operate in S/PDIF or I^2S mode, S/PDIF, I^2S or DSD mode (DSD only SiI9136/9334), as selected by the host through TPI. In either case, the host determines which configurations are valid by reading the audio descriptors directly from the EDID.

Configuring Audio using S/PDIF

The S/PDIF audio subsystem selection is made by TPI control. Most operations thereafter are automatic.

S/PDIF Initialization and Operation

The transmitter requires only the following initialization for S/PDIF applications.

1. Ensure that a valid S/PDIF audio stream is coming into the transmitter.
2. Select S/PDIF input mode using register bits 0x26[7:6].

The transmitter supports automatic recognition of new S/PDIF audio rates when the correct header information is supplied in the S/PDIF stream. It continually checks the f_s value in the S/PDIF stream, and calculates N values accordingly whenever f_s changes.

For audio sources that do not supply correct S/PDIF stream headers, the information must be programmed manually as described in the Configuring Audio using I2S section.

Additional Audio Features

The following registers are provided for the host to select an audio mode. The default is Basic Audio, since HDMI hosts are always allowed to send Basic Audio even before reading the EDID descriptors. The Basic Audio configuration can always be selected.

Audio Muting. The Mute bit is used when the host has a specific need to temporarily turn off audio. It stops the audio stream to the audio FIFO, muting the audio. However, the audio module is still enabled, so that un-muting requires no additional re-initialization.

Audio Handling. Three modes are available.

- Pass Basic Audio Only. Incoming audio will be transmitted over HDMI only if is uncompressed (PCM) and is 32kHz, 44.1kHz, or 48kHz. All other streams are blocked and the output is muted.
- Pass All Audio Modes. The hardware transmits the audio stream over HDMI exactly as it is received.
- Down-sample Incoming Audio as Needed. The hardware uses the transmitter down-sampler to automatically detect and convert incoming high audio rates to their Basic Audio correspondent. For example, 192 kHz audio would always be down-sampled to 48 kHz before transmission over HDMI.

Note that for proper operation, the down-sampling feature requires that the incoming S/PDIF header information be correct.

Audio Override. By default, the incoming S/PDIF stream header is used by chip logic to automatically configure audio operation. Override bits are provided in registers 0x26 and 0x27 to manually set this information. Note that these bits must be used to set the correct output stream header when the Audio Handling bits in 0x25[1:0] = 10. Setting 0x27[5:3], in particular, will overwrite the incoming audio stream rate data on the outgoing audio packets. Setting the override bits does not affect the Audio InfoFrame information.

Access. These are byte-accessed registers. Refer to the following section for sequence information.

Table 18. TPI Audio Configuration Write Data (RW)

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x24[1] [D0] read-only	S/PDIF Header bits 35:32, Sample Length refer to IEC60958 specification				S/PDIF Header bits 27:24, Sample Frequency refer to IEC60958 specification			
0x25[1] [03]	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Audio Handling 00 – Pass Basic Audio only 01 – Pass all audio modes 10 – Down-sample incoming audio as needed 11 – Do not check audio stream (default)	
0x26 [00]	Audio Interface 00 – Disabled 01 – S/PDIF 10 – I^2S 11= DSD (SiI9136/9334 Tx only)		Layout Bit "A" & SiI9136/9334 revisions only: audio packet header layout indicator 0 – Layout 0 (2-channel) 1 – Layout 1 (up to 8 channels)	Mute 0 – Normal 1 – Mute	Audio Coding Type CT[3:0] (not used by chip logic) 0000 – Refer to Stream Header 0001 – PCM 0010 – AC-3 0011 – MPEG1 0100 – MP3 0101 – MPEG2 0110 – AAC 0111 – DTS 1000 – ATRAC all others are reserved			
0x27 [00]	Audio Sample Size SS[1:0] 00 – Refer to Stream Header 01 – 16-bit 10 – 20-bit 11 – 24-bit		Audio Sample Frequency SF[2:0] 000 – Refer to Stream Header 001 – 32kHz 010 – 44.1kHz 011 – 48kHz 100 – 88.2kHz 101 – 96kHz 110 – 176.4kHz (MCLK = 128 f_s) 111 – 192kHz (MCLK = 128 f_s)		High Bit-Rate (HBR) Audio Support[2] (SiI9136/9334 Tx only) 0 – Disable 1 – Enable	Rsvd	Rsvd	
0x28 [00]	Reserved							

Note

1. TPI 0x24 and 0x25 are specific to S/PDIF operating mode, and are available only when 0x26[7:6] = 01.
2. In previous TPI specifications, TPI 0x27[2:0] were assigned as Audio Channel Count bits [2:0], but were never used. These bits are now reassigned as noted.

Audio Configuration Overview. S/PDIF audio handling is fully automated with TPI. The audio logic automatically detects the incoming S/PDIF sampling frequency and makes the register settings to pass the audio through correctly. I^2S audio handling is nearly as automated; only the sampling frequency needs to be written since it is not available from header information.

The incoming audio data is raw data, which is not parsed in any way by the audio logic. Therefore, information such as audio sample size is not known. Therefore, the data written to 0x26 and 0x27 serves to inform the transmitter of the source choices and preferences.

A typical configuration sequence takes place after a Hot Plug event as follows.

1. The host requests and is granted the DDC bus, reads video and audio capabilities from the EDID ROM, and starts sending video at a supported resolution. It also passes sink audio information to the source audio handler.
2. The host audio subsystem sends 2-channel uncompressed audio at 48kHz and a 16-bit sample size, the minimum configuration required to be supported by all HDMI sinks. The audio logic passes this audio data through by default.

   Therefore, audio will be heard immediately at the sink device once the audio input type is selected.

3. The host audio application makes an appropriate audio mode choice. It writes:
    - register 0x26 with the Mute bit set
    - register 0x27 as required
    - register 0x26 again, this time with the Mute bit cleared and either S/PDIF or I^2S selected.
4. When it detects an unmute write to register 0x26, TPI sends Audio InfoFrames as required by HDMI.

Pixel Rate. Slower video pixel rates may not allow enough bandwidth to send compressed modes with high audio sample frequencies and high channel number counts. The only real example of this for CE applications is for 480p resolution, where 8-channel compressed audio is limited to a 48kHz sample frequency.

Therefore, when programming the TPI Audio Configuration registers, the host audio handler may need to eliminate any configurations that are not compatible with the current video mode. Note that high-definition CE modes of 720p, 1080i, and 1080p have pixel rates high enough to leave no restrictions on the audio selection.

The S/PDIF input logic automatically compensates for slow pixel rates with fast S/PDIF stream clocks by increasing the sampling rate.

HDMI Audio InfoFrame Requirements for S/PDIF Operation

Audio InfoFrame requirements in the HDMI specification are handled automatically for S/PDIF. As long as the S/PDIF stream carries all header information, the HDMI specification allows most Audio InfoFrame information to be set to 0 (the "Refer to Stream Header" selection). The only required information not carried in the stream header is the Speaker Configuration byte of the infoframe, which must always be set according to the CEA-861-E standard when more than two speakers are used. TPI assumes that S/PDIF headers are being provided correctly by the audio host.

Configuring Audio using I^2S

The I^2S audio subsystem selection is made by TPI control.

I^2S Initialization and Operation

The transmitter requires the following initialization for I^2S applications.

1. Ensure that a valid I^2S audio stream is coming into the transmitter.
2. Select I^2S input mode using register bits 0x26[7:6], with Mute enabled (bit [4] = 1).
3. Write register 0x20 to select the general incoming SD format.
4. Write register 0x1F up to four times, to program each of the SD inputs.
5. Program register bits 0x27[5:3] with the correct audio rate.
6. Program registers 0x21–25 with the correct header information for the stream that will be sent over HDMI.
7. Write registers 0xBF–CD with the appropriate Audio InfoFrame information.
8. Set the audio packet header layout indicator to 2-channel or multi-channel mode as needed using the sequence described below. Note that Audio InfoFrame byte 1 must also have this same setting.
9. Again write register 0x26 with I^2S selected, this time with Mute disabled (bit [4] = 0).

I²S Input Configuration Register. Software configures the incoming SD format as shown in Table 19.

Table 19. Configuration of I²S Interface (RW)

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x20 [95]	**I²S Input Configuration Register**							
	SCK Sample Edge 0 – Falling (change data on rising edge) 1 – Rising	MCLK Multiplier – the Tx uses these bits to divide the MCLK input to produce CTS values according to the 128* f_s formula. The MCLK-to- f_s ratio is for input f_s, not down-sampled output f_s. 000 – 128 001 – 256 010 – 384 011 – 512 100 – 768 101 – 1024 110 – 1152 111 – 192			WS Polarity – Left when: 0 – WS is Low 1 – WS is High	SD Justify Data is justified: 0 – Left 1 – Right	SD Direction Byte shifted first: 0 – MSB 1 – LSB	WS to SD First Bit Shift? 0 – Yes (per spec) 1 – No

I²S Enable and Mapping. Software typically writes TPI 0x1F multiple times, with a separate FIFO selected each time, to assign SD pins to FIFOs. A single SD pin may be connected to multiple FIFOs. For example, the same SD0 pin could be assigned to FIFO#0, FIFO#1, FIFO#2, and FIFO#3 in order to provide 8 audio output channels. Unused FIFOs can be assigned to disabled SD inputs.

Note that no gaps are allowed when mapping channels to FIFOs – SD pins must be mapped to FIFO#0 and FIFO#1 before mapping a channel to FIFO#2, and so on.

Automatic Down-Sample. This feature provides sample rate conversion of stereo input to the Basic Audio rate that all HDMI sinks are required to accept; the specification allows this level of audio to be sent even before determining the device capabilities from EDID. The logic is only capable of converting a stereo signal, and cannot down-sample more than two channels. The down-sample logic output operates only on FIFO#0.

Table 20. Mapping of I²S Interface (RW)

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1F [00]	**I²S Enable and Mapping Register**[1]							
	SD pin selected by [5:4] 0 – Disable 1 – Enable	Rsvd	Select SD pin to be connected to a FIFO 00 – SD0 01 – SD1 10 – SD2 11 – SD3		Automatic down-sample to Basic Audio mode (FIFO#0 only) 0 – Disable 1 – Enable	Swap Left / Right I²S channels on this channel 0 – No swap 1 – Swap	This FIFO will take its input from the SD pin selected in bits [5:4] 00 – FIFO#0 01 – FIFO#1 10 – FIFO#2 11 – FIFO#3	

Notes

1. Reads of this register return the last value written, so the readback value has meaning only for the channel most recently configured.

Header Layout Setting Sequence

Use TPI 0x26[5] to select the header layout. Once set, this bit setting will remain in effect and does not need to be rewritten on f_s change events.

→ **Exception.** For the SiI9022 and SiI9024 (non "A") transmitters and the SiI9222/9226 transmitter, TPI 0x26[5] is not available. Instead, follow the sequence below:

```
a. Write 0xBC=0x02              // Internal page 2
b. Write 0xBD=0x2F              // Indexed register 2F
c. Read 0xBE                    // Read current value
d. Modify bit[1] = Layout       // Change only the identified bit
e. Write 0xBE                   // Write back modified value
```

The sequence must be repeated any time audio has been muted before it is unmuted, or if the f_s rate has changed, because hardware will overwrite the previously programmed information on either of those events.

Table 21. Audio Packet Header Layout Indicator (R/W)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Internal Register available at 0xBE when: 0xBC=02 0xBD=2F	Rsvd – write as read.						Layout Audio packet header layout indicator 0 – Layout 0 (2-channel) 1 – Layout 1 (up to 8 channels)	Rsvd – write as read.

Audio Word Length

When using the I^2S interface, audio word length must be defined independently for the incoming I^2S stream and outgoing HDMI stream.

Output Word Length. Whether for S/PDIF or I^2S, the HDMI stream always accommodates a 24-bit audio sample word, regardless of whether all bits of the word are used. An indicator is provided in the stream header to identify the actual length of data to be used. For S/PDIF, this information is transferred automatically to HDMI. However, for I^2S, it is necessary to program the length explicitly if it is less than the default value of 24.

Use TPI 0x25[3:0] to select the word length to be indicated to the receiver as shown in Table 22.

Table 22. Stream Header Settings for I^2S (RW)

Note that these registers are available **only** when TPI 0x26[7:6] = 10 to select I^2S input.

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x21 [00]	**I^2S Channel Status Byte 0**							
	cbit7	cbit6	cbit5	cbit4	cbit3	cbit2	cbit1	cbit0
0x22 [00]	**I^2S Channel Status Byte 1: Category Code**							
	cbit15	cbit14	cbit13	cbit12	cbit11	cbit10	cbit9	cbit8
0x23 [00]	**I^2S Channel Status Byte 2: Source, Channel Number**							
	I^2S Channel Number cbit23:20				I^2S Source Number cbit19:16			
0x24 [0F]	**I^2S Channel Status Byte 3: Accuracy, Sampling f_s**							
	Clock Accuracy cbit31:28				Sampling Frequency cbit27:24 0000 – 44.1kHz 1000 – 88.2kHz 1100 – 176.4kHz 0010 – 48kHz 1010 – 96kHz 1110 – 192kHz 0011 – 32kHz 1001 – 768 kHz (HBRA) 0001 – not indicated			
0x25 [0B]	**I^2S Channel Status Byte 4: Original f_s, Sample Length**							
	Original f_s, Channel Status bits 39:36 Refer to IEC60958 specification				Sample Length, Channel Status bits 35:32 Word Length 1011 – 24 bits (default) 1001 – 23 bits 0101 – 22 bits 1101 – 21 bits 1010 – 20 bits 1000 – 19 bits 0100 – 18 bits 1100 – 17 bits 0010 – 16 bits			

Input Word Length. Unlike S/PDIF, the incoming I^2S audio stream has a variable word length. The output word length should be set to this same value or less, but never more.

The I^2S sampling circuit defaults to 24-bit word length. The Input Word Length bits follow the same definition as the output word length bits: they are automatically set whenever the Output Word Length (TPI 0x25[3:0]) is written. To configure the circuit for sample word sizes less then 24 bits, follow the procedure listed below; it is necessary only if the Input and Output word length values are different.

→ **Exception.** This setting procedure is mandatory for the SiI9022 and SiI9024 (non "A") devices.

```
// Select the specific word length
   a) Write 0xBC=0x02                    // Internal page 2
   b) Write 0xBD=0x24                    // Indexed register 24
   c) Read 0xBE                          // Read current value
   d) Modify bits[3:0] = Word length     // Change only the identified bits
   e) Write 0xBE                         // Write back modified value
```

Table 23. Word Length Selection (R/W)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Internal Register available at 0xBE when: 0xBC=02 0xBD=24					Word Length 1011 – 24 bits (default); 1001 – 23 bits; 0101 – 22 bits; 1101 – 21 bits; 1010 – 20 bits 1000 – 19 bits 0100 – 18 bits 1100 – 17 bits 0010 – 16 bits			

HDMI Audio InfoFrame Requirements for I^2S Operation

Audio InfoFrame requirements in the HDMI specification must be handled manually for I^2S. All stream header information must be programmed by the host. The host must also program the Audio InfoFrame information.

HDMI allows for up to eight channels of audio content. Two channels pass through each of the four FIFOs. HDMI does not restrict the source to use any specific subset of the FIFOs. For example, 4-channel content can use many combinations of two FIFOs and two fields in the Audio InfoFrame packets (indicated by each packet's B.X and SP.X bits; see the *HDMI Specification*) limited only by the channel assignment choices in EIA/CEA-861-E Annex K.

The HDMI transmitter logic sets the B and PR bits automatically in each Audio InfoFrame packet, using both the I^2S channel enables and the channel FIFO mapping. Some HDMI receiver chips do not make the arriving B and PR bit information accessible to the sink firmware. Therefore, the only indicator of *used audio channels* is in Data Byte 4 of the Audio InfoFrame packet.

→ **Note: Since the transmitter can be connected to a sink or repeater with SPDIF output, it is sometimes needed to control IEC60958 Vality bit (V bit). It can be done as follows.**

```
1) Write 0xBC=0x01                    // Internal page 1
2) Write 0xBD=0x1D                    // Indexed register 1D
3) Read 0xBE                          // Read current value
4) Modify bit [4] = V_bit value       // Change only the identified bits
5) Write 0xBE                         // Write back modified value
```

Configuring Audio for DSD Format

The Direct Stream Digital (DSD) Audio format, referred to as One-Bit Audio format in the HDMI specification, is supported using the I^2S clock and data inputs, S/PDIF input, and two additional pins for the 7th and 8th channels. Not all transmitters support DSD – for details, refer to the device data sheet.

Setting TPI 0x26[7:6]=11 selects the DSD input format. When selected, the appropriate I^2S configuration register bits become control for the DSD logic. According to the number of channels, register 0x1F needs to be set up the same way as for I^2S input. Note that automatic down sampling of One-Bit Audio is not possible. Therefore, TPI 0x1F[3] needs to be set to zero.

The following is an example of how to set up DSD Audio for 5.1 Channel SACD transfer.

```
a) Write 0x26=0xF0 // DSD, Layout 1, Mute
b) Write 0x1F=0x80
c) Write 0x1F=0x91
d) Write 0x1F=0xA2
```

In addition to these settings, for standard 5.1-channel SACD, the following Audio InfoFrame fields need to be set:

- Coding Type (CT) → 0x00 (Refer to Stream Header)
- Channel Count (CC) → 0x05 (6 Channels)
- Sample Frequency (SF) → 0x02 (44.1kHz).

Other settings are also possible depending on usage case.

As a final step, un-mute the audio inputs.

```
e) Write 0x26=0xE0 // DSD, Layout 1
```

Configuring Audio for HBR Format

High Bit Rate (HBR) Audio is always transferred via I^2S using all 4 data lines (SD0-SD3). The following is an example of how to set up HBR Audio.

```
a) Write 0x26=0x90 // I2S, Layout 0, Mute
b) Write 0x27=0xFC // HBR Audio, 192kHz, 24 bit
c) Write 0x1F=0x80
d) Write 0x1F=0x91
e) Write 0x1F=0xA2
f) Write 0x1F=0xB3
g) Write 0x26=0x80 // I2S, Layout 0, Unmute
```

Note that the Sample Frequency field (SF) of the Audio InfoFrame needs to be set to the correct value (for this example, to 192kHz) as channel status data is not sent across HDMI when HBR Audio is enabled.

→ **Important Note:** For HBR audio, the HDMI specification requires the Layout bit TPI 0x26[5] to be cleared to 0.

→ **Important Note: For the SiI 9136 / 9334 I2S IN Ctrl must be set through the indexed register 0x1D.**

```
// Set I2S IN CTRL
   1) Write 0xBC=0x01                    // Internal page 1
   2) Write 0xBD=0x1D                    // Indexed register 1D
   3) Read 0xBE                          // Read current value
   4) Modify bit[5] = 1            // Change only the identified bits
   5) Write 0xBE                         // Write back modified value
```

Interrupt Service

TPI can be configured to generate an interrupt to the host to notify it of various events. The host can either poll for activity or use an interrupt handler routine. TPI generates only a single interrupt signal (INT) to the host.

Interrupt Enable Register

Enables TPI and transmitter to generate interrupts to the host. Hot plug interrupts to the host will be generated even in D3 (low-power) state. Writing any bit to 1 enables the interrupt source, and also clears any pending interrupts. Note that writing 0 to disable the interrupt does not clear any previously pending interrupt.

Access. This register is accessed as a single byte.

Table 24. TPI Interrupt Enable (R/W)

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x3C [00]	HDCP Authentication Status Change 0 – Disable 1 – Enable	HDCP V* Value ready 0 – Disable 1 – Enable	Security Status Change 0 – Disable 1 – Enable	Audio Error Event 0 – Disable 1 – Enable	CPI Event in place of Rx Sense 0 – Disable 1 – Enable	CTRL Bus Event in place of Hot Plug[1] 0 – Disable 1 – Enable	Receiver Sense Event 0 – Disable 1 – Enable	Hot Plug / Connection (cable plugged/ unplugged) Event 0 – Disable 1 – Enable

Note
1. Applicable to SiI923x Mobile HD Link devices only.

Interrupt Status Register

Shows current status of interrupt events, even if the event has been disabled. This register can be polled for activity if the associated interrupt has been disabled. Write 1 to interrupt bits to clear the 'pending' status. Bits 3 and 2 (bits 3:0 on Mobile HD Link devices) serve only to show the current state and cannot be cleared.

Access. This register is accessed as a single byte.

Table 25. TPI Interrupt Status (R/W)

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x3D [00]	HDCP Authentication status change Event pending 0 – No 1 – Yes	HDCP V* Value ready Event pending 0 – No 1 – Yes	Security Status Change Event pending 0 – No 1 – Yes	Audio Error Event pending 0 – No 1 – Yes	RxSense current state or CPI Event pending state (RO) 0 – No Rx sensed/CPI 1 – Powered Rx attached/ CPI event pending	Hot Plug pin current state or CTRL Bus Transaction Event pending state (RO) 0 – HP Low or no event pending 1 – HP High or CTRL event pending	Receiver Sense Event pending or CTRL Bus Error indicated 0 – No 1 – Yes	Hot Plug / Connection Event pending 0 – No 1 – Yes
0x3E [00]	Reserved						Received 1st byte of KSV 0 – No 1 – Yes	HDMI Link Stable 0 – No 1 – Yes
0x3F [00]	Reserved						Interrupt Control Received 1st Byte of KSV 0 – Disable 1- Enable	Interrupt Control HDMI Link Stable 0 – Disable 1 – Enable

Hot Plug / Connection. The Hot Plug *state* (HTPLG signal from the DVI or HDMI sink) indicates whether a display is attached (the EDID is readable, but the display is not necessarily powered up). The Hot Plug *event* indicates whether the state has changed. For Mobile HD Link devices, this event and state are "virtual" and reflect the combined status of both the remote HTPLG pin at the HDMI connector of the bridge device and the connection state of the CTRL bus.

Receiver Sense. The Receiver Sense *state* (RxSense signal from HDCP) indicates whether a powered-up receiver is sensed (whether the TMDS lines are being pulled externally to 3.3V). The Receiver Sense *event* indicates whether the state has changed. Note that to clear the Receiver Sense event bit on Mobile HD Link devices, the host may need to use the CTRL bus register set, as noted in Appendix B.

CPI Event. Even though the CPI register set is accessed at a completely separate I^2C slave address, CPI event pending status can optionally be reflected in the TPI Interrupt Status register in place of the Receiver Sense status bit. In this way, a single register read is adequate to check all interrupt sources at once. Setting 0x3C[3] = 1 allows 0x3D[3] to indicate a CPI Event Pending status. Note that the event itself must be cleared from the CPI registers (writing 1 to 0x3D[3] has no effect).

To further clarify: Setting 0x3C[3]=1 simply allows the CPI interrupt pending status registers to reflect into 0x3D[3]. The interrupt is caused by enabling its source in the CPI registers, not by setting 0x3C[3]=1 – the interrupt would happen just the same if this bit were 0. It is only a convenient way to be able to see the pending CPI interrupt status from the main TPI interrupt register.

CTRL Transaction Event. The CTRL bus transaction registers are used to control and monitor Private Channel exchanges for Mobile HD Link devices, as described in the *Link Control Bus Programmer's Reference* (SiI-PR-1031). Even though this register set is accessed in a separate address block, CTRL bus transaction event pending status can optionally be reflected in the TPI Interrupt Status register in place of the Hot Plug status bit. In this way, a single register read is adequate to check all interrupt sources at once. Setting 0x3C[2] = 1 allows 0x3D[2] to indicate CTRL bus transaction event pending status. Note that the event itself must be cleared from the CTRL bus registers (writing 1 to 0x3D[2] has no effect).

CTRL Bus Error Event. As noted above, the CTRL bus register set is accessed in a separate address block; that set includes the interrupt status registers associated with CTRL bus errors. CTRL bus error event pending status can optionally be reflected in the TPI Interrupt Status register at 0x3D[1]. Whether this bit represents RxSense events, CTRL bus error events, or both, is determined by a bit setting in the CTRL bus register set.

Audio Error. The Audio Error event indicates that an event related to the incoming S/PDIF audio stream has been detected and handled automatically. The most common event is a change in audio header f_s information. The hardware handles the event without a need for intervention, but the host can use this interrupt to read back the updated status information. No audio events related to I^2S input are reported.

Security Status Change. Any change in the Link Status value (TPI 0x29[5:4]) generates a Security Status Change event so that the host can take appropriate action to re-establish the link.

HDCP V* Value Ready. Once a V* value is selected, this event indicates that the computation has completed and the value is available (TPI 0x31[3] = 1).

> **Note:** This interrupt feature is functional only on the SiI9136/9334 Tx and SiI923x Tx devices.

HDCP Authentication Status Change. An authentication status change event reflects changes in TPI 0x29[7:6], indicating that:

- The previous authentication request (from a write to the Protection Level bit) has completed successfully.
- The extended authentication process failed to complete within ~5s.
- An Ri mismatch has caused authentication to fail.

Refer to the "Extended Link Protection Level" discussion in the HDCP section for details.

Interrupt Operation

The chip provides an interrupt signal INT that is programmable with either active-high (driven) or active-low (open drain) polarity when in SiI9020 Tx Compatible Mode (refer to Appendix A). However, in TPI register mode, this line is pre-set to operate as active low, which allows the external signal to be shared with other active-low interrupt-capable devices.

A number of interrupt functions can be optionally added to INT after startup. If the host enables interrupt sources by setting bits in register 0x3C, one or more events from an enabled source cause a pulse on the INT line. The host will use the signal to recognize and service the interrupt. This sequence is illustrated in Figure 6.

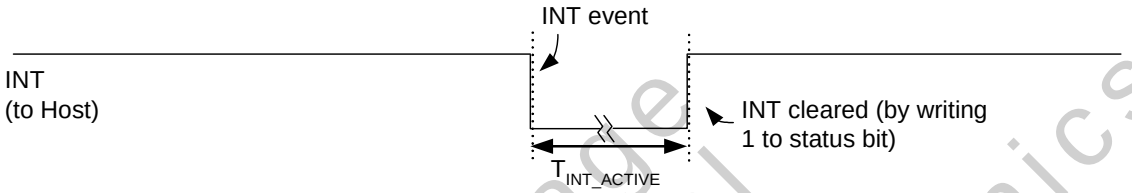


Figure 6. INT Pulse on Event other than HTPLG

When the host clears the interrupt event (by writing 1 to the triggering Interrupt Status Register bit), the INT line will go high, as long as there are no more active events. T_{INT_ACTIVE} duration depends on the response time of the host and firmware.

Before leaving the service routine, the host should poll for additional events that could have occurred after the host completed the initial service.

For SiI9334 and SiI9136: To use the interrupt pin in D2 or D3 power states, it is required to make a software reset (setting and then clearing 0x40[1]) before entering the power down modes.

For SiI 9022A and 9024A: To use the interrupt in D3 power state, it is required to make hardware reset before entering the power down mode and HPD must be low or Cable must not be connected prior to entering D3 Hot or D3 Cold mode for wake-up to be valid.

TPI System Reset And Control

The transmitter subsystem has additional control necessary from the firmware

Table 26. TPI Soft Reset (R/W)

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x40	TPI Soft Reset and Control							
[00]	Alternative TMDS Clock Stable 0 = Unstable 1 = Stable	TMDS Clock Stable 0 = Unstable 1 = Stable	Reserved			Deep Color GCP Packet 0 = Disable 1 = Enable	Reserved	Software Reset 0 = Disable 1 = Enable

Software Reset – Reset all sections, including the audio FIFO, except registers that are user configurable. Caution: CEC operation is not guaranteed after a Software Reset because the software rewset clears only write pointer while keeping the read pointer. Therefore, there will be mismatches in write/read pointers, the amount of mismatch will depend on when software reset is issued.

Deep Color GCP Packet – Enable the General Control Packet transmission for Deep Color operation.

TMDS Clock Stable – IDCK to TMDS clock is stable and the Transmitter can send reliable data on the TMDS link. A change to the IDCK sets this bit LOW. Along with a status bit for TMDS Clock Stable there is a TPI Interrupt (TPI 0x3E[0]) for TMDS Clock Stable and a corresponding Interrupt Enable (TPI 0x3F[0]).

Alternative TMDS Clock Stable – Similar to TMDS Clock Stable, but uses alternative method for clock checking. There is no interrupt associated with this bit change.

Power State Control and Hot Plug Management

The transmitter subsystem requires control of power state after a hardware reset, following by ongoing management of plug events to determine when the subsystem should be put back into a low-power mode. Note that the SiI9136/9334 Tx defaults to device power state D0 after reset, while all other devices come up in D2 state.

Transmitter Power State Register

TPI supports ACPI power states D0, D2, and D3. Transition from D0 to any other state requires only a write to the Power_state[1:0] bits.

When the host writes 0x1E[1:0] after reset, the subsystem operates as follows.

→ **03 (D3):**

- An RSEN or Hot Plug interrupt event bit in TPI 0x3D[1:0] must be set **prior** to entry to D3 if a wakeup interrupt is to be enabled.

  → **Exception:** For the SiI9136/9334 Tx only, if a wakeup interrupt will be enabled, it is **also** necessary to first reset internal logic before entering D3 state. Otherwise, INT will be asserted immediately if HPD is high on entry to D3.

```
1. Set   TPI 0x40[0] = 1          // Assert software reset
2. Clear TPI 0x40[0] = 0          // Clear software reset
```

  → **Exception:** For the SiI9022A/9024A Tx:

  1. A full hardware reset is required to wake the system up from D3 Hot or D3 Cold mode.
  2. HPD must be low or Cable must not be connected prior to entering D3 Cold but is optional per usage model on D3 Hot mode for wake-up to be valid.

  For D3 Cold:

  1. Disconnect Cable
  2. Clear any pending interrupts via TPI 0x3D
  3. Reset SiI9022A/9024A Tx via HW
  4. Write device address 0x72, register offset 0xC7 = 0x00 to enter TPI mode
  5. Set INT# source to Hotplug via TPI 0x3C[0] = 1b
  6. Clear any pending interrupts via TPI 0x3D
  7. Enter D3 Cold mode via TPI 0x1E[1:0] = 11b

  For D3 Hot

  1. Cable can be disconnected or left connected.
  2. Set INT# source to either RSEN or HPD
  3. Clear any pending interrupts via TPI 0x3D
  4. Enable D3 Hot mode via register 0x1E[1:0] = 11b
  5. Go back to D3 Hot or enter D3 Cold if cable is unconnected or wake up if cable is connected based on cable setting before entering D3 Hot.

RSEN	Hot Plug
D3 Hot	D3 Hot
	D3 Cold

- The transmitter is brought to its lowest-power state.
- The host can no longer read any registers.
- If a wakeup interrupt bit was set before entering D3 state, a plug-in event will cause INT to be asserted and stay there (it cannot be cleared since register access is disabled).
- The host must assert RESET# to the chip to leave D3 state. Reset is **required** for proper return from D3.

→ 02 (D2):

- The transmitter is brought to a low-power state, but not quite as low as D3 state.
- Host can read registers.
- A plug-in event will cause INT to be asserted if enabled.

  → **Exception:** For the SiI9136/9334 Tx only it is **also** necessary to first reset internal logic before entering D2 state.

```
1. Set   TPI 0x40[0] = 1            // Assert software reset
2. Clear TPI 0x40[0] = 0            // Clear software reset
```

- The host must then program the system back to D0 state in order to restore full operation, and must clear the host plug interrupt in TPI 0x3D to allow INT to be deasserted.

→ 00 (D0):

- The transmitter is brought to full operation. TMDS output will be enabled (disabled for SiI9136/9334) according to TPI 0x1A settings.
- Writing D1 has the same effect as writing D0.

D0→D2 Transition

- The D2 state powers down the transmitter (TMDS output is disabled), but leaves the registers operational. All register settings remain unchanged.

D2→D0 Transition

- All register settings remain unchanged except for 0x1A, which disables TMDS output.

Hot vs Cold Wakeup Modes

The SiI9022A/SiI9024A and SiI9136/9334 devices offer a deeper power saving mode than other devices. Enabling best power savings requires disabling one of the wakeup features.

- Hot Plug Detect (HDP from the HDMI connector) is always available as a wakeup source in D2 and D3 states.
- Receiver Sense (RSEN, monitoring the TMDS lines for active pullups at the receiver side) is only available as a wakeup source when TPI 0x1E[2]=0.

SiI9022A/SiI9024A Tx. TPI 0x1E[2] is effective only for D3 state. It defaults to a setting of 0, for which the D3 description above is valid, except that the power consumption is not yet at its absolute lowest. This is known as D3hot mode, in which HPD and RSEN wakeup events can be monitored.

To enter the lowest power mode, the host must write TPI 0x1E[2]=1 to select D3cold mode *prior* to writing TPI 0x1E[1:0]=11. That is, the mode must already be set before selecting D3 mode. In D3cold state, the chip will go to its absolute lowest power state. However, it will ignore HPD and RSEN wakeup events regardless of other programming.

SiI9136/9334 Tx. TPI 0x1E[2] is effective for both D3 and D2 states. It defaults to a setting of 0, for which the D3 description above is valid, except that the power consumption is not yet at its absolute lowest. This is known as D3hot mode, in which HPD and RSEN wakeup events can be monitored.

Other Devices. Other devices do not implement this bit, and go to a D3hot state within D3 state – that is, they are always able to generate an interrupt within D3 state (if the interrupt was enabled prior to entry to D3 state).

Access. This register is accessed as a single byte.

Table 27. TPI Device Power State Control Data (R/W)

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1E [02]	Rsvd					Wakeup state[1] 0 – Hot 1 – Cold	Tx Power_ state[1]	Tx Power_ state[0]

Hot Plug Management

To properly handle plug and unplug events, the host must implement the Hot Plug Service Loop.

Hot Plug Service Loop

After the host releases Reset to the HDMI transmitter subsystem and initializes the part, the host program typically enters a Hot Plug Service Loop. The transmitter subsystem logic monitors for Hot Plug activity, but will not attempt detection of the attached device until the host program takes specific action.

During this time, the following registers are of importance.

- Request/Grant register 0x1A. Any time the host wants to read EDID, it must follow the correct procedure for requesting access to the DDC bus.
- Interrupt Enable 0x3C. If desired, interrupt-driven operation can be enabled through TPI 0x3C. Otherwise polling is used. The bits in 0x3C serve only to enable corresponding active interrupt event bits in 0x3D to cause the INT line to go low.
- Interrupt Status 0x3D. Whether polling or interrupt driven mode is used, the host uses TPI 0x3D to monitor and service all hot plug activity.

The host can poll the Interrupt Status register to watch for EDID availability (bit 2 = 1) and monitor powered-on status (bit 3 = 1), or can enable interrupts for hot plug events.

Suggested Service Flow. When the host either receives an interrupt or polls TPI 0x3D and detects Hot Plug activity with TPI 0x3D[0] = 1, it should follow this procedure.

1. Clear the service event. Write TPI 0x3D[1:0] = 11 to clear the event.
2. Read and record the active pin states. TPI 0x3D[3:2] provide active state information for the HPD and RSEN signal levels.
3. Determine the event that occurred.
   - If the prior state was "plugged-in", an Unplug event has occurred. An interrupt is registered **immediately** in TPI 0x3D[1:0] for an Unplug event. TPI 0x3D[3:2] = 00 confirms an Unplug event; any other state indicates instability in the connection (which should be monitored until it becomes stable before proceeding).
   - If TPI 0x3D[2] = 1, a Plug event has occurred and has likely stabilized. Interrupts due to Plug events are **delayed** until after the HPD signal has stabilized at a High level for ~500ms. Host software can choose to provide additional de-bouncing if desired (See Hot Plug Delay De-bounce).
4. Take action as needed.
   - For a confirmed Plug event, the host should use the Request / Grant protocol to take control of the DDC bus and read EDID as described in the Detailed Sequences section.
   - For an Unplug event, the host should stop sending all video. This step also ensures that no secure video content is being sent.

Operating Sequences

Some of the major events involved in setting up and running the chip are illustrated below.

Reset. The host is required to reset the transmitter subsystem at power-up time. The reset pulse width T_{RST} should meet the minimum requirement of each device. Please refer to the respective Transmitter Data Sheet of the device used to determine the minimum value.**DDC Access by HDCP Subsystem.** When the host selects Operational (D0) state, the chip reserves the DDC bus for immediate host use. As always, the host must use the request/grant mechanism to get the bus. However, only after it has finished and releases the request will the HDCP subsystem look for an HDCP-capable sink on the DDC bus.

In all future uses of the bus, the host must rely on the Request/Grant register bits to use the DDC bus, preventing conflicts with the HDCP logic.

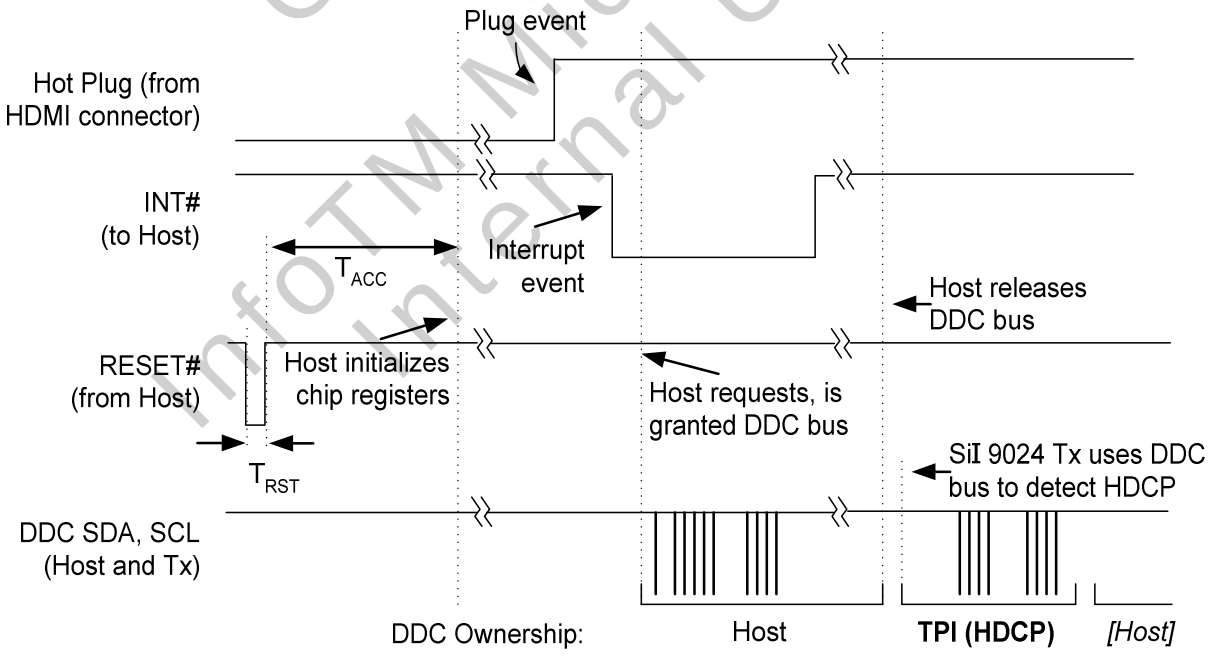


Figure 7. Hot Plug Control Output Timing

Parameter	Description	min	max	unit
T_{RST}	Reset pulse width	50		us
T_{ACC}	Time from reset until host can access chip registers	—	1	ms

Hot Unplug and Plug-in. When the sink device is unplugged, or if the sink device momentarily toggles its HTPLG line low, the hardware immediately returns a Link Lost message when queried by way of TPI. If the interrupt is enabled, the INT line is also asserted until the host clears the interrupt.

The host should check register 0x3D[2] to determine whether a hot plug or hot unplug event is being signaled. If hot plug, the host should continue checking for a minimum of T_{RST_DLY} before recognizing the attachment state, to ensure that the HDMI plug attachment is stable.

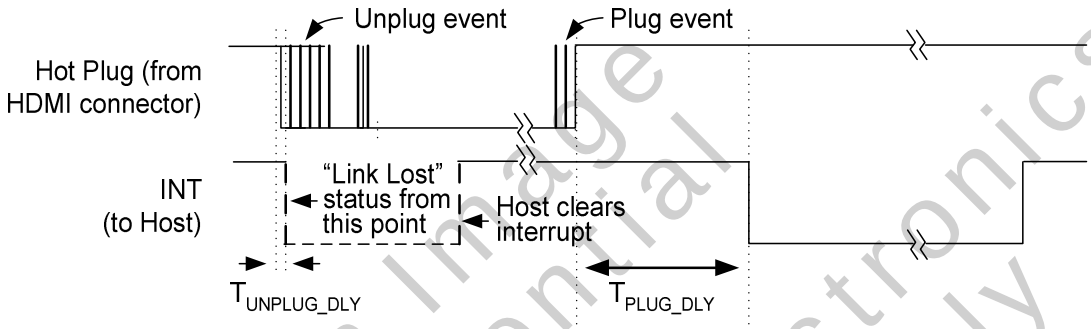


Figure 8. Hot Plug Control Output Timing

Parameter	Description	min	typ	max	unit
T_{PLUG_DLY}	Delay from Hot Plug (HPD) HIGH and stable to INT active (programmable, see Hot Plug Delay De-bounce)	400	480	600	ms
T_{UNPLUG_DLY}	Delay from Hot Plug (HPD) LOW to INT active (not programmable)	—	—	1	ms

Hot Plug Delay De-bounce:

The hot plug delay debounce is programmable in steps of 3.4ms. The logic needs to be manually configured as follows:

```
1. Write 0xBC=0x01          // Internal page 1
2. Write 0xBD=0x7C          // Indexed register 0x7C
3. Write 0xBE=0x13          // Program a delay of approximately 64ms
```

HDCP Implementation

HDCP link security logic is implemented in certain transmitters; unique keys are embedded in each chip as part of the solution. The security scheme is fully automatic and is handled completely by hardware.

Control for HDCP

The host uses standard data structure elements to select the correct level of high definition content protection.

Table 28. Mapping of HDCP Data to TPI Register Bits

Name	Read/ Write	How to Derive from TPI Registers

`ProtLevel`
`Min (0)`
`Max (1)`
	W	The host writes this value to request that link security (HDCP) be enabled (1) or disabled (0).

`ProtType`
`None (0)`
`HDCP (1)`
	R	The host reads this value to determine whether HDCP is available on the attached monitor. The transmitter logic automatically detects whether the sink is HDCP-capable after a hot-plug event. The host must have requested and released the DDC bus at least once to trigger the automatic detection.

`Flags`
`Status Normal (0x00)`
`Link Lost (0x01)`
`Renegotiation Required (0x02)`
	R	The host polls this value, or can be interrupted when this value changes.
		Status Normal: The data link is operating according to the requested Protection Level.
		Link Lost: The physical link has been interrupted (through cable detachment or error).
		Renegotiation Required: During HDCP operation, an Ri mismatch has occurred requiring the host to re-request security.

`ConnectorType`
`DVI (0)`
`HDMI (1)`
	R	The host reads this value to determine whether the attached sink device is DVI or HDMI. It reflects the value written to TPI 0x1A[0].

`ProtectionLevel (Local/Extended)`
`No Link Protection (0)`
`Link Secure (1)`
	R	The host polls this value, or can be interrupted when the value changes.
		Local Link: The link from the transmitter to the attached sink, whether display or repeater.
		Extended Link: The link downstream from the attached repeater. If no repeater is attached, this value will always be 0.

`HDCPFlags` `HDCPRepeater (0x01)`	R	The host reads this value to determine whether the device is an HDCP repeater.
`BKey` `Bksv from attached device.`	R	The host requests `BKey` to determine whether the HDCP keys are valid.

HDCP Operation

Once a connection is made, video is being transmitted, and link video is stable, the host can request link security through TPI 0x2A[0]. All subsequent authentication is performed automatically, and the resulting security level is reflected in TPI 0x29[7:6]. Typically the process takes under 1s.

Once the link is authenticated, periodic link integrity checks take place every 128 frames. The time interval between checks is therefore roughly 2s, depending on whether 60 or 50Hz video is being supplied. Note that some resolutions run at lower frame rates (such as 24Hz) will create a corresponding slow-down in the frequency of the periodic checking. It is possible to enable intermediate Ri reading 0x2A[3] to satisfy the 2 s requirement for Ri checking.

Because any lengthy host use of the bus could conflict with HDCP link checks that occurs every 2 s, it is strongly recommended that the host clear its link security request (TPI 0x2A) whenever it wants to access the DDC bus.

HDCP Data Structure

The registers below reflect the information needed for the security interface. Use of these bits is detailed on the previous page. Additional information is provided below.

Link Status. These bits operate as follows; a status change can cause an interrupt if enabled.

> Normal: The link is operating correctly; valid whether HDCP is running or not.
>
> Link Lost: A hot plug or other event has caused the link to go down. A reset may be necessary to restore operation, if the logic is unable to return the connected link to Normal condition.
>
> Renegotiation required: The link is still active, but some event (usually Ri mismatch) has caused HDCP to fail. The host must disable and then re-enabled the security request (TPI 0x2A[0]).
>
> Link Encryption Suspended: The link is still active, but encryption has been turned off by clearing 0x2A[0]. This condition will return to Normal once 0x2A[0] is set to 1 again.

Note that the HDCP subsystem continues to keep the link authenticated (doing Ri checking) even after 0x2A[0] is switched from 1 to 0, so that subsequent security requests can return a "secure" status more quickly.

Extended Link Protection Level. TPI 0x29[7] indicates that the repeater authentication is complete. The bit should be ignored if the HDCP Repeater bit is not = 1.

> → **Link Integrity Mode.** If a downstream HDCP repeater is discovered, Link Integrity Mode bit TPI 0x1A[6] should be set to 1 (Dynamic). This setting forces the logic to re-authenticate any time the incoming clock resolution changes. This same setting will work even when the downstream sink is not a repeater; however, authentication may take slightly longer.

Repeater authentication takes place automatically after local link protection is established. The possible outcomes are:

- Success. Within 5s, TPI 0x3D[7] → 1 to indicate the change in security status. Firmware then checks that TPI 0x29[7]=1, indicating that the extended link is now secure.
- Failure: After ~5s, if the extended link cannot be authenticated (typically due to lack of Ready status by the downstream HDCP repeater), TPI 0x3D[7] → 1 to indicate that authentication could not take place. TPI 0x29[7] remains at 0.

Using this mechanism, firmware can avoid implementing a timer – the logic design guarantees that TPI 0x3D[7] will be triggered as soon as the outcome is known.

> → **Important Note:** AV Mute must not be set before requesting authentication. If it is set, there will be no indication in TPI 0x3D[7] of the status outcome.

Protection Type. This bit indicates whether the automatic logic has detected an attached HDCP-capable device. The TPI subsystem will not attempt to detect an HDCP receiver until the host has requested and then released the DDC bus once after hot plug, and then turned on TMDS output to send valid clocks. Therefore, even if the host does not read the EDID immediately, it should still request and then release the DDC bus to trigger detection.

Access. All registers can be read either individually or in a burst.

The correct sequence for enabling or disabling HDCP is:

- Poll 0x29[1] until it indicates that HDCP is available; the Bksv values are only valid when 0x29[1] = 1.
- Write 0x2A[0] with the desired setting.
- Poll 0x2A[0] until it matches the setting just made.
- Poll 0x29[7:6] until they indicate the desired security level.

Note that TPI 0x29 may not be updated immediately after a cable connect event, due to the delay (max 1s) introduced by the automatic de-bounce logic. If desired, Interrupt Status register TPI 0x3D bits 2 and 0 can be read to verify the connection before reading TPI 0x29.

Table 29. TPI Security Registers

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x29	QueryData (RO)							
	Extended Link Protection Level (across repeaters) 0 – No link protection 1 – Link secure	Local Link Protection Level 0 – No link protection 1 – Link secure	Link Status 00 – Normal 01 – Link Lost 10 – Renegotiation required 11 – Link Encryption Suspended		HDCP Repeater 0 – No 1 – Yes	Connector Type Bit 2 + bit 0 work together: 0+0 – DVI 1+0 – HDMI 0+1 – Rsvd 1+1 – Future	Protection Type 0 – None 1 – HDCP	Connector Type Extension See bit 2
0x2A [00]	ControlData (RW)							
	Rsvd		encryption disable 0 = encryption enabled if authentication succeded 1 = no HDCP encryption (even after authentication)	KSV Forward 0 = disable 1 = enable	Ri Intermediate Check 0 = disable 1 = enable	Ri Read Twice 0 = disable 1 = enable	Ri Read Format: 0 = normal 1 = short	Protection Level 0 – Min (no protection needed) 1 – Max (HDCP required)
0x2B	BKSV_1(RO)							
0x2C	BKSV_2(RO)							
0x2D	BKSV_3(RO)							
0x2E	BKSV_4(RO)							
0x2F	BKSV_5(RO)							
0xBB [76]	OptionControl (RW)							
	Internal Use Write as 0	Internal Use Write as 1	Internal Use Write as 1	Internal Use Write as 1	Ri Check Skip 0 – Enforce Ri check every 128 frames 1 – Allow up to two Ri checks to be skipped	Internal Use Write as 1	Internal Use Write as 1	Internal Use Write as 0

For SiI 9022A/9024A only: Always enable 0xBC = 0x01; 0xBD = 0x0A; 0xBE = 0x09 for HDCP to work in embedded mode with a Device_Count = 0 condition before enabling video output or polling for HDCP availability.

Important Notes

The automatic HDCP module expects firmware to follow a certain logical order in order to correctly sequence the HDCP events. Important considerations for this sequencing are noted below.

- **Initial Request/Grant Requirement.** On a hot plug event, host firmware requests and is granted the DDC bus for reading EDID. The bus must be requested, granted, and released at least once after any hot plug event (through TPI 0x1A). This action releases the bus from an initial hold state, allowing internal logic to access it as needed.
- **Triggering the Bksv/Bcaps Read.** After the host has read the EDID and determined an acceptable resolution, it starts sending video to the transmitter input. Once this video is stable, the host enables the TMDS output from the transmitter (again through TPI 0x1A). Turning on TMDS output triggers the logic to attempt to discover downstream HDCP devices, which require a TMDS clock before they become accessible. Only then can the Tx read Bcaps and Bksv.
- **Causes of "Renegotiation Required".** Once the host requests link security through 0x2A[0]=1, the DDC bus is tied up by the 1st, 2nd, and 3rd parts of the authentication process described in the HDCP specification. After the 1st part is complete, TPI 0x29[6]=1. After the 2nd part is complete, TPI 0x29[7]=1. The 3rd part is a recurring event, repeating every 128 frames. Interruption of any of these phases will result in TPI 0x29[5:4]=11, indicating Renegotiation Required. This would likely happen if an intentional external hack were taking place on the DDC bus to circumvent HDCP.
- **Causes of "Link Encryption Suspended".** Even when HDCP encryption is turned off through TPI 0x2A[0]=0, the logic will attempt to keep the link authenticated through periodic Ri checks. If no other DDC activity has interfered with an Ri check event, turning HDCP encryption back on will take effect immediately and the link will still be considered secure (no new authentication needed). But if some device takes over the DDC bus and prevents a periodic Ri check, the result is TPI 0x29[6:5]=11, Link Encryption Suspended.
- **ksv List Acquisition in Source Applications.** When the Tx is used in an HDMI Source system, the host uses a normal request/grant procedure to obtain control of the DDC bus, and then reads the downstream ksv lists for comparison against keys in the SRM. HDCP encryption and link integrity checking can be left enabled; a bus grant will arrive within 2s of the request, and the host can then retrieve and compare the ksv list.
- **ksv List Acquisition in Repeater Applications.** When the Tx is used in an HDMI Repeater system, the HDMI CTS restricts the amount of time allowed for loading the downstream ksv list into the upstream Rx FIFO and setting the Ready bit. TPI development firmware supplied by Silicon Image includes special "shortcut" routines for quickly and safely forcing a grant of the DDC bus, allowing the ksv list to be quickly acquired and loaded to the upstream Rx FIFO. Refer to the supplied firmware for details on this and other Repeater-related topics.

Ri Read (Available only on the SiI9136/9334.)

Postponing the Ri Check. There are times when the host would want to use the DDC bus while still keeping the link authenticated, but may not be able to return the bus in time for the next Ri check to take place. TPI 0xBB[3] is provided to allow extra time in this case. When set to 1, if the DDC bus is granted to the host, up to two Ri checks (coming at the usual 128 frame intervals) can be missed without triggering a Link Encryption Suspended or Renegotiation Required event. This bit can be set to 1 once, at initialization time, if desired.

Ri Short Reads. Enabled through TPI 0x2A[1] = 1, short read are done in order to minimize the number of bits that must be transferred for the link integrity check, a second short read format is supported. This access has an implicit offset address equal to 0x08, the starting location for Ri'. The short read format may be uniquely differentiated from combined reads by tracking STOP conditions (P) on the bus. Short reads are supported with auto-incrementing addresses and enabled by TPI Ri Read Format Register.

The following describe the formats of the Ri reads:

- A normal Ri read over the I2C bus is of the following format:
  <S> <Slave Address (7)> <W> <A> <Slave Offset (8)> <A>
  <S> <Slave Address (7)> <R> <A> <Read Data (8)> <A> <Read Data (8)> <Â> <P>

- A short Ri read over the I2C bus is of the following format:
  <S> <Slave Address (7)> <R> <A> <Read Data (8)> <A> <Read Data (8)> <Â> <P>

Ri Reading Twice: Enable Ri checking at the time of Ri counter = 127. Without setting this bit, Ri check is performed at only counter = 0. Recommend to set this bit.

Ri Intermediate Check: Enable the intermediate check to also cause the Ri values to be checked at Ri counter 64.

Auxiliary HDCP Registers

TPI supports HDCP repeater authentication and revocation through the simple interface described below.

HDCP Info Register

Identifies the support for HDCP revision 1.2. If this byte reads 00, HDCP is not supported in this device. However, if the byte is not zero, HDCP may still not be supported. Software must read and verify Aksv as described on the next page (TPI 0x36-3A) to verify HDCP capability.

Access. This register is accessed as a single byte.

Table 30. TPI HDCP Revision Data (RO)

Offset	Bits	Bit Field Description	Return value
0x30	[3:0]	HDCP Minor revision	0x02
	[7:4]	HDCP Major revision	0x01

V* Value Select Register

"V* value" is the Silicon Image designation for the KSV values it has hashed together with the transmitter M0 value. The host reads the V* value and compares it with its own calculated value to verify a match.

Write: Allows the host to select V*0 to V*4 for readback at offsets 0x32–35.

Read: The microcontroller needs some time to load the selected V* values for reading. After the host writes this register to select the set of V* values to be read, it must poll the 'ready' bit until it reads = 1 indicating that the V* values are ready for reading.

Authentication State. This value returns the status of an internal state machine. It should **not** be used by the host for normal activities, as its timings depend on the system configuration. However, it can be convenient for use in HDCP debugging in the case of repeater authentication, where it will stay in the '11' state until all downstream devices have reported back as "ready".

Downstream HDCP Device Count. The transmitter supports a maximum of 16 downstream devices. This bit indicates whether this limit has been exceeded. It is only valid when the repeater authentication process has completed.

Access. This register is accessed as a single byte.

Table 31. TPI KSV and V* Value Data (R/W)

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x31 [00]	Authentication State (RO) 00 – Auth. required 01 – Re-auth. required 10 – Authenticated 11 – Repeater auth. required		Rsvd for internal use	Downstream HDCP Device Count (RO) 0 – Within Tx limit 1 – Exceeds Tx limit	Selected V* Values Ready? (RO) 0 – No 1 – Yes	V* Value Select 000 – H0 001 – H1 010 – H2 011 – H3 100 – H4 101 – Rsvd 11x – Rsvd		

V* Value Readback Registers

The host reads back the 32-bit value for the selected V* value from these registers.

Access. Registers 0x32–0x35 must be accessed as a complete group using a burst read.

Table 32. TPI V* Value Readback Data (RO)

Offset	Bits	Bit Field Description
0x32	[7:0]	V* Hx bits [7:0]
0x33	[7:0]	V* Hx bits [15:8]
0x34	[7:0]	V* Hx bits [23:16]
0x35	[7:0]	V* Hx bits [31:24]

Aksv Value Readback Registers

The host reads back the 40-bit value for the transmitter Aksv from these registers. It must check the Aksv for 20 1s and 20 0s to verify that HDCP capability is available. A 9022A Tx will typically return the values 0x09, 0x00, 0x02, 0x02, 0x0A from these registers, indicating that it is not HDCP-capable.

Access. Registers 0x36–0x3A must be accessed as a complete group using a burst read.

Table 33. TPI Aksv Readback Data (RO)

Offset	Bits	Bit Field Description
0x36	[7:0]	AKSV_1
0x37	[7:0]	AKSV_2
0x38	[7:0]	AKSV_3
0x39	[7:0]	AKSV_4
0x3A	[7:0]	AKSV_5

KSV List Forward (Available only on the SiI9136/9334.)

When KSV forwarding feature is disabled (0x2A[4] is 0) and a repeater is connected to the HDMI output, downstream KSV list is read first by hardware during 2nd authentication part of HDCP. Then firmware needs reading it second time to do KSV revocation (source case) or forward to upstream (repeater case). The reading usually occurs during HDCP part 3 when Ri check periodically occurs. Such reading may take significant time and violate 500 ms requirement for KSV list propagation (repeater case). KSV forwarding feature allows avoiding such problems.
Set 0x2A[4] to enable it. When enabled, hardware reads up to 16 KSV bytes into KSV FIFO. Firmware gets 0x3E[1] interrupt when the FIFO is not empty. The number of available bytes is indicated in 0x41[0…4]. The counter is decremented when a FIFO byte is read from 0x42. It is possible reading from this register in burst mode. If the FIFO is not full and there is data to read from the downstream device, hardware logic continues reading. Once last byte of the KSV list is read, 0x41[7] is set.
Note. If downstream device is a repeater with zero KSV list, no 0x3E[1] interrupt occurs.

Table 34. TPI KSV Forward (RO)

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x41	Last Byte of KSV FIFO received 0 – No 1 – Yes	Reserved		Number of bytes in KSV FIFO				
0x42	KSV FIFO Data							

Bcaps and Bstatus Readback Registers (Available only on the SiI9136/9334.)

Register 0x44 shows shadow downstream BCAPS registers read by hardware during HDCP part 1 and 2.

Table 35. TPI BCAPS (RO)

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x44	HDMI Reserved	Repeater Capability	KSV FIFO Ready	FAST	Reserved		1.1 Features	Fast re-authentication

Bstatus Readback Registers (Available only on the SiI9136/9334.)

In addition to assembling the KSV list, an HDCP Repeater propagates topology information upward through the connection tree to the HDCP Transmitter. An HDCP Repeater reports the topology status variables DEVICE_COUNT and DEPTH. If the DEVICE COUNT is exceeded the Repeater asserts the MAX_DEVS_EXCEEDED status bit. If the computed DEPTH is exceeded the Repeater asserts the MAX_CASCADE_EXCEEDED status bit.

Table 36. TPI BSTATUS (RO)

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x45	MAX DEVS EXCEEDED 0 – No 1 – Yes	Device Count						
0x46	Reserved			HDMI Mode 0 – DVI 1 – HDMI	MAX CASCADE EXCEEDED 0 – No 1 – Yes	Depth		

Appendix A – SiI9020 Tx Compatible Mode

The SiI9022/9024/9022A/9024A Tx devices implement an SiI9020 Tx Compatible Mode, in which the device defaults to register mapping that is nearly identical to the SiI9020 Tx.

Note: When the chip is left in Compatible mode, the TPI register set is **not** accessible.

SiI9020-9022-9022A Transmitter Mode Differences

The current document describes only the Transmitter Programming Interface (TPI) programming model. For new designs, use of the SiI9020 transmitter backwards-compatible register set is discouraged, since TPI is much more efficient and automated. Moreover, the HDCP functionality of the SiI9024/9024A transmitter can be accessed only through the TPI register set (since the SiI9020 transmitter did not offer HDCP).

The chip defaults to SiI9020 transmitter register-compatible mode to allow operation with firmware in existing designs. The following document is required only if the SiI9020 transmitter backwards-compatible programming mode is used.

- SiI-PR-0020: *SiI9020 HDMI PanelLink Transmitter Programmer's Reference*

In addition, some register programming changes are required as described below.

PLL Settings

Due to the newly designed PLL used in the SiI9022/9022A transmitter, a small amount of additional register programming is required to set the PLL according to the input bus clocking. Table A - 1 lists the settings.

TCLKSEL refers to existing bits in the SiI9020 transmitter registers, and is selected as before. ACLKCNT, HLFCLKEN, and CLKMULTCTL must then be set according to both TCLKSEL and the input pixel clock range being used.

Note that when using the TPI mode of operation, the logic sets PLL registers automatically according to the pixel frequency programmed, so the registers shown below are not used.

Table A - 1. PLL Programming Registers – SiI9020 Mode Only (R/W)

Input Clock Multiplier	TCLKSEL 0x82[6:5]	Input Pixel Clock (MHz)	ACLKCNT 0x84[5:4]	HLFCLKEN 0x84[1]	CLKMULTCTL 0x83[5:4]	Resulting PLL Clock (MHz)
0.5x	00	< 36	00	1	01	125–166
		36 – 78	00	0	00	91–178
		78 – 139	01	0	00	98–178
		> 139	10	0	00	115–140
1x	01	< 36	00	0	01	125–166
		36 – 71	01	0	01	91–162
		71 – 104	10	0	01	118–158
		> 104	11	0	01	104–168
2x	10	< 36	01	0	10	125–166
		>36 – 53	10	0	10	122–162
		> 53	11	0	10	107–156
4x	11	always	11	0	11	107–161

Note: These are Device 0x72 Registers.

Table A - 2. summarizes the SiI9022/9022A transmitter PLL-related register changes to the original SiI9020 transmitter register set.

Table A - 2. SiI9020 Tansmitter Mode Difference – PLL Setup (R/W)

Legacy Mode Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x82 [00]	SiI9020 Tx Compatibility PLL Programming Register 1							
	Rsvd	TCLKSEL Refer to Table A - 1		Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
0x83 [00]	SiI9020 Tx Compatibility PLL Programming Register 2							
	Rsvd	Rsvd	CLKMULTCTL Refer to Table A - 1		Rsvd	Rsvd	Rsvd	Rsvd
0x84 [00]	SiI9020 Tx Compatibility PLL Programming Register 3							
	Rsvd	Rsvd	ACLKCNT Refer to Table A - 1		Rsvd	Rsvd	HLFCLKEN Refer to Table A - 1	Rsvd

Notes

1. These are Device 0x72 Registers, and should be changed using a **read-modify-write** sequence **only**.
2. Writing TCLKSEL in 0x82 must be done **before** writing 0x83 or 0x84.

DDC Bus Request/Grant

The SiI9020 transmitter logic included a bus mastering I^2C interface that required preprogramming for background transfer of EDID information to and from its internal buffers. However, this mechanism limited the speed of transfers to well under 100kHz and imposed unnecessary overhead on the transaction.

Therefore, the bus mastering logic was improved for the SiI9022/9022A transmitter to use a direct access mechanism. The host device must simply request bus access and then perform data transfers directly with the end device, with the SiI9022/9022A transmitter logic acting as a "pass-through" buffer. The bus can run up to 400kHz depending on the capabilities of the host and slave devices (but should not exceed the 100kHz HDMI limit). I^2C clock stretching by slave devices is fully supported (by passing the clock stretch back to the master as required).

To use the new direct access mode of DDC operation: The host device uses the DDC bus Request control and Grant status bits as follows.

1. Before performing a DDC bus access, write 0x72:0xC7 = 0x87 to request the bus and switch to the output DDC bus instead of the internal registers.
2. Execute all DDC transfers directly. No internal registers are accessible at this time, except for writes to 0x72:0xC7.
3. When finished, write 0x72:0xC7 = 0x80 to clear the request and switch back to internal registers.

Note that no ACK will be returned to this write. Writing or reading any device 0x72 register will disconnect local I^2C from the external DDC bus, but it is important to perform this specific 0x72:0xC7 write to remove the bus request.

Video Black Mode

The SiI9022/9022A transmitter provides a means of driving out all-black video output as long as it is receiving valid clock and sync inputs. 0x72:0xC7[5] controls this feature.

Table A - 3. summarizes the SiI9022/9022A transmitter register changes to the original SiI9020 transmitter register set.

Table A - 3. SiI9020 Transmitter Mode Difference – Request/Grant/Black Mode (R/W)

Legacy Mode Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xC7 [80]	SiI9020 Tx Compatibility Register							
	TPI Register Set 1 – Disable (9020 mode) 0 – Enable (9022/9024 TPI mode)	Rsvd	Video Black Mode 0 – Normal 1 – Force video to black	Rsvd	Rsvd	I^2C Switch – Local I^2C accesses: 0 – Internal registers 1 – DDC	DDC Grant (RO) 0 – Tx owns DDC bus 1 – Host is granted DDC bus access	DDC Request 0 – Bus not needed 1 – Host requests use of DDC bus

Note: This is a Device 0x72 register.

Power-Down Register

The SiI9022/9022A transmitter HDMI core exhibits reduced power consumption over the SiI9020 transmitter. The new circuitry that is implemented changes how the chip behaves in low power modes, in that clearing PDOSC# or PDTOT# disables further local I^2C bus access.

Therefore, after PDOSC# or PDTOT# are set to 0, hardware reset must be applied before attempting to use the local I^2C bus for register or DDC bus access.

Table A - 4. Power-Down Register for SiI9020 Transmitter Register-Compatible Mode (R/W)

Legacy Mode Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x3D [17]	SiI9022 Tx Power Down Register							
	Rsvd	Rsvd	Rsvd	Factory Test bit Must be 1 for normal operation	Factory Test bit Must be 0 for normal operation	PDIDCK# 0 – Gate off IDCK signal to disable video clock based logic 1 – Normal operation	PDOSC# 0 – Disable internal oscillator clock to digital core 1 – Normal operation	PDTOT# 0 – Power down TMDS, gate off internal clocks 1 – Normal operation

Note: This is a Device 0x7A register.

Transmitter Mode after Reset

The SiI9022A transmitter core is modified for better performance compared to both the SiI9020 and SiI9022 devices. However, unlike these previous devices, the SiI9022A device powers up after a reset in a state where the TMDS transmitter is active. This function is controlled through existing Compatible Mode register bit 0x08[0], which defaults to 1 in the SiI9022A part after reset.

If it is desired to reset the device but then enter the lowest power standby state, write 0x08[0]=0 to turn off the transmitter core output.

Appendix B – Mobile HD Link

Silicon Image Mobile HD Link solutions carry digital video and audio streams over a reduced pin-count TMDS interface, but in a format that is readily converted for 100% HDMI compatibility.

The transmitter device and receiver/bridge device appear to software as an integral unit, in that remote functions such as CEC and EDID access appear to be local. Therefore, this appendix describes operation in terms of the combined transmitter-receiver solution.

Table B - 1. Mobile HD Link Products Described in this Appendix

HDCP-enabled Version	Non HDCP-enabled Version	Input Interface
SiI9222 Tx	SiI9226 Tx	RGB
SiI9232 Tx	SiI9236 Tx	RGB

Note: Data on Mobile HD Link products and features is provided here as **advance** information, and is therefore subject to change. Contact your Silicon Image representative for updates.

Figure B - 1 illustrates a typical Mobile HD Link implementation.

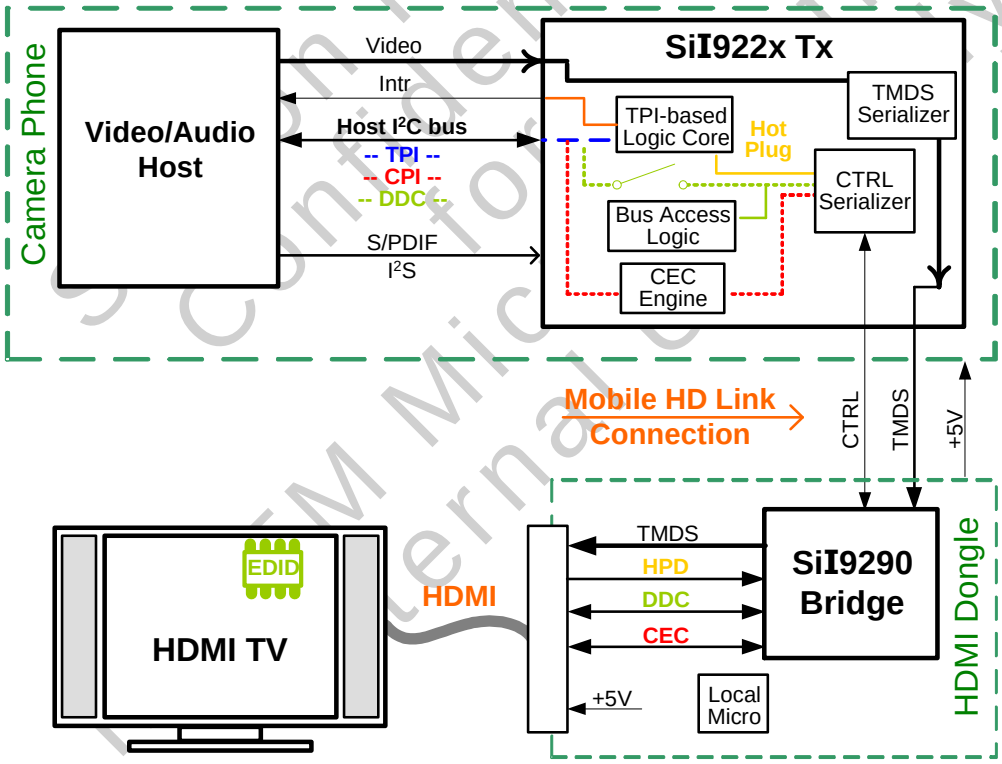


Figure B - 1. Typical Mobile HD Link Solution

Summary of Differences between HDMI and Mobile HD Link families. Designs using TPI and CPI with the SiI9022/24 Tx adapt to the SiI922x or SiI923x transmitter with virtually no software changes. The default TPI and CPI register sets have been maintained from the SiI9022/24 Tx. The main differences in support from a programmer's point of view are summarized as follows.

- The host decides when to allow the transmitter to "discover" a connected device, and must follow an explicit sequence to complete this discovery process.
- Most TPI register functionality is meaningful only when the transmitter is connected to the receiver/bridge device. Therefore, software must monitor Hot Plug status information using TPI 0x3C and 0x3D (either by hardware interrupt or by polling methods) before programming other TPI information.
- A non maskable interrupt is added to alert the host to unrecoverable cable connection errors.
- An interface known as the CTRL bus is used to transparently exchange DDC and CEC information with the remote Mobile HD Link receiver. A small amount of initialization and operational programming is required for the CTRL bus.
- The older SiI9020-compatible register interface is no longer supported.
- The I^2S audio input option is limited to two channels.

These differences are described in detail in the following sections.

Detailed Programming Requirements

The following programming information is in addition to the TPI programming described in the main part of this document.

I^2C Requirements

In the typical transmitter environment, the host masters the TPI/CPI/input DDC I^2C interface, and the transmitter-receiver combination masters the output DDC I^2C interface, as illustrated in Figure B - 1.

- **Host TPI/CPI/input DDC I^2C Interface.** The Tx implements this slave interface, mastered by the host. The host serially transmits and receives data over this bus, which implements a register interface structure where the host writes video mode control data and reads back connection status information.

  This link also allows host inter-chip register read/write access to the Mobile HD Link Bridge register set, through the Private Channel of the CTRL bus (see below).

- **Output DDC I^2C Interface.** The Mobile HD Link Tx and Bridge together implement this interface so that is appears as a pass-through connection from the host to the DDC bus of the HDMI TV. The transmitter has the ability to block the graphics host from accessing this bus, and also monitors the bus for activity to prevent breaking an active connection.

Identification

The ID registers return the TPI family device ID and TPI revision ID. The ID registers are listed in the tables below.

Access. These registers are accessed as single bytes.

Table B - 2. TPI Identification Registers (RO)

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1B	TPI Family Device ID							
0x1C	Rsvd				Device Revision ID			
0x1D	Rsvd = 0	TPI revision level (major.minor)						

Table B - 3. Device ID Information

Device	Input Type	Device ID TPI 0x1B	TPI Revision ID TPI 0x1D	Sub-Identifier* at 0xBE with 0xBC=01, 0xBD=02	HDCP Available? TPI 0x30
SiI9226 Tx	RGB	0xB0[1]	0x00[2]	0x22	No
SiI9222 Tx	RGB	0xB0[1]	0x00[2]	0x22	Yes
SiI9232 Tx	RGB	0xB2	0x00	0x32	Yes
SiI9236 Tx	RGB	0xB2	0x00	0x32	No

Notes

1. The Device ID of 0xB0 is also shared with the Silicon Image SiI9022/24 Tx. Following the sequence below enables the host to uniquely identify the transmitter.

```
1. Write 0xBC=0x01   // Internal page 1
2. Write 0xBD=0x03   // Indexed register 03
3. Read 0xBE         // Returns 0x92 for SiI 92xx Tx series
4. Write 0xBD=0x02   // Indexed register 02
5. Read 0xBE         // 0x20? 9224 Tx; 0x22? 9222/9226 Tx; 0x32? 9232/9236 Tx
6. Read TPI 0x30     // Returns 0 for non HDCP parts
```

Initialization

Mobile HD Link transmitters typically share their connector pins with other signals, and therefore must stay off the buses until a connection with a receiver is requested. Once a connection is needed, the transmitter and bridge devices must go through an automatic Discovery process for each of them to verify that a compatible Mobile HD Link device is connected on the other end.

Reset

For Reset of the SiI9222/9226 Tx, the transmitter host processor **must** always follow this procedure.

1. Drive the CSCL input pin low.
2. Drive the RST# input low, hold for at least 50us, then release.
3. Release CSCL and program the chip as usual.

This process forces the device to come up in a mode where the TMDS and CTRL pins will not drive the bus.

Connection and Discovery

To enable the Tx device to communicate with an attached bridge device, the Tx must "discover" the bridge. The host processor initiates this process as follows.

1. Write TPI 0x1E[4]=1. This bit enables the CTRL pin to drive out, and starts the Discovery process. Refer to Table B - 6.
2. Read the Link Control Bus Status Register 0x0A[0] to verify that the Control Bus is connected. This bit is located in the Link Control Bus register space. Refer to the Link Control Bus Programmer's Reference, SiI-PR-0031, for information.

CTRL Bus Configuration

An additional step is required in the program flow for Mobile HD Link devices under "Hot Plug Service".

Hot Plug Service. Until a device is attached, the host just monitors the connection status either through interrupts or by polling. The host software waits for an attached Sink hot plug event, and then:

- Initializes the Bridge CTRL bus registers
- Reads the downstream Sink EDID information
- Sends active video corresponding to the Sink capabilities, and selects DVI or HDMI mode, depending on the EDID information found
- Sets the subsystem to Operational (D0) state.

The Tx and Bridge together implement the CTRL Bus protocol across the CTRL pin, to transparently perform EDID reads, CEC exchanges, and various status information exchanges.

Initializing the CTRL Bus Registers

The host microcontroller, and optionally the bridge microcontroller as well, have the ability to carry out additional communication through the CTRL bus interface using the Private Channel registers. The full set of Private Channel registers is not documented here; contact Silicon Image for additional information.

However, the Tx host must minimally set up the CEC Logical Address using the Private Channel registers. This process is explained below.

I^2C Access Address. The I^2C address used to access the CTRL bus registers from the Tx is 0xC8. An alternate address of 0xCC is available, selected by strap setting as described in the specific data sheet for the chip.

Two Tx offset addresses are listed. Tx0 refers to the Primary connection on a Bridge chip, and Tx1 to the Secondary connection. In general, only Tx0 is available.

Table B - 4. CTRL Bus – Command Registers

Offset (device 0xC8)		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX0	TX1								
		Private Channel Execution Control Register Set only one bit at a time. Once executed, these bits are self-clearing.							
0x12	0x52								Forward Opcode 0=No action 1=Execute
0x13	0x53	**Command Opcode Register** ***Forwarded Opcodes.*** Before triggering a forwarding action (0x12[0]=1), the local host writes the opcode here.							

Table B - 5. CTRL Bus – Command Definitions

Code	Command	Description
0x66	SET_CEC_LADDR	Set CEC Logical Address and valid bit
0x67	GET_CEC_LADDR	Get CEC Logical Address and valid bit

The typical programming sequence would be as follows.

Write (to I^2C Device 0xC8):

```
1. 0x13=0x66   // load 'Set CEC Logical Address' command
2. 0x12=0x01   // issue 'Start Private Channel Transaction' command
3. 0x13=0x67   // load 'Get CEC Logical Address' command
4. 0x12=0x01   // issue 'Start Private Channel Transaction' command
```

Transmitter Power State

Mobile HD Link devices support ACPI-type power state control through the standard TPI register described elsewhere in this document. Refer to the Data Sheet for information on the various power savings that can be achieved at each level of ACPI power states D0, D2, and D3. Transition from D0 to any other state requires only a write to the Power_state[1:0] bits.

For the D3 power state, there are two power scenarios possible depending on the system design.

- **Attached State.** If the cable is plugged in, simply selecting D3 state will result in the lowest power.
- **Unattached State.** If cable is unplugged, selecting D3 state alone will not result in the lowest power state. Instead, the sequence should be:

    a. Drive CSCL low

    b. Assert and then release Reset

    c. Release CSCL

    Selecting D3 state will now leave the chip in its lowest power state. Subsequently leaving D3 state will require a Reset with CSCL released (not driven low).

Access. This register is accessed as a single byte.

Table B - 6. TPI Device Power State Control Data (R/W)

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1E [02]	Rsvd			CTRL Pin Control 0 = Tri-state 1 = Driven by Tx and Bridge as needed	Rsvd	Rsvd	Tx Power_ State[1:0] 00, 01 = D0 state (full operation) 10 = D2 state (standby mode) 11 = D3 state (shutdown mode)	

CTRL Pin Control. The CTRL signal on the mobile connector may be shared with other device signals. When cleared to 0, the CTRL Pin Control bit forces the Tx to tri-state its CTRL drive output, leaving the connector signal free for other compatible uses. This bit has an effect only after the Unattached State sequence above has been followed (without going to D3 state). Doing so leaves the CTRL pin tri-stated by default, which also prevents DDC bus usage. To subsequently resume normal operation with full DDC bus functionality available, the host would need to write this bit to 1.

Maximum Speed Limitations

The output frequency of the TMDS clock is the product of the input clock frequency, the `TClkSel` setting, and the 3x Mobile HD Link encoding multiplier. The system software engineer must ensure that the resulting frequency does not exceed the operational limits of the chip (225MHz). If such a multiplier is selected and results in excessive operating speed, the chip state machines on both the transmitter and bridge may lock up. This situation is recoverable only by a hardware reset of each component.

Interrupt Service

Because the Mobile HD Link establishes a "virtual" link from the host to the HDMI interface, certain ones of its TPI-level interrupts represent multiple underlying sources within the Internal Register set.

TPI 0x3D[0]: Hot Plug/Connection Event

The TPI 0x3D[0] event will be indicated when any of the Internal Event bits below are enabled to generate an interrupt.

1. Virtual HPD Event in Internal Register bit 0x71[6]. This event is always enabled.
2. Events in Internal Register bits 0x74[6:2]; the corresponding bit in 0x78[6:2] must be enabled generate INT.
3. The CTRL Bus Heartbeat Failure Monitor in Internal Register 0x74[7]. This bit simply reflects the status of bit CTRL 0x1E[3] (in the 0xC8 register space).

Write 1 to the appropriate register bit to clear the corresponding event pending status. In the case of the CTRL Bus Heartbeat Failure Monitor event, use CTRL 0x1E[3] to clear the event. Refer to the *Link Control Bus Programmer's Reference* (SiI-PR-1031) for information.

Table B - 7. Connection Event Triggers

Internal Registers available at **0xBE** when:	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0xBC=**00** 0xBD=**71** [00]	**Interrupt Status Register (R/W)** Write '1' to clear pending status							
		Virtual HPD Event Pending (INT always enabled) 0 = No 1 = Yes						
0xBC=00 0xBD=**74** [00]	**Interrupt Status Register (R/W)** Write '1' to clear pending status							
	CTRL Heartbeat failure (RO) Use CTRL 1E[3] to clear (device 0xC8)		VBUS Staying low after MHD established and cable disconnected Event pending 0 = No 1 = Yes	Ctrl BUS Lockout Window Started Event pending 0 = No 1 = Yes	USB Mode Established Event pending 0 = No 1 = Yes	MHD Mode Established Event pending 0 = No 1 = Yes		
0xBC=**00** 0xBD=**78** [00]	**Interrupt Enable Register (R/W)**							
	0 = Disable 1 = Enable		0 = Disable 1 = Enable	0 = Disable 1 = Enable	0 = Disable 1 = Enable	0 = Disable 1 = Enable		

TPI 0x3D[1]: RxSense Event or CTRL Bus Error

The TPI 0x3D[1] event will be indicated when any of the Internal Event bits below are enabled to generate an interrupt.

1. Internal Register RxSense Event (see below). This event is always enabled.
2. CTRL Bus register bits 0x08[7:5], 0x08[2:0], 0x1E[4], 0x1E[2:1]. These bits are in the 0xC8 device space. Refer to the *Link Control Bus Programmer's Reference* (SiI-PR-1031) for information.

Write 1 to the appropriate register group to clear the corresponding event pending status.

Table B - 8. CTRL Bus Error Event Triggers

Internal Registers available at **0xBE** when:	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0xBC=**00** 0xBD=**71** [00]	**Interrupt Status Register (R/W)** Write '1' to clear pending status							
			RxSense Event Pending (INT always enabled) 0 = No 1 = Yes					

TPI 0x3D[2]: CTRL Bus Transaction Event

The TPI 0x3D[2] event will be indicated when any of the Internal Event bits below are enabled to generate an interrupt. This register bit has a dual function, controlled by TPI 0x3C[2], which must be set to 1 to use the CTRL bus interrupt monitoring function.

1. CTRL Bus (device 0xC8) registers 20 to 23; bits must be enabled to generate INT
2. CTRL Bus register bits 0x08[4:3] or 0x0E[0]; bits must be enabled to generate INT.

Write 1 to the appropriate register group to clear the corresponding event pending status.

Non Maskable Interrupt

The Interrupt Status register for the SiI922x Tx implements a special non maskable interrupt function for Mobile HD Link devices.

Table B - 9. TPI Interrupt Status (R/W)

Offset	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0x3D [00]	HDCP Authentication status change event pending 0 – No 1 – Yes	HDCP V* Value ready event pending 0 – No 1 – Yes	Security Status Change event pending 0 – No 1 – Yes	Audio Error Event pending 0 – No 1 – Yes	Rx Sense or CPI Event pending state (RO) 0 – No Rx sensed/CPI 1 – Powered Rx attached/ CPI event pending	Hot Plug pin current state (RO) 0 – Low 1 – High	Receiver Sense event pending 0 – No 1 – Yes	Hot Plug event pending 0 – No 1 – Yes
	←——— **Non Maskable Interrupt (SiI922x Tx only):** Byte returns 0xFF (cleared only by hardware Reset) ———→							

Non Maskable Interrupt (SiI922x Tx only). Should an unrecoverable condition arise, TPI 0x3D will return 0xFF. This value (all interrupts triggered at once) indicates an error on the CTRL bus, typically due to poor connectivity. The only correct host response to a Non Maskable Interrupt is to perform a hardware reset to the chip, and to then re-initialize it.

Appendix C – HDMI 1.4 HEAC Support

The SiI9334 Tx offers HDMI 1.4 Ethernet and Audio Return Channel (HEAC) features.

- The Audio Return Channel (ARC) allows the transmitter to accept S/PDIF audio input from the downstream HDMI 1.4 receiver device.
- The Home Ethernet Channel (HEC) allows the transmitter to pass Ethernet signalling to/from the downstream HDMI 1.4 receiver device.

These features are configured and enabled through the following registers.

I^2C Access Addresses. The I^2C address used to access the HEAC registers is 0x90. The logic can optionally respond at address 0x94 depending on the CI2CA hardware strap setting described in the transmitter Data Sheet.

Table C - 1. HEAC Module Configuration 1 (R/W)

Addr 0x90 Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	HEAC Module Configuration – These registers **must** be set when using any of the HEAC features.							
0x04 [00]	Internal Test Use Write as 1 always.	Band gap bias current calibration for HEAC module. Program setting = 0b100			Band gap voltage reference calibration for HEAC module. Program setting – 0b100			Band gap voltage reference 0 – Disable 1 – Enable
0x05 [00]	Rsvd		HEAC termination control setting Program = 0b00101					HEAC termination 0 – Disable 1 – Enable
	Ethernet Control Group							
0x08 [00]	Rsvd	Ethernet Tx input coarse gain control. Program setting = 0b01000					Rsvd	Ethernet Tx input 0 – Disable 1 – Enable
0x09 [00]	Rsvd					HEAC Differential mode driver 0 – Disable 1 – Enable	Rsvd	
0x0C [00]	Rsvd	Ethernet Rx output gain control Program setting = 0bxxxxxx						Rsvd
0x0D [00]	Rsvd							Ethernet driver 0 – Disable 1 – Enable
0x10 [00]	Rsvd							
0x11 [00]	Rsvd					Not used in Evita Write as 1 always	Not used in Evita Write as 0 always	Differential resistor enable 0 – Single Mode 1 – Common Mode

Table C - 2. HEAC Module Configuration 2 (R/W)

Addr 0x90 Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Ethernet Full Duplex Group							
0x0A [00]	Rsvd					HEAC receiver full duplex normal gain path mute 1 – Normal 0 - Mute	HEAC receiver full duplex reduced gain path mute 1 – Normal 0 - Mute	HEAC receiver full duplex Ethernet operation 0 – Disable 1 – Enable
0x0B [00]	Rsvd	HEAC receiver full duplex state differential gain control Program setting = 0b0xxxxx						Ethernet RX output 0 – Disable 1 - Enable
0x12 [00]	ARC output selection 0 – Single Mode 1 – Common Mode	ARC self biasing 0 – Common Mode 1 – Single Mode	HEAC receiver full duplex stage slew control Program setting = 0b000000					
0x0E [00]	Rsvd	S/PDIF output gain control Program setting = 0b0xx10					Rsvd	ARC sink S/PDIF output gain 0 – Disable 1 – Enable
0x0F [00]	Rsvd					ARC sink S/PDIF output driver 0 – Disable 1 – Enable	Rsvd	

Start by writing (to I^2C Device offset 0x90) the following register values:

1. 0x04 = 0xC9 // Enable band gap and program reference value
2. 0x05 = 0x0B // Enable termination and program value
3. 0x06 = 0x00 // Not used, program to 0x00
4. 0x07 = 0x00 // Not used, program to 0x00
5. 0x09 = 0x04 // Enable HEAC differential mode driver
6. 0x11 = 0x05 [0x04] // Program setting recommended
7. 0x12 = 0x80 [0x40] // ARC output selection / self bias and slew rate

To continue to configure HEC:

8. 0x08 = 0x21 (0x00) // Enable Ethernet TX input and program gain
9. 0x0A = 0x05 (0x00) // Enable full duplex Ethernet operation
10. 0x0B = 0x7F (0x00) // Enable Ethernet RX output and program full duplex differential gain
11. 0x0C = 0x7E (0x00) // Set Ethernet RX output gain
12. 0x0D = 0x01 (0x00) // Enable Ethernet driver
13. 0x10 = 0x00 // RSVD
14. 0x0E = 0x00 // Disable SPDIF output gain
15. 0x0F = 0x00 // Disable SPDIF output driver

To continue to configure ARC:

16. 0x0E = 0x09 [0x39] // Enable SPDIF output and program gain
17. 0x0F = 0x04 // Enable SPDIF output path driver

Note:

Write values shown in ( ) are for either ARC CM or SM

Write values shown in [ ] are for ARC SM only

Example 1. To configure for ARC Common Mode with HEC:

1. 0x04 = 0xC9
2. 0x05 = 0x0B
3. 0x06 = 0x00
4. 0x07 = 0x00
5. 0x09 = 0x04
6. 0x11 = 0x05
7. 0x12 = 0x80
8. 0x08 = 0x21
9. 0x0A = 0x05
10. 0x0B = 0x7F
11. 0x0C = 0x7E
12. 0x0D = 0x01
13. 0x10 = 0x00
14. 0x0E = 0x09
15. 0x0F = 0x04

Example 2. To configure for ARC Single Mode only:

1. 0x04 = 0xC9
2. 0x05 = 0x0B
3. 0x06 = 0x00
4. 0x07 = 0x00
5. 0x09 = 0x04
6. 0x11 = 0x04
7. 0x12 = 0x40
8. 0x08 = 0x00
9. 0x0A = 0x00
10. 0x0B = 0x00
11. 0x0C = 0x00
12. 0x0D = 0x00
13. 0x10 = 0x00
14. 0x0E = 0x39
15. 0x0F = 0x04

Example 3. To configure for HEC only:

1. 0x04 = 0xC9
2. 0x05 = 0x0B
3. 0x06 = 0x00
4. 0x07 = 0x00
5. 0x09 = 0x04
6. 0x11 = 0x05
7. 0x12 = 0x80
8. 0x08 = 0x21
9. 0x0A = 0x05
10. 0x0B = 0x7F
11. 0x0C = 0x7E
12. 0x0D = 0x01
13. 0x10 = 0x00
14. 0x0E = 0x00
15. 0x0F = 0x00

Appendix D – SiI9136 Tx and SiI9334 Tx Features

The SiI9136 Tx and SiI9334 Tx offer special features not provided in other TPI transmitters.

- Extra support is provided for x.v.Color operation.
- 3D video mode capability provides support for many 3D modes listed in the HDMI 1.4 specification.
- General Purpose I/O (GPIO) pins can be configured to meet custom requirements.
- HEAC support is detailed in Appendix C.
- 16-bit color depth is programmable through the standard input and output format registers at 0x09-0A.

Additional information is provided below on the x.v.Color, GPIO, and 3D features.

Special x.v.Color Features

The SiI9136 Tx and SiI9334 Tx provide color space conversion and dedicated GBD packet support to improve x.v.Color operation. The color space conversion is described below; the GBD packet support is noted in the 3D Support section that follows.

Color Space Conversion

The SiI9136 Tx and SiI9334 Tx offer a color space converter that can map incoming RGB to the x.v.Color space.

For x.v.Color operation without any color space conversion, the programming is the same as the YCbCr 4:4:4 mode of operation: TPI 0x09[3:0] need to be set to 0x09, and TPI 0x0A[3:0] to 0x05. Conversion of data width and dithering is configurable as shown in Table 9 (video input/output format registers 0x09/0x0A bits [7:4]).

For x.v.Color operation with color space conversion, some additional programming is required. First, set TPI 0x09[3:0]=0x00 and TPI 0x0A[3:0]=0x01 to select RGB to YCbCr 4:4:4 conversion. Then, program the following sequence:

```
a) Write 0xBC=0x00     // Internal page 0
b) Write 0xBD=0x50     // Indexed register 50
c) Write 0xBE=0x03     // Access x.v.Color Control Register
```

The bit mapping of the x.v.Color configuration register written to TPI 0xBE is shown in the table below.

Table D - 1. x.v.Color Control (R/W)

Internal Register available at 0xBE when: 0xBC=00 0xBD=50	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	x.v.Color Control Register							
						Coefficient Override 0 – Disable (default) 1 – Enable	x.v.Color full scale output 0 – Disable (default) 1 – Enable	RGB to x.v.Color conversion 0 – Disable (default) 1 – Enable

Bit 2 of this register allows overriding the internal coefficient table for RGB to x.v.Color conversion. The coefficient table is mapped for access one byte at a time as shown in the table below. Software uses it to load the conversion matrix: TPI 0xBD to select the Index for the low or high byte of each 16-bit coefficient word, and TPI 0xBE to write the corresponding byte. Note that every index from 0x51 to 0x62 needs to be programmed to get satisfactory results.

Table D - 2. x.v.Color Coefficient Override Table Access (R/W)

	R to Y	G to Y	B to Y	R to Cb	G to Cb	B to Cb	R to Cr	B to Cr	C to Cr
Index, bits [15:8]	**0x52**	**0x54**	**0x56**	**0x58**	**0x5A**	**0x5C**	**0x5E**	**0x60**	**0x62**
Index, bits [7:0]	**0x51**	**0x53**	**0x55**	**0x57**	**0x59**	**0x5B**	**0x5D**	**0x5F**	**0x61**

3D Support

HDMI 1.4 defines 3D operation over HDMI. The SiI9136 Tx and SiI9334 Tx support 3D mode timing, and make special provisions to accommodate the extra InfoFrames needed.

A 3D video format is defined by the Video Identification Code (VIC) defined in the CEA-861-D standard, table 2, in conjunction with one of the extended 3D_Structure values defined in the HDMI 1.4 standard, table H-2. In addition to sending the VIC to the receiver using the standard AVI InfoFrame format, the transmitter needs to send the 3D_Structure value to the receiver using the HDMI Vendor Specific InfoFrame, defined in HDMI 1.4, sections 8.2.3, H.1 and H.2.

3D Formats Supported

The following 3D formats and resolutions are tested and supported, and include Deep Color depths up to 12 bits.

- 720p 50Hz Frame Packing
- 720p 59.94/60Hz Frame Packing
- 1080i 50Hz Frame Packing
- 1080i 59.94/60Hz Frame Packing
- 1080p 23.98/24Hz Frame Packing
- 1080i 50Hz Side-by-Side (Half)
- 1080i 59.94/60Hz Side-by-Side (Half)
- 1080p 23.98/24Hz Side-by-Side (Full)
- 720p 50Hz Side-by-Side (Full)
- 720p 59.94/60Hz Side-by-Side (Full)
- 720p 50Hz L+depth
- 720p 59.94/60Hz L+depth
- 1080p 23.98/24Hz L+depth

HDMI Vendor Specific InfoFrame

The HDMI Vendor Specific InfoFrame carries the 3D information to the receiver. It is defined in the HDMI 1.4 standard, sections 8.2.3, H.1, H.2. When the Tx transmits a 3D video signal, it must send an accurate HDMI Vendor Specific InfoFrame at least once per two video fields.

The HDMI Vendor Specific InfoFrame header is shown in the HDMI 1.4 specification. The fields that need to be set for transmission by the Tx are:

- 3D Structure, per HDMI 1.4 standard, table H-2.
- 3D_Ext_Data, for "Side-by-Side (Half)" only. It should be set to the required sampling method per the HDMI 1.4 standard, table H-3 (for example, set to 0 for "odd/left, odd/right horizontal sub-sampling method").

It is recommended that the MPEG InfoFrame buffer category be used for this InfoFrame type. The SiI9136 Tx and SiI9334 Tx offer a dedicated buffer, category 7, for GBD data. When category 7 (0xBF[2:0]= 111) is used for the GBD packet, it leaves category 3 (0xBF[2:0]= 011) available for the HDMI Vendor Specific InfoFrame entry.

The entry below is taken from Table 16 and emphasizes the recommended usage for SiI9136/9334 transmitters.

Table D - 3. SiI9136/9334 Tx InfoFrame Options (R/W)

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xBF [00]	I-F_SELECT							
	Enable	Repeat	Rsvd			Info Frame to load (SiI9136/9334 only) … 110 – HDMI VSIF 111 – Dedicated GBD		

Sink EDID Vendor Specific Data Block

HDMI 1.4 extends the Vendor Specific Data Block (VSDB) of the sink EDID to include information about the sink 3D support capabilities. The Tx firmware needs to parse that information in order to limit the sending of 3D video to sinks that support that 3D format.

Detailed specifications of the EDID VSDB are listed in the HDMI 1.4 standard, section H.3.

Pixel Clock

Except for the Side-by-Side (Half) 3D modes, all 3D modes supported require doubling of the pixel clock frequency, compared to the pixel clock frequency used with 2D video modes that have the same VIC.

Doubling the pixel clock is described in the Deep Color Operation paragraph of the Input Bus Format and Pixel Repetition section.

Limitations

Color space conversion is generally supported. However, support in Side-by-side format is limited – edge pixels (on the border between left and right images) will not be converted correctly and must be discarded. No color space conversion support is provided in 3D L+depth modes.

General Purpose I/O

The GPIO Pins can either act as inputs or outputs. The direction is configured individually, per pin, as noted in the table below.

Table D - 4. GPIO Configuration

Internal Registers available at **0xBE** when:	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0xBC=**03** 0xBD=**E0** [00]	**GPIO Rising Edge Trigger Register (R/W)**							
					Assert INT# on rising GPIO3 0 – Disable 1 – Enable	Assert INT# on rising GPIO2 0 – Disable 1 – Enable	Assert INT# on rising GPIO1 0 – Disable 1 – Enable	Assert INT# on rising GPIO0 0 – Disable 1 – Enable
0xBC=03 0xBD=**E1** [00]	**GPIO Falling Edge Trigger Register (R/W)**							
					Assert INT# on falling GPIO3 0 – Disable 1 – Enable	Assert INT# on falling GPIO2 0 – Disable 1 – Enable	Assert INT# on falling GPIO1 0 – Disable 1 – Enable	Assert INT# on falling GPIO0 0 – Disable 1 – Enable
0xBC=**00** 0xBD=**75** [00]	**GPIO Interrupt Status Register (R/W)** Write '1' to clear pending status							
					GPIO3 Event Pending 0=No 1=Yes	GPIO2 Event Pending 0=No 1=Yes	GPIO1 Event Pending 0=No 1=Yes	GPIO0 Event Pending 0=No 1=Yes
0xBC=03 0xBD=**E3** [00]	**GPIO Data Input Register (RO)**							
					GPIO3 0=Low 1=High	GPIO2 0=Low 1=High	GPIO1 0=Low 1=High	GPIO0 0=Low 1=High
0xBC=**03** 0xBD=**E2** [00]	**GPIO Data Output Register (R/W)**							
					GPIO3 0=Low 1=High	GPIO2 0=Low 1=High	GPIO1 0=Low 1=High	GPIO0 0=Low 1=High

GPIO Interrupt Status. Shows current status of GPIO trigger events that have been enabled in the Trigger registers. Write 1 to interrupt bits to clear the 'pending' status.

Example. The following describes how to configure GPIO0 and GPIO2 as input and GPIO1 and GPIO3 as output pins:

```
a) Write 0xBC=0x03
b) Write 0xBD=0xE0
c) Write 0xBE=0x05 // set OE_N for GPIO0 and GPIO2 pads
```

After configuring the pin polarity, output data is written using the sequence:

```
a) Write 0xBC=0x03
b) Write 0xBD=0xE2
c) Write 0xBE=0x0A // set output Pins GPIO1 and GPIO3 to 1
```

Reading input of GPIO is done by:

```
a) Write 0xBC=0x03
b) Write 0xBD=0xE3
c) Read  0xBE
```

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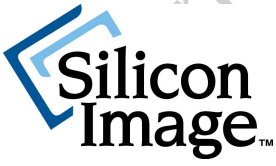

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